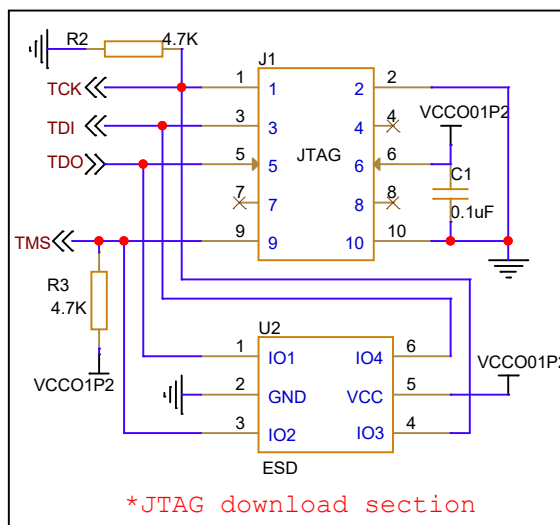
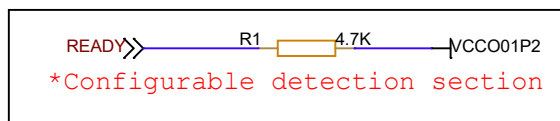
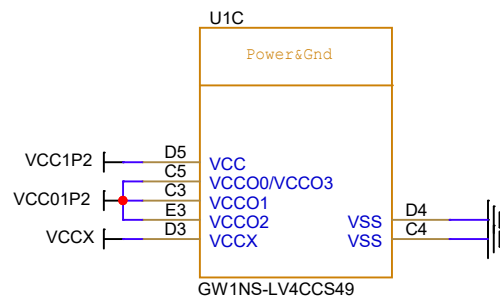
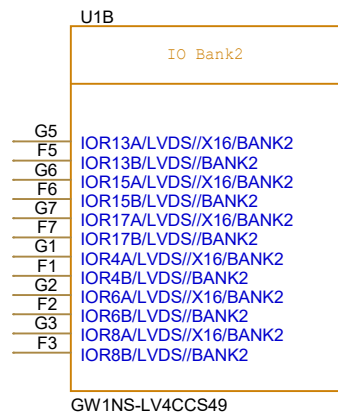
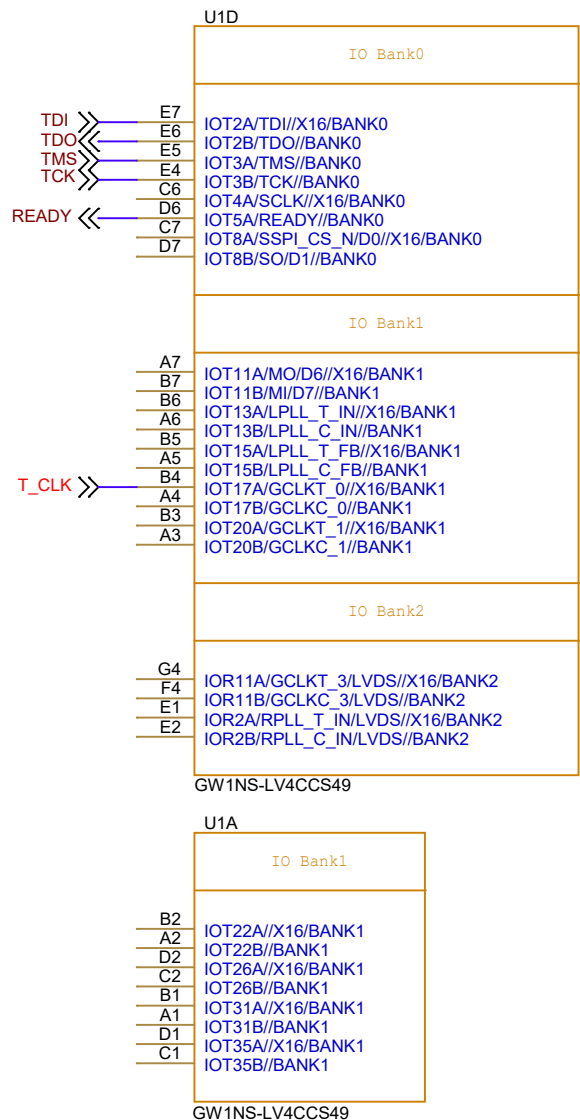
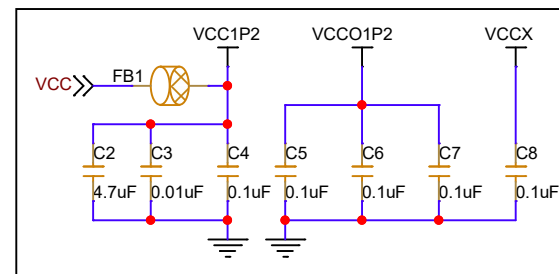


GW1NS-LV4CCS49



Recommended Operating Conditions of CS49 Package in GW1NS-4/GW1NS-4C			
Name	Description	Min.	Max.
VCC	Core voltage	1.14V	1.26V
VCCIO1, VCCIO2	I/O Bank voltage When MIPI input is used in BANK1, VCCIO1 should provide 1.2V voltage. When MIPI output is used in BANK2, VCCIO2 should provide 1.2V voltage.	1.14V	3.6V
VCCIO0/VCCIO3	I/O Bank voltage, VCCIO0/VCCIO3 are internally connected. When MIPI input is used in BANK0, VCCIO0 should provide 1.2V voltage.	1.14V	3.6V
VCCX	Auxiliary voltage	1.71V	3.6V

VCCX should be greater than or equal to VCCIO.

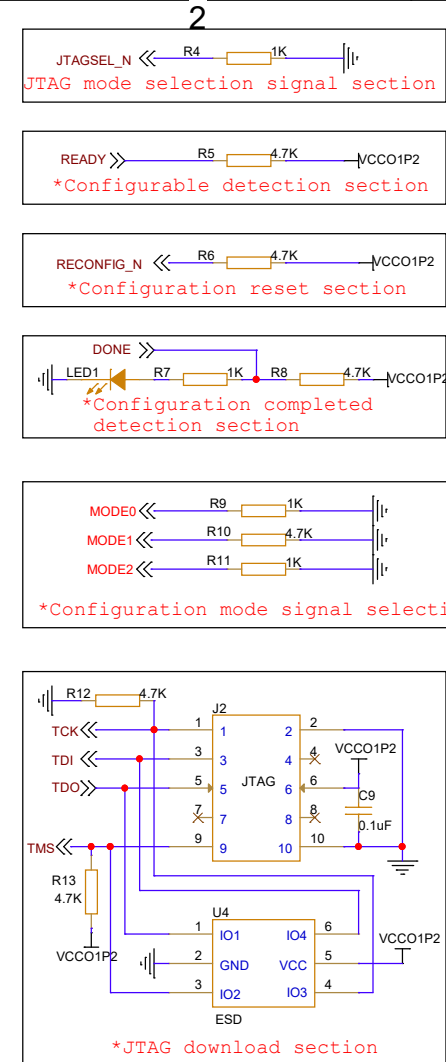
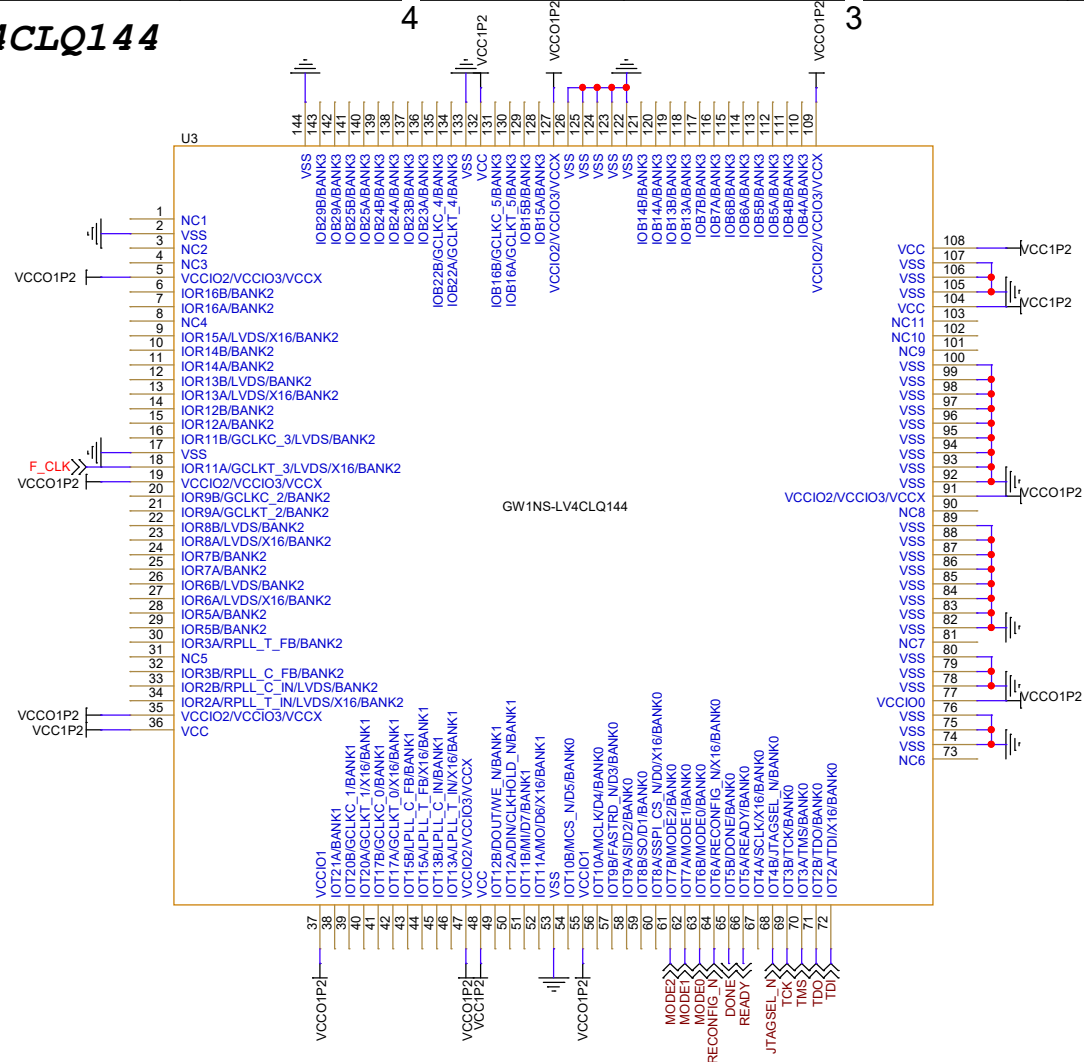


Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 3.The CS49 package supports GW1NS-4 & GW1NS-4C.

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GW1NS-LV4CLQ144



Name	Description	Min.	Max.
VCC	Core voltage	1.14V	1.26V
VCCIO0, VCCIO1	I/O Bank voltage When MIP1 input is used in BANK0 and BANK1, VCCIO0 and VCCIO1 should provide 1.2V voltage.	1.14V	3.6V
VCCIO2/VCCIO3/VCCX	I/O Bank voltage VCCIO2/VCCIO3 and auxiliary voltage VCCX are internally connected. When MIP1 output is used in BANK2, VCCIO2 should provide 1.2V voltage.	1.71V	3.6V

VCCX should be greater than or equal to VCCIO.

Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 3.The MG64 package supports GW1NS-4 & GW1NS-4C.

Title				
GOWIN Minimum System Diagram				
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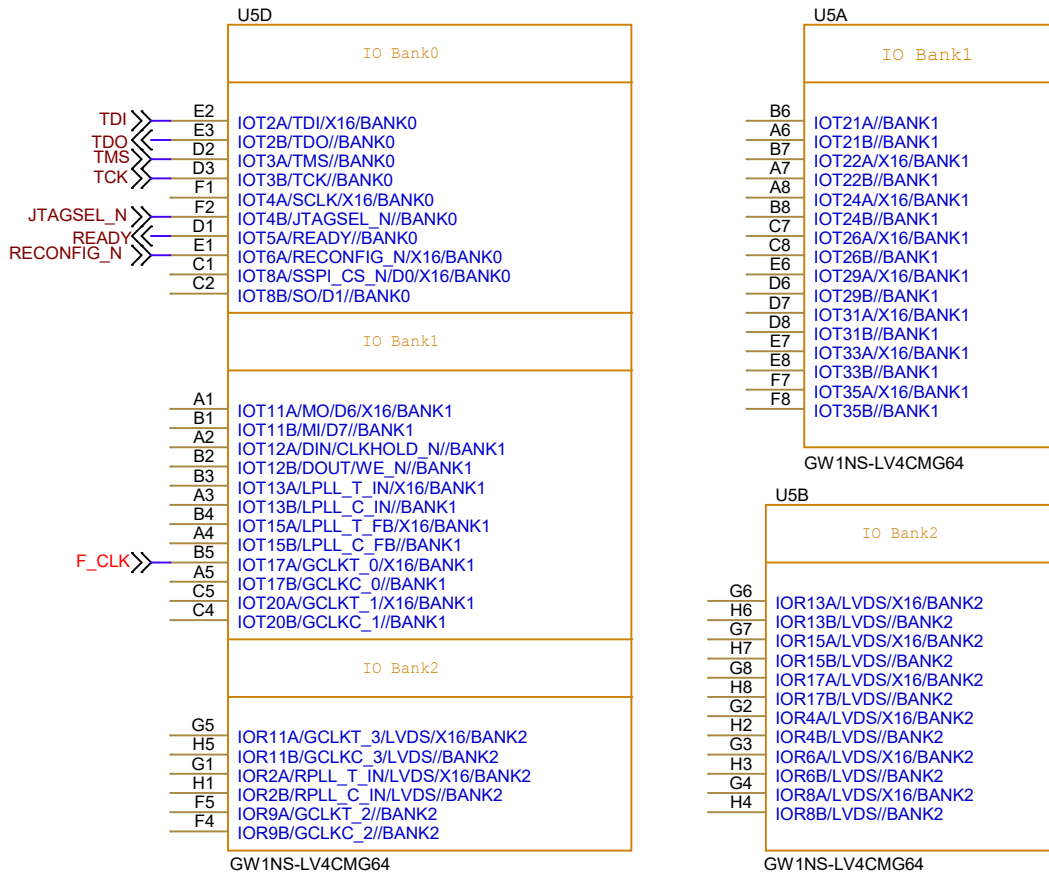
GW1NS-LV4CMG64

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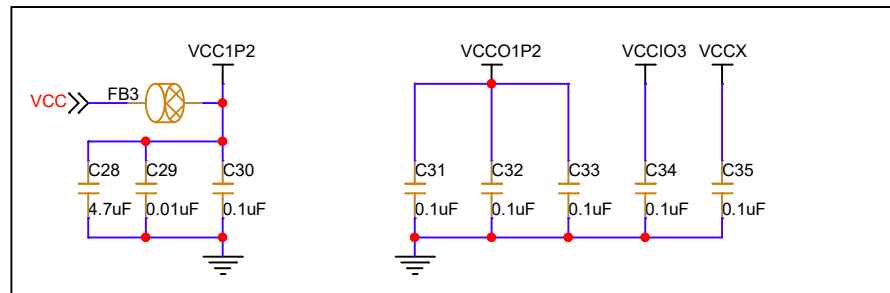
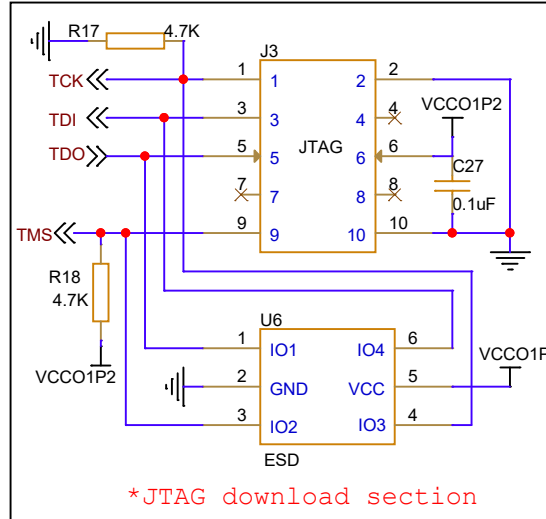
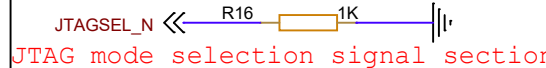
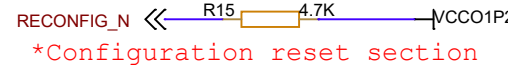
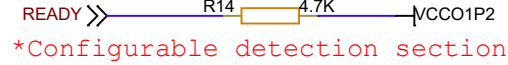
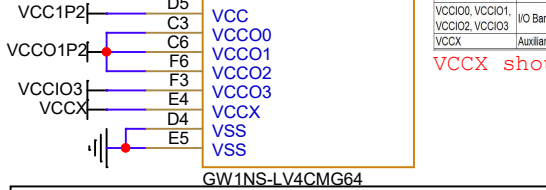
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Recommended Operating Conditions of MG64 Package in GW1NS-4/GW1NS-4C			
Name	Description	Min.	Max.
VCC	Core voltage	1.14V	1.26V
VCCIO0, VCCIO1, VCCIO2, VCCIO3	I/O Bank voltage	1.14V	3.6V
VCCX	Auxiliary voltage	1.71V	3.6V

VCCX should be greater than or equal to VCCIO.

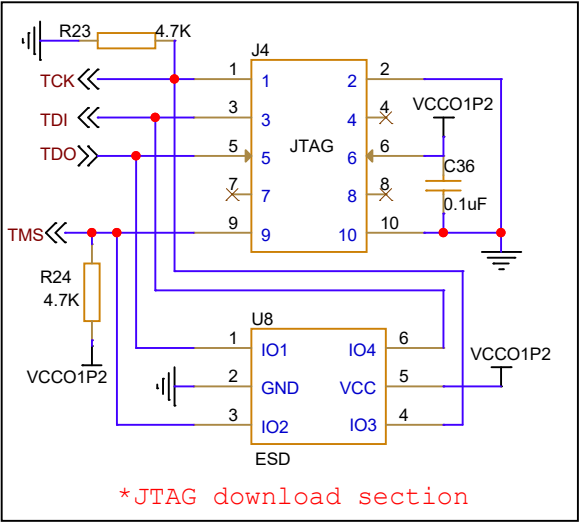
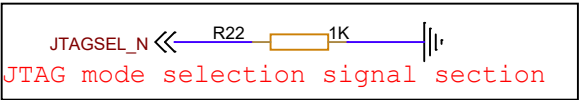
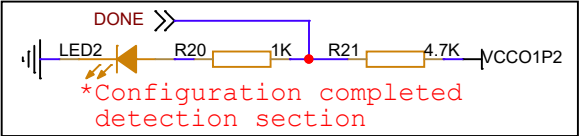
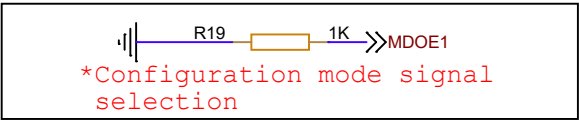
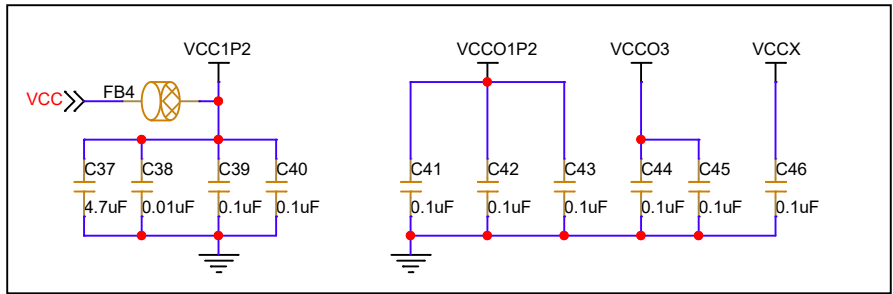
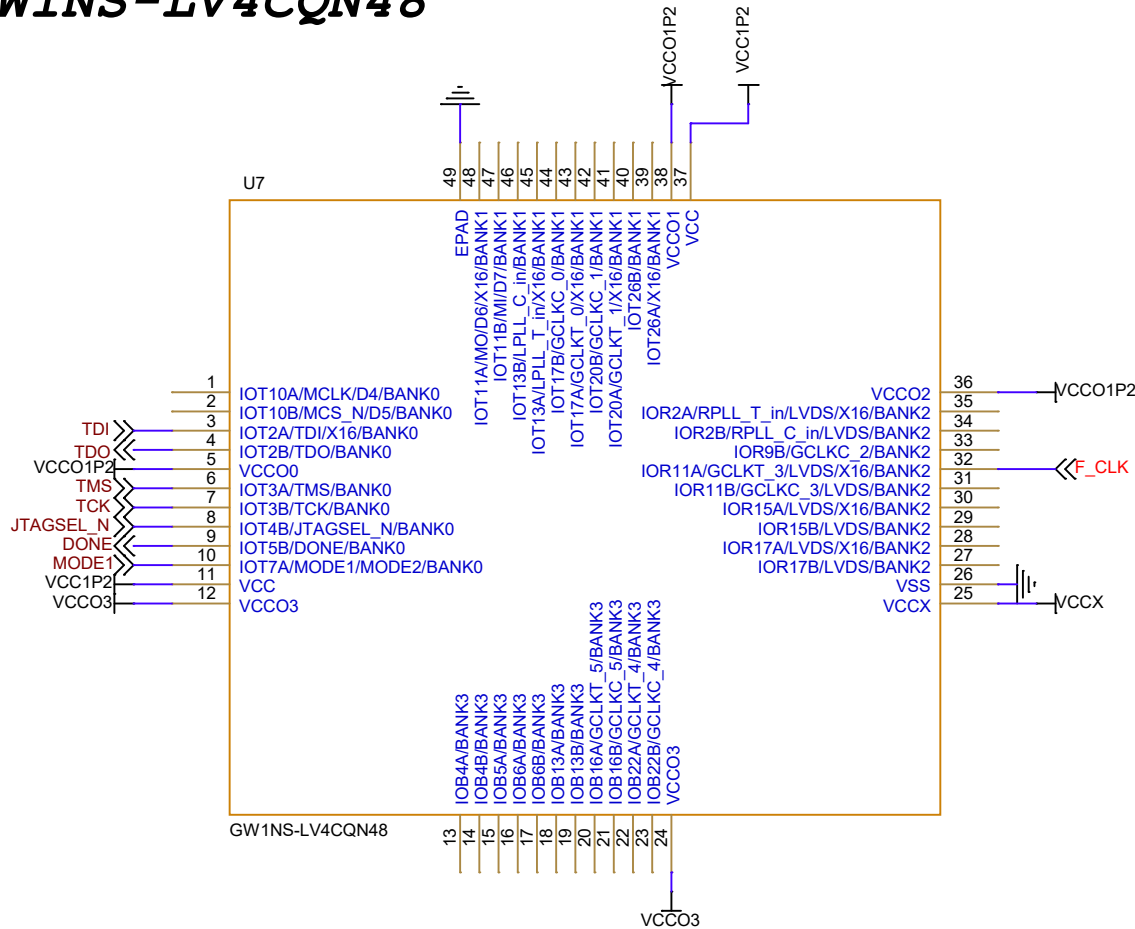


Notes:

- F_CLK signal is an external input clock signal. It is recommended that F_CLK signal be provided through an active oscillator crystal.
- It is recommended that add an ESD protection chip to the JTAG download circuit.
- The MG64 package supports GW1NS-4 & GW1NS-4C.

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GW1NS-LV4CQN48

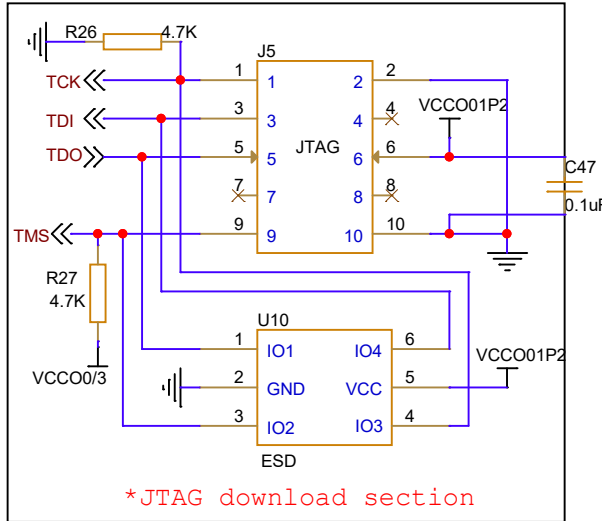
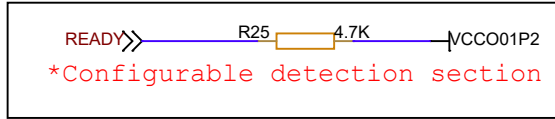
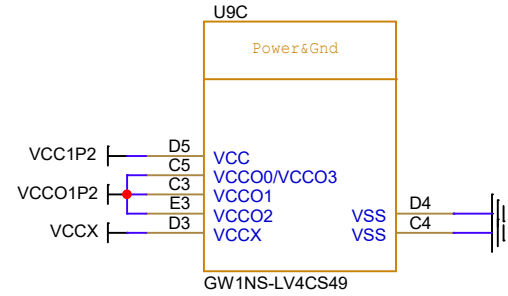
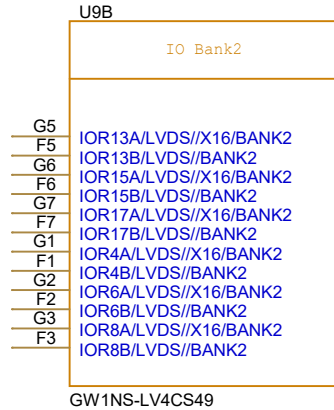
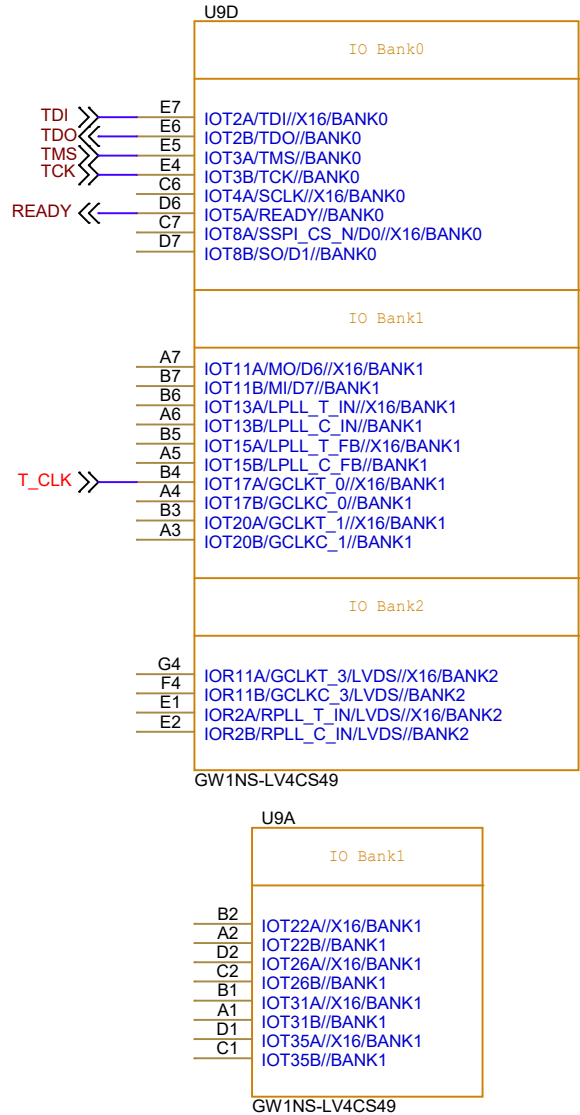


Recommended Operating Conditions of QN48 Package in GW1NS-4/GW1NS-4C			
Name	Description	Min.	Max.
VCC	Core voltage	1.14V	1.26V
VCCIO0, VCCIO1, VCCIO2, VCCIO3	I/O Bank voltage	1.14V	3.6V
VCCX	Auxiliary voltage	1.71V	3.6V

VCCX should be greater than or equal to VCCIO.

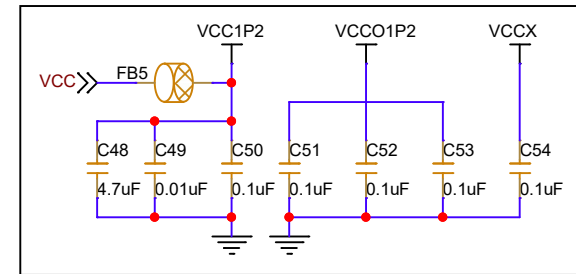
- Notes:
- 1.F CLK signal is an external input clock signal. It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.
 - 3.The QN48 package supports GW1NS-4 & GW1NS-4C.

GW1NS-LV4CS49



Recommended Operating Conditions of CS49 Package in GW1NS-4/GW1NS-4C			
Name	Description	Min.	Max.
VCC	Core voltage	1.14V	1.26V
VCCIO1, VCCIO2	I/O Bank voltage	1.14V	3.6V
VCCIO0/VCCIO3	I/O Bank voltage	1.14V	3.6V
VCCX	Auxiliary voltage	1.14V	3.6V

VCCX should be greater than or equal to VCCIO.

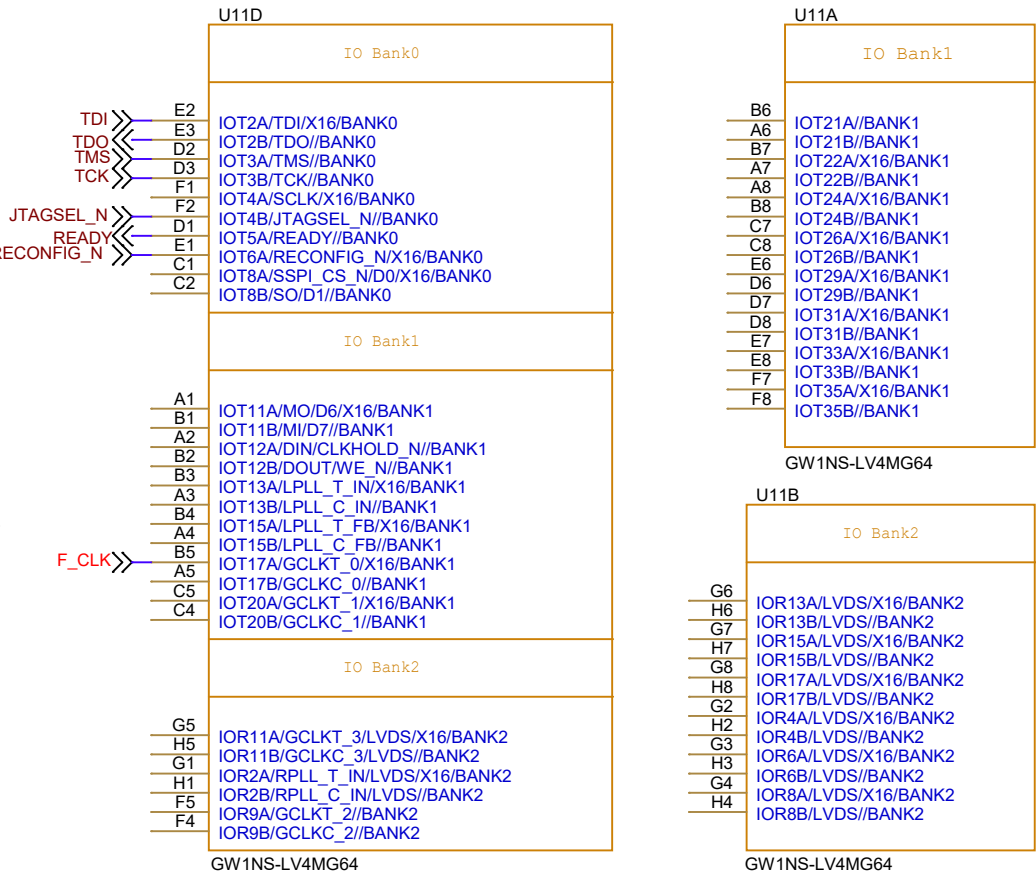


Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 3.The CS49 package supports GW1NS-4 & GW1NS-4C.

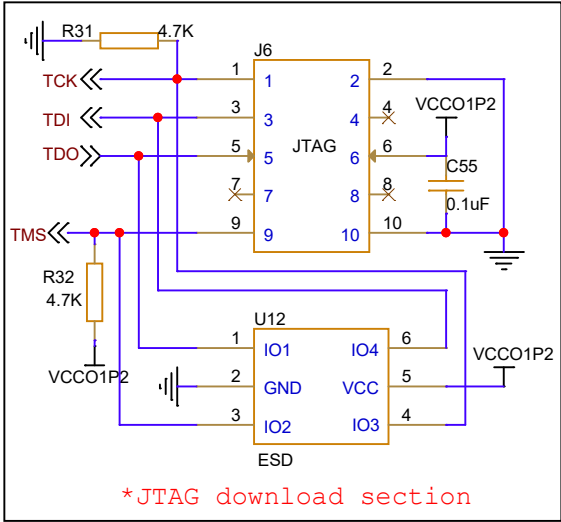
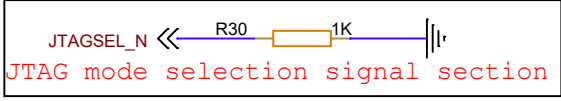
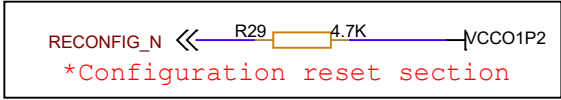
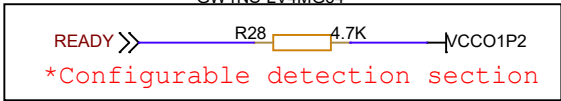
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GOWIN Minimum System Diagram		
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GW1NS-LV4MG64



Recommended Operating Conditions of MG64 Package in GW1NS-4/GW1NS-4C			
Name	Description	Min.	Max.
VCC	Core voltage	1.14V	1.26V
VCCIO0, VCCIO1, VCCIO2, VCCIO3	IO Bank voltage	1.14V	3.6V
VCCX	Auxiliary voltage	1.71V	3.6V

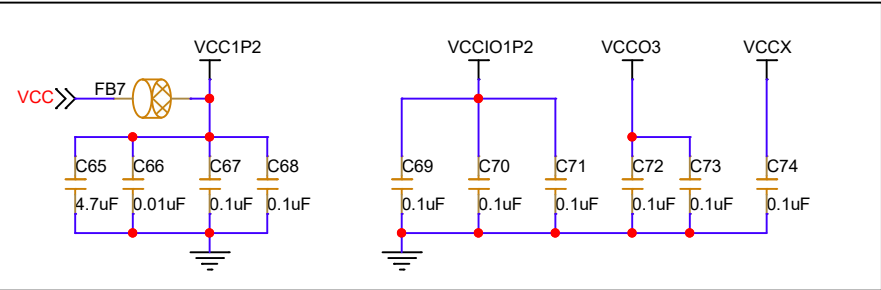
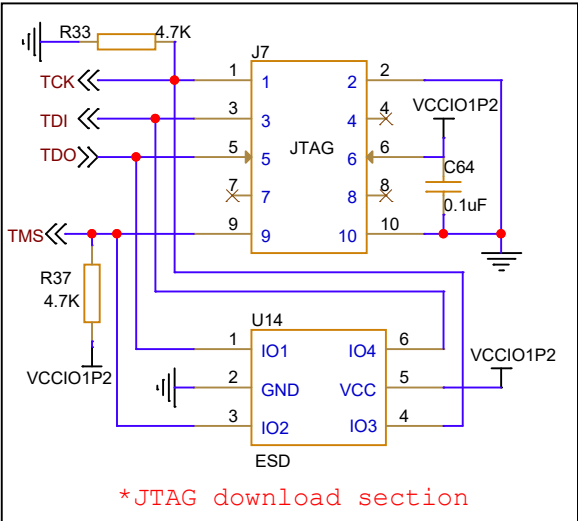
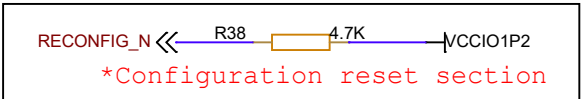
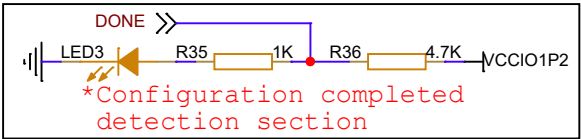
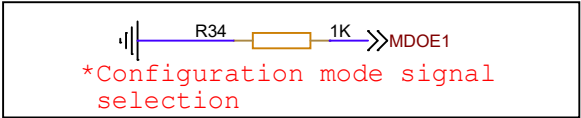
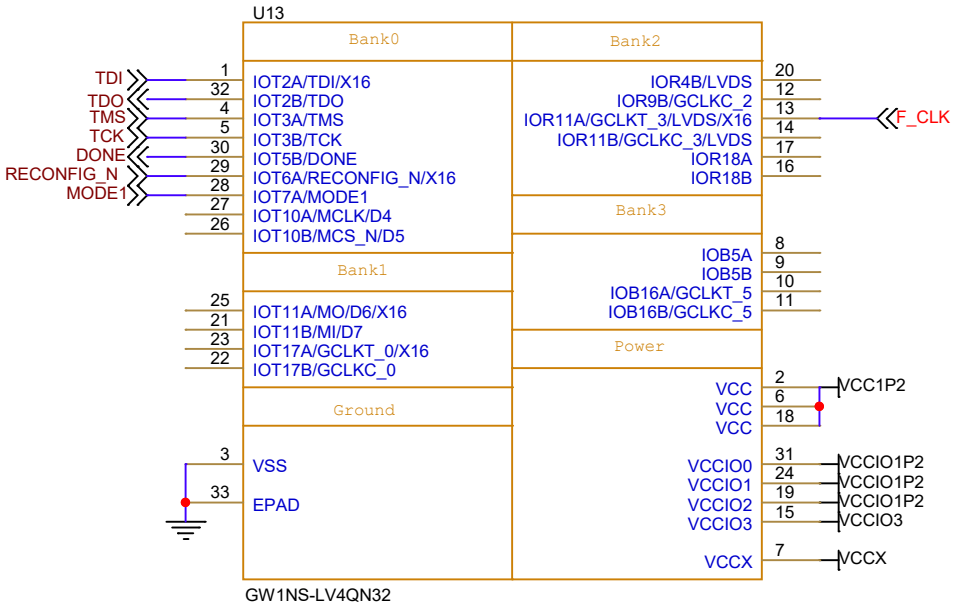
VCCX should be greater than or equal to VCCIO.



Notes:

- F_CLK signal is an external input clock signal. It is recommended that F_CLK signal be provided through an active oscillator crystal.
- It is recommended that add an ESD protection chip to the JTAG download circuit.
- The MG64 package supports GW1NS-4 & GW1NS-4C.

GW1NS-LV4QN32

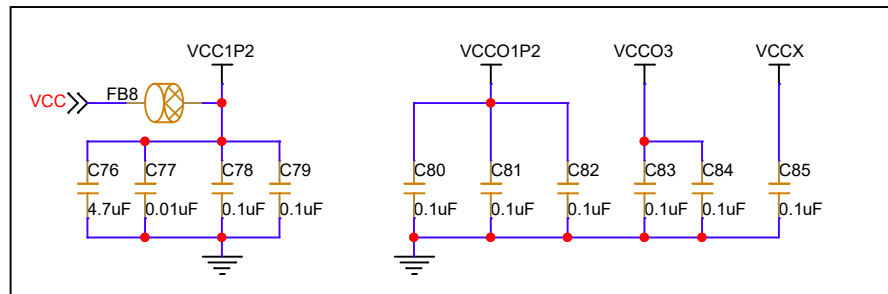


Recommended Operating Conditions of QN32 Package in GW1NS-4				
Name	Description	Min.	Max.	
VCC	Core voltage	1.14V	1.26V	
VCCIO0, VCCIO1, VCCIO2, VCCIO3	I/O Bank voltage	1.14V	3.6V	When MIPI input is used in BANK0 and BANK1, VCCIO0 and VCCIO1 should provide 1.2V voltage. When MIPI output is used in BANK2, VCCIO2 should provide 1.2V voltage.
VCCX	Auxiliary voltage	1.71V	3.6V	
Note ! It is highly recommended that the EPAD connect to GND, but not a requirement.				

VCCX should be greater than or equal to VCCIO.

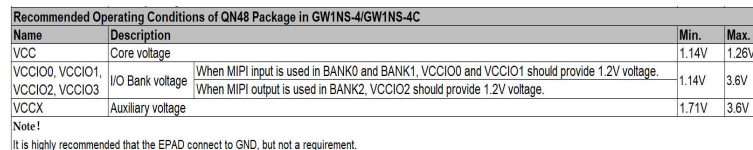
- Notes:
- F_CLK signal is an external input clock signal. It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - It is recommended that add an ESD protection chip to the JTAG download circuit.

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VCCX should be greater than or equal to VCCIO.