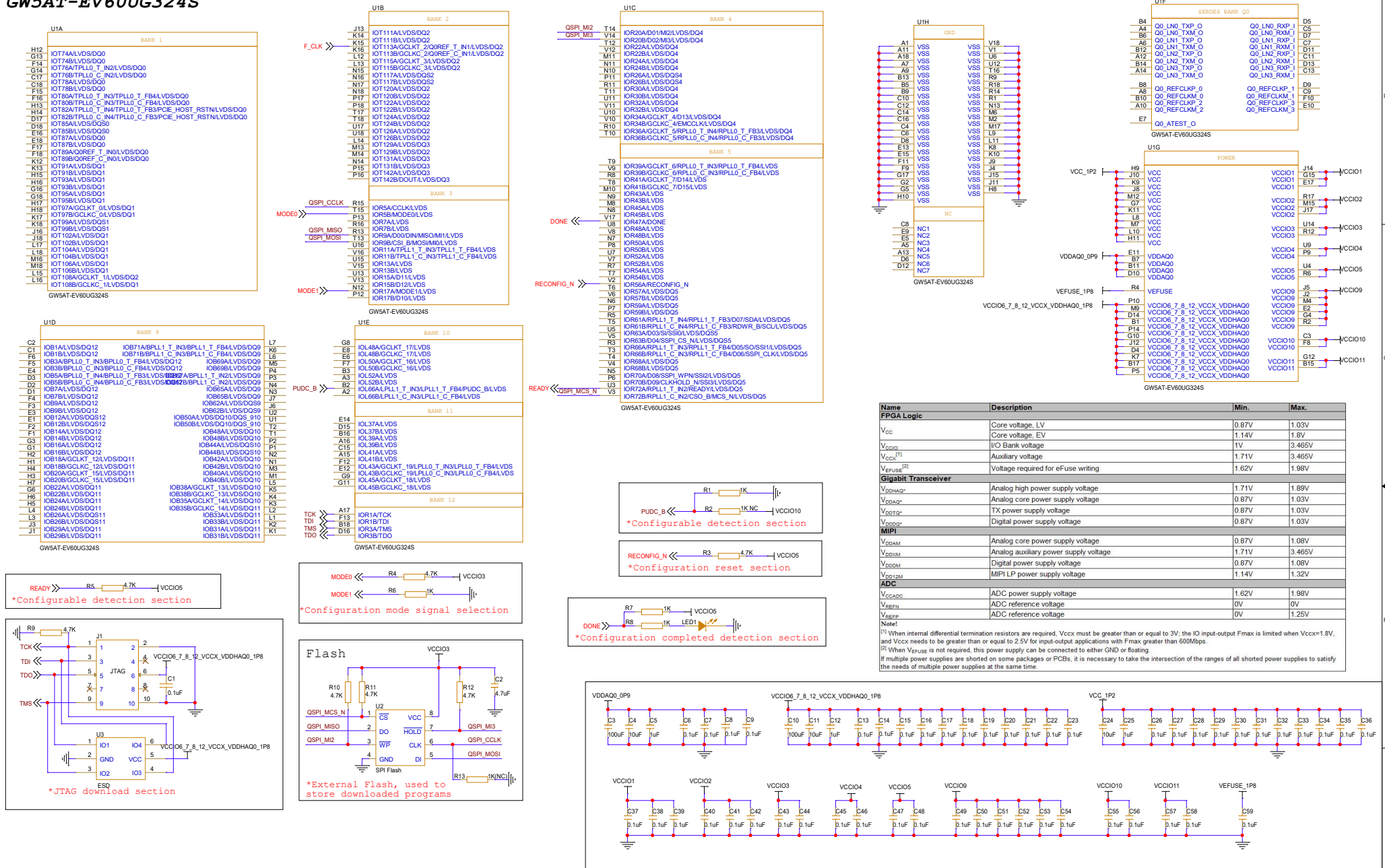


***GW5AT-EV60UG324S***

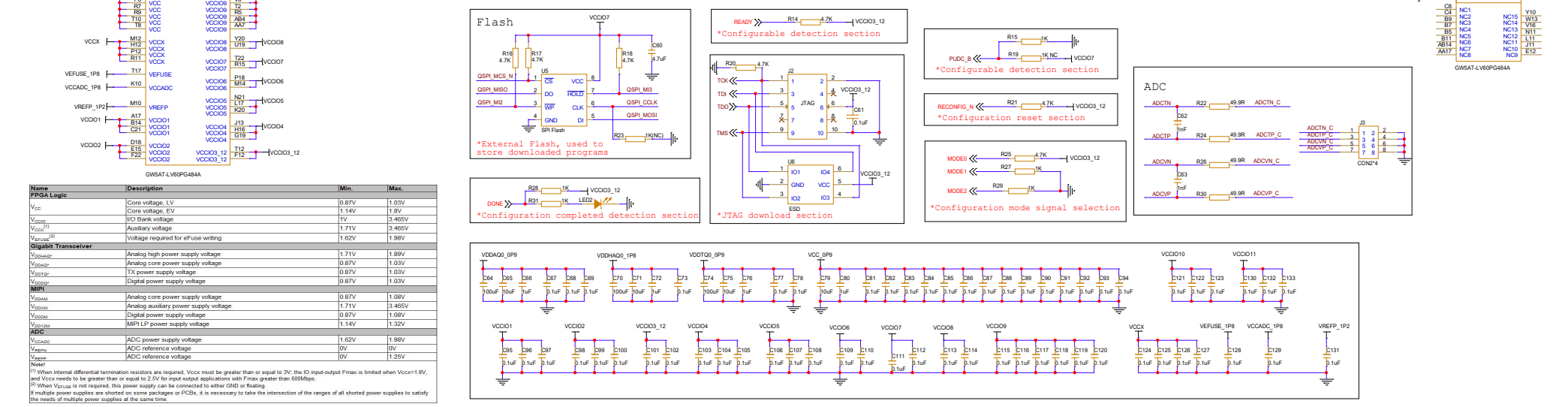


Notes:

1. F.CLK signal is an external input clock signal.
  - It is recommended that F.CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
  - For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. VCC core voltage requires a large current, so it is recommended to supply power separately.
5. The MODE pin is the GowinCONFIG configuration mode selection signal.
  - For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.
6. This package does not support the use of internal differential termination resistors.

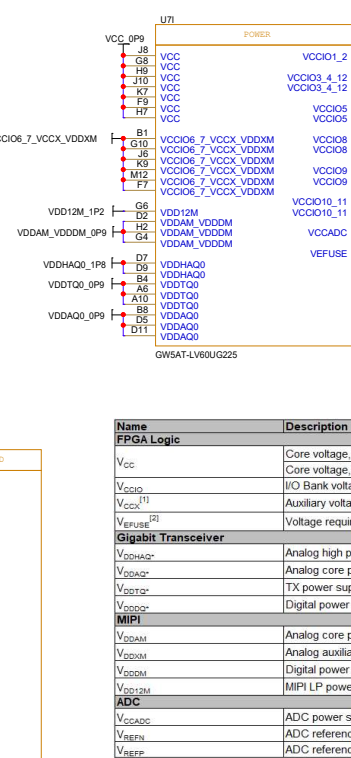
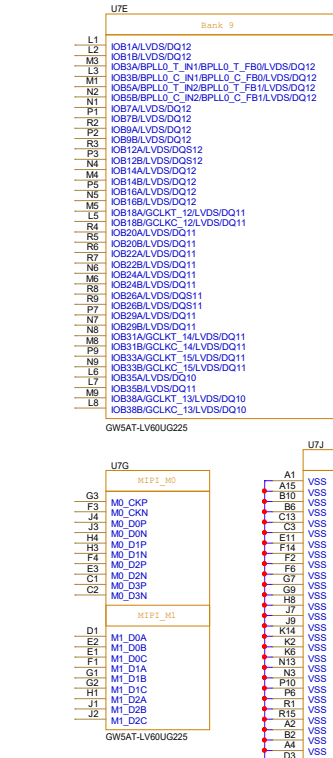
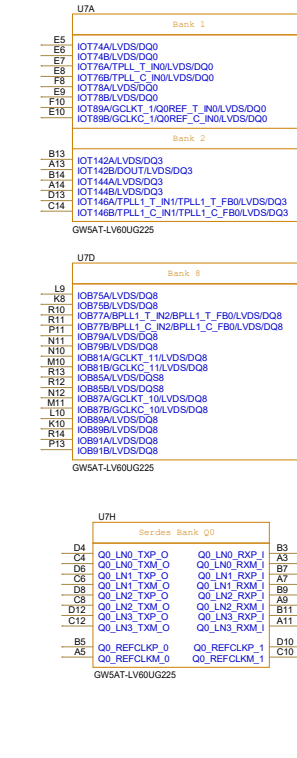
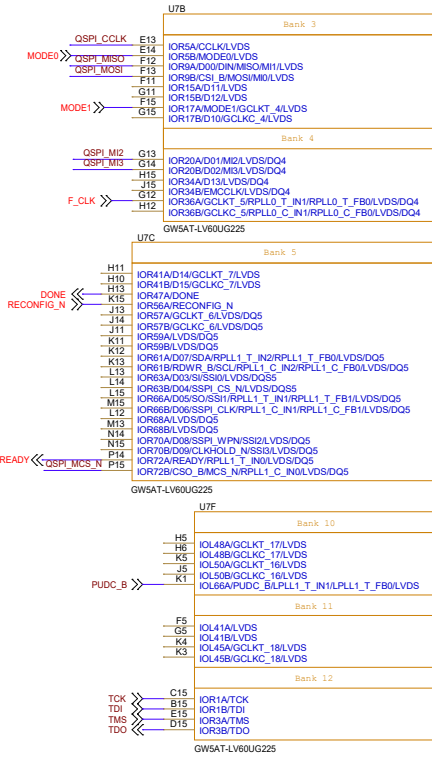
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GOWIN Minimum System Diagram			
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C	GW5AT-EV60UG324S		1.3
Date:	Friday, March 14, 2025	Sheet	1 of 5

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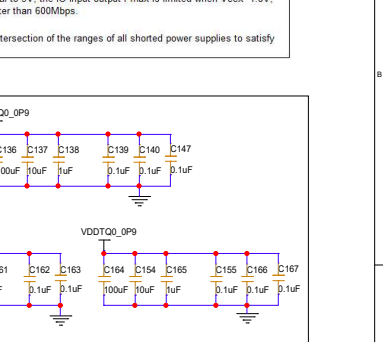
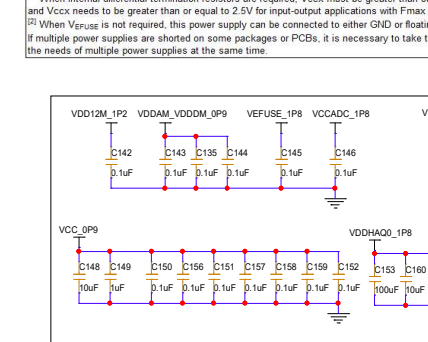
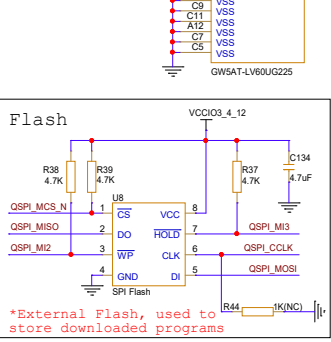
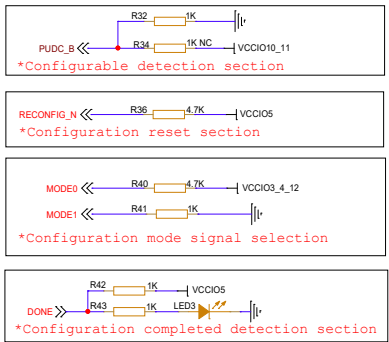
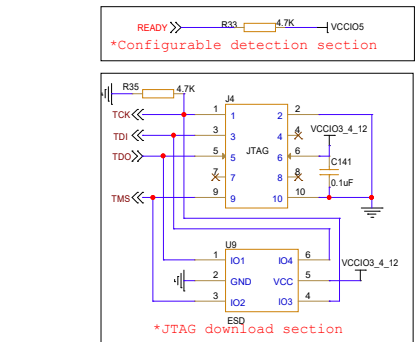


Notes:  
1.F CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.  
2.External Flash memory is used to store downloaded programs.  
For details about SPI Flash memory selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide .  
3.It is recommended that add an ESD protection chip to the JTAG download circuit.  
4.VCC core voltage requires a large current, so it is recommended to supply power separately.  
5.the MODE pin is the GowinCONFIG configuration mode selection signal.  
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.

# GW5AT-LV60UG225



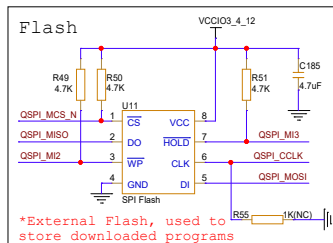
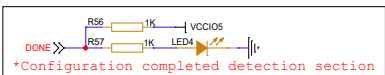
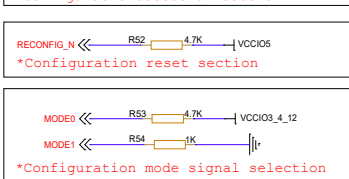
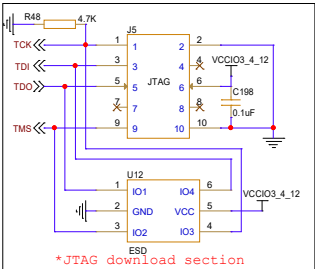
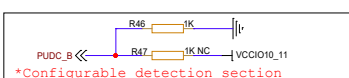
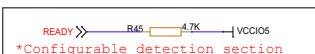
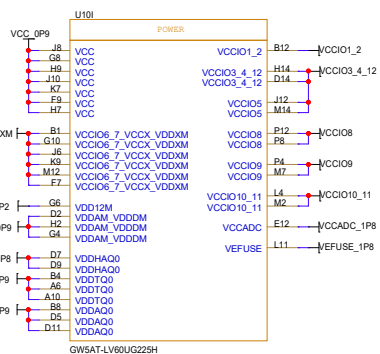
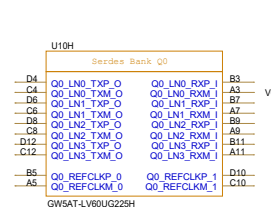
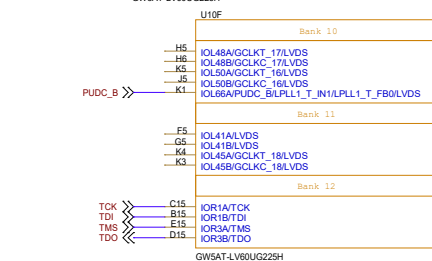
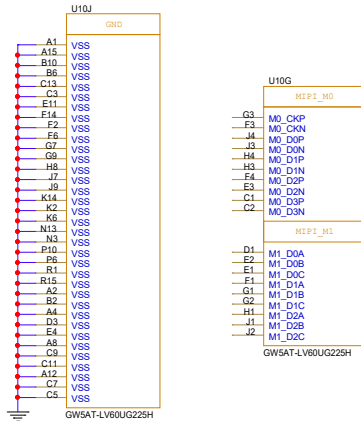
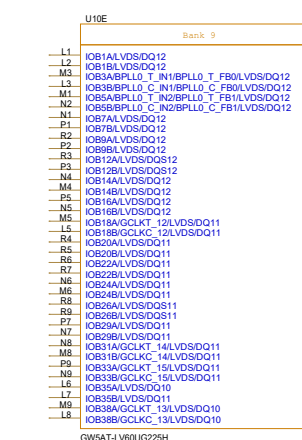
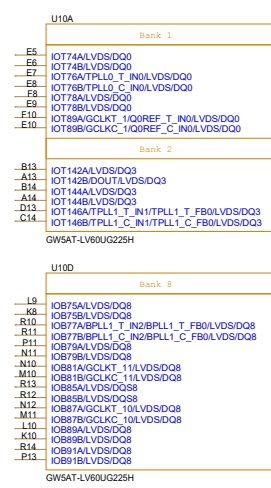
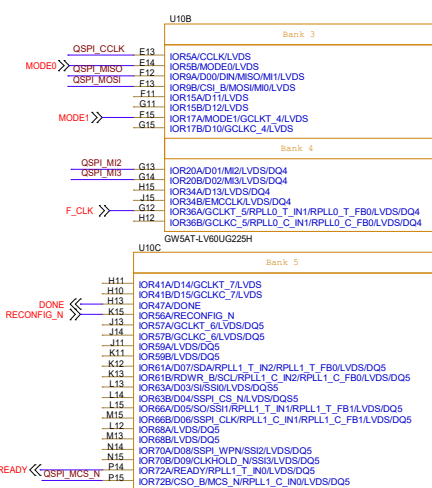
Name	Description	Min.	Max.
<b>Power</b>			
V <sub>CC</sub>	Core voltage, LV	0.87V	1.03V
V <sub>CC</sub>	Core voltage, EV	1.14V	1.8V
V <sub>IO</sub>	I/O Bank voltage	1V	3.465V
V <sub>CCX</sub> <sup>(1)</sup>	Auxiliary voltage	1.71V	3.465V
V <sub>EFUSE</sub> <sup>(2)</sup>	Voltage required for eFuse writing	1.62V	1.98V
<b>Gigabit Transceiver</b>			
V <sub>DDHAQ</sub> <sup>(2)</sup>	Analog high power supply voltage	1.71V	1.89V
V <sub>DDAQ</sub> <sup>(2)</sup>	Analog core power supply voltage	0.87V	1.03V
V <sub>DDTQ</sub> <sup>(2)</sup>	TX power supply voltage	0.87V	1.03V
V <sub>DDQ</sub> <sup>(2)</sup>	Digital power supply voltage	0.87V	1.03V
<b>MIPI</b>			
V <sub>DDAM</sub>	Analog core power supply voltage	0.87V	1.08V
V <sub>DDVM</sub>	Analog auxiliary power supply voltage	1.71V	3.465V
V <sub>DDDM</sub>	Digital power supply voltage	0.87V	1.08V
V <sub>DD12M</sub>	MIPI LP power supply voltage	1.14V	1.32V
<b>ADC</b>			
V <sub>CCADC</sub>	ADC power supply voltage	1.62V	1.98V
V <sub>REFN</sub>	ADC reference voltage	0V	0V
V <sub>REFP</sub>	ADC reference voltage	0V	1.25V
Note!			
<sup>(1)</sup> When internal differential termination resistors are required, Vccx must be greater than or equal to 3V; the IO input-output Fmax is limited when Vccx=1.8V, and Vccx needs to be greater than or equal to 2.5V for input-output applications with Fmax greater than 600Mbps.			
<sup>(2)</sup> When V <sub>DDQ</sub> is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			



Notes:

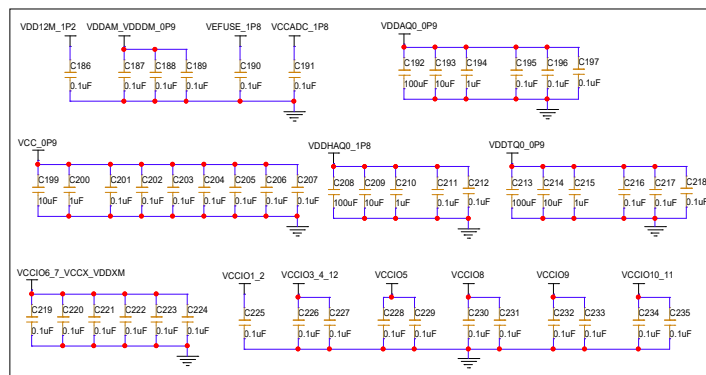
- 1.F CLK signal is an external input clock signal.
- It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.

***GW5AT-LV60UG225H***



Name	Description	Min.	Max.
<b>FPGA Logic</b>			
V <sub>CC</sub>	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V <sub>CCIO</sub>	I/O Bank voltage	1V	3.465V
V <sub>CC1</sub> <sup>(1)</sup>	Auxiliary voltage	1.71V	3.465V
V <sub>REFUSE</sub> <sup>(2)</sup>	Voltage required for eFUSE writing	1.62V	1.98V
<b>Gigabit Transceiver</b>			
V <sub>DDHAG+</sub>	Analog high power supply voltage	1.71V	1.89V
V <sub>DDAG+</sub>	Analog core power supply voltage	0.87V	1.03V
V <sub>DDTQ+</sub>	TX power supply voltage	0.87V	1.03V
V <sub>DDO+</sub>	Digital power supply voltage	0.87V	1.03V
<b>MIPI</b>			
V <sub>CCAM</sub>	Analog core power supply voltage	0.87V	1.08V
V <sub>CCOM</sub>	Analog auxiliary power supply voltage	1.71V	3.465V
V <sub>DDOM</sub>	Digital power supply voltage	0.87V	1.08V
V <sub>CCPLLMI</sub>	MIPI LP power supply voltage	1.14V	1.32V
<b>ADC</b>			
V <sub>CCADC</sub>	ADC power supply voltage	1.62V	1.98V
V <sub>REFIN</sub>	ADC reference voltage	0V	0V
V <sub>REFP</sub>	ADC reference voltage	0V	1.25V

<sup>[2]</sup> When internal differential termination resistors are required, Vccx must be greater than or equal to 3V; the IO input-output Fmax is limited when Vcccx=1.8V, and Vccx needs to be greater than or equal to 2.5V for input-output applications with Fmax greater than 600Mbps.

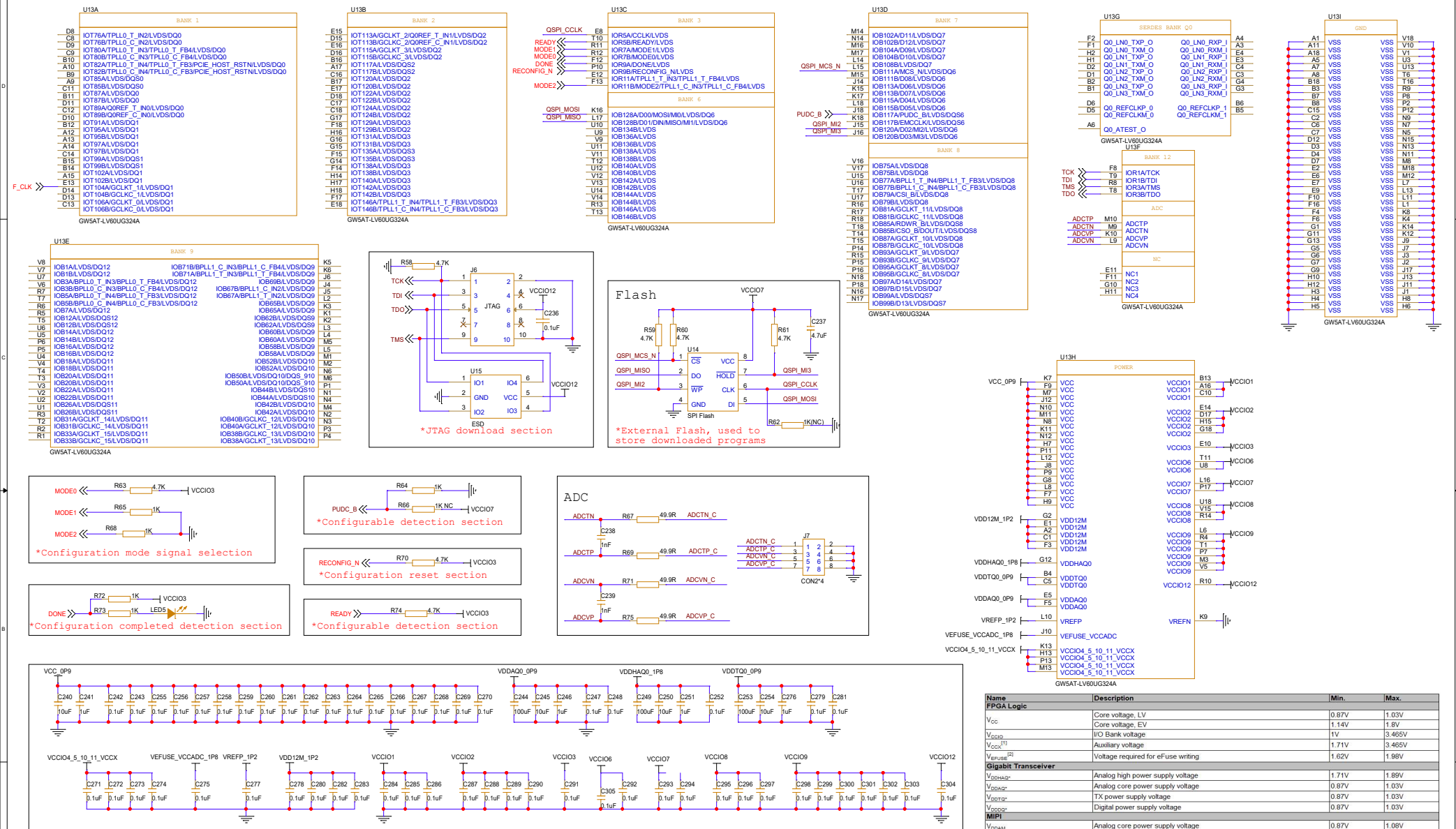


Notes:

1. F.CLK signal is an external input clock signal.
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3. External Flash memory is used to store downloaded programs.
4. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.
5. It is recommended that add an ESD protection chip to the JTAG download circuit.
6. VCC core voltage requires a large current, so it is recommended to supply power separately.
7. The MODE pin is the GowinCONFIG configuration mode selection signal.
8. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.



***GW5AT-LV60UG324A***



Notes:

1.F CLK signal is an external input clock signal.

It is recommended that F CLK signal be provided through an active oscillator crystal.

2. External Flash memory is used to store downloaded programs.

For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718,

Arora V 60K FPGA Products Programming and Configuration Guide .

3. It is recommended that add an ESD protection chip to the JTAG download circuit.

4.VCC core voltage requires a large current, so it is recommended to s

5.The MODE pin is the GowinCONFIG configuration mode selection signal.

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For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.

[2] When internal differential termination resistors are required, Vccx must be greater than or equal to 3V; the IO input-output Fmax is limited when Vccx=1.8V.

and Vccx needs to be greater than or equal to 2.5V for input-output applications with Fmax greater than 600Mbps.

[2] When V<sub>EFUSE</sub> is not required, this power supply can be connected to either GND or floating. If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the

If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.

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[illegible]

	Title
	GOWIN M