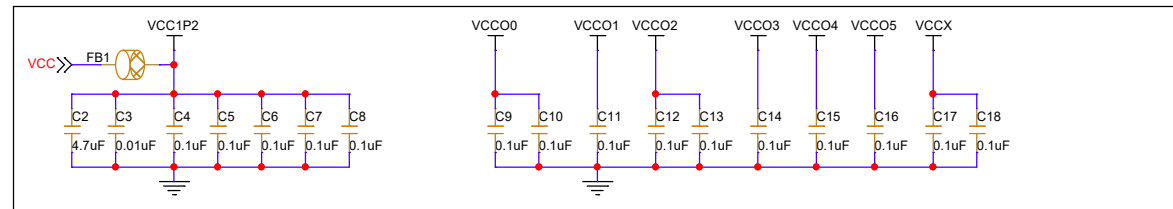
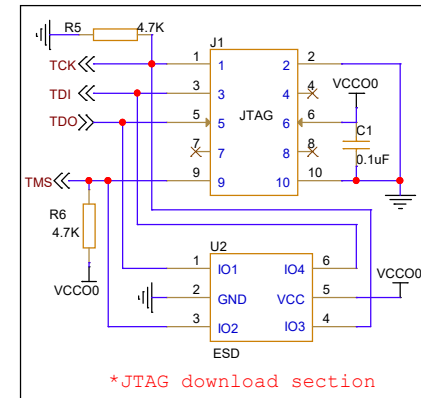
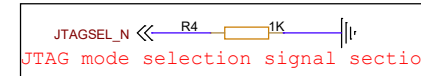
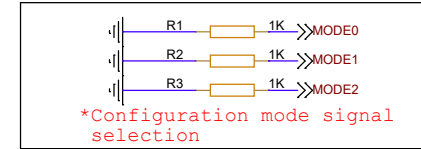
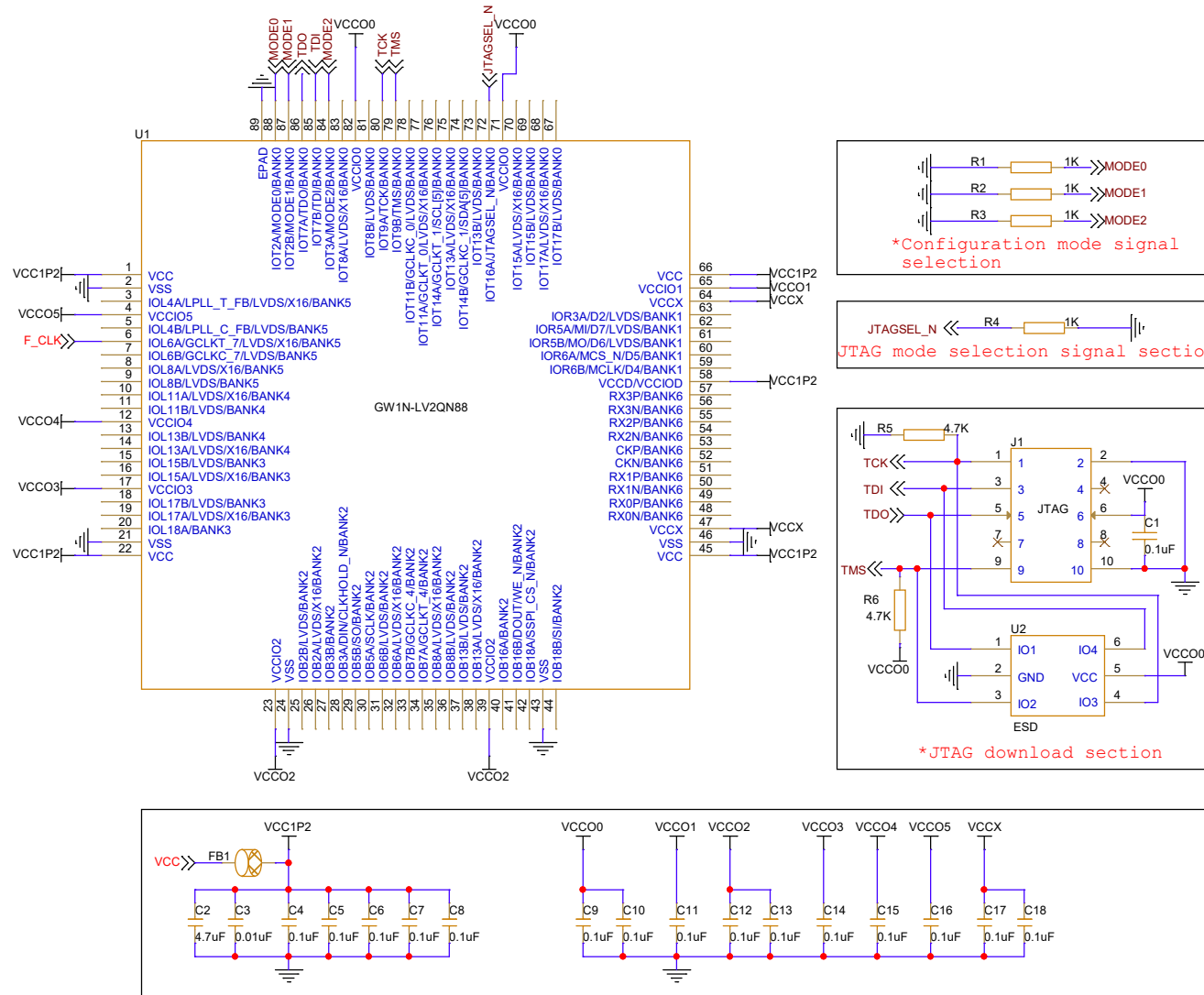


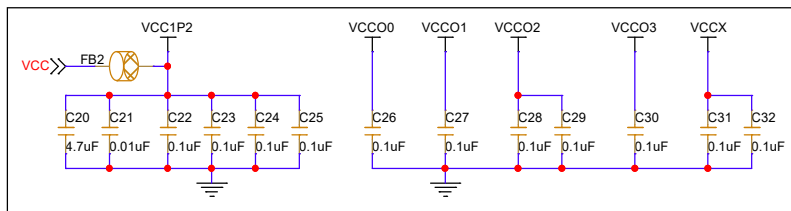
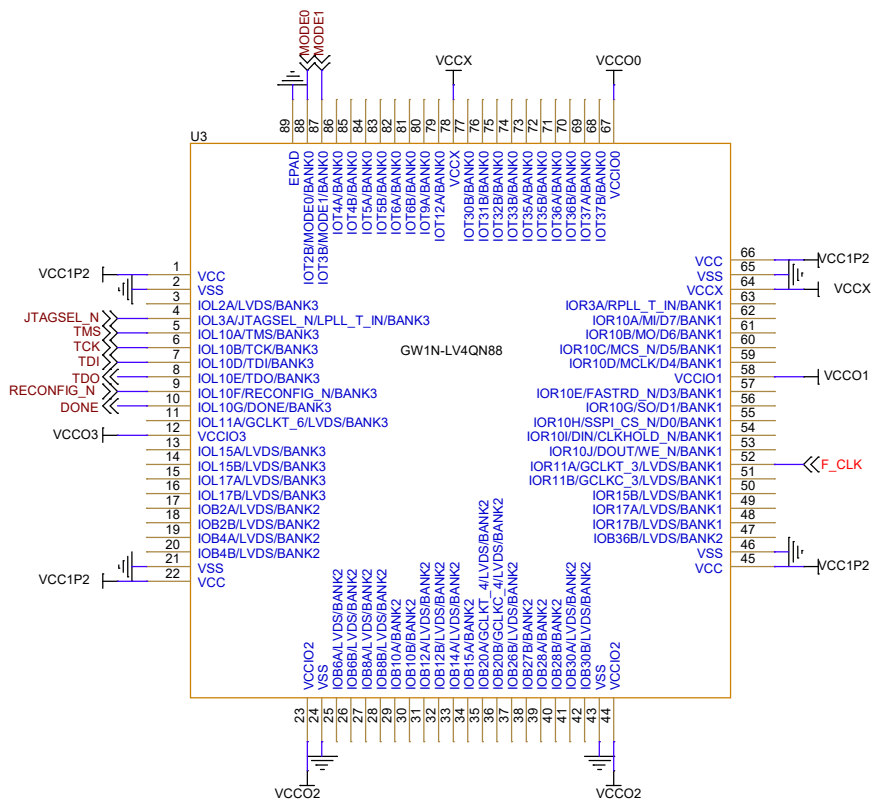
GW1N-LV2QN88



- Notes:
- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

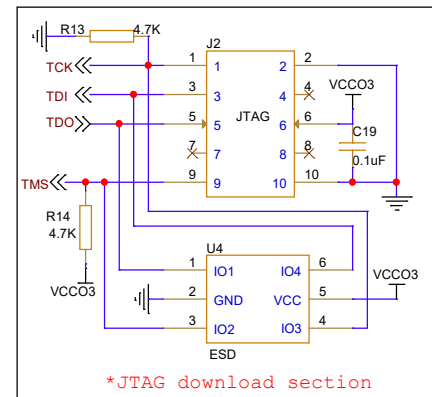
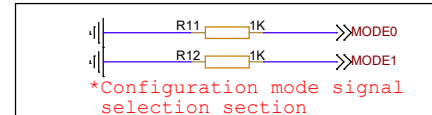
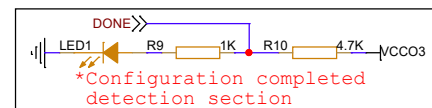
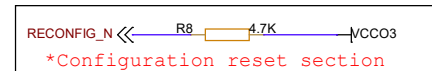
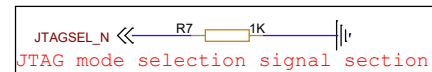
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GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-LV2QN88	3.4
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GW1N-LV4QN88



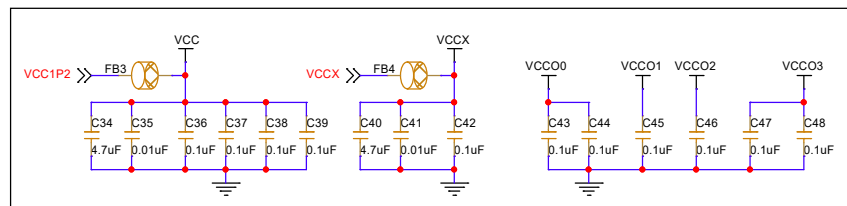
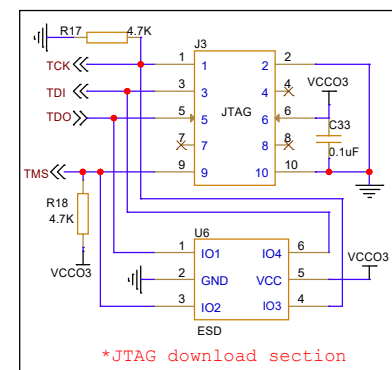
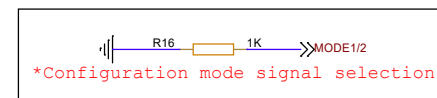
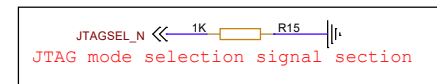
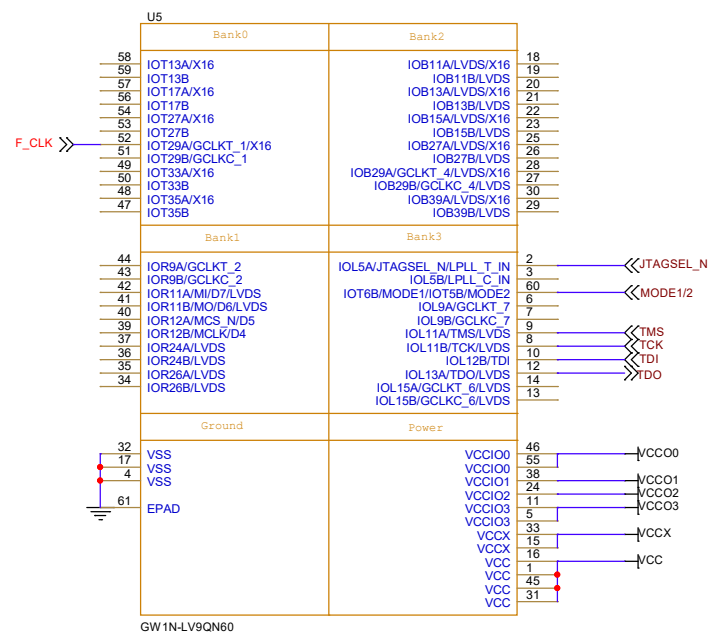
Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



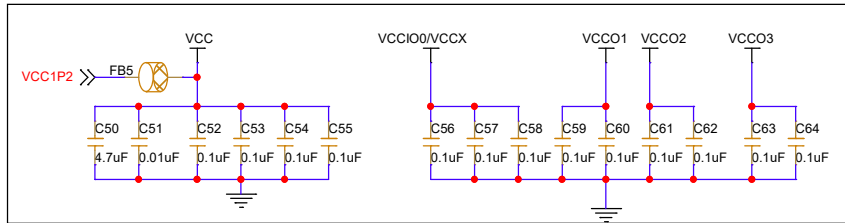
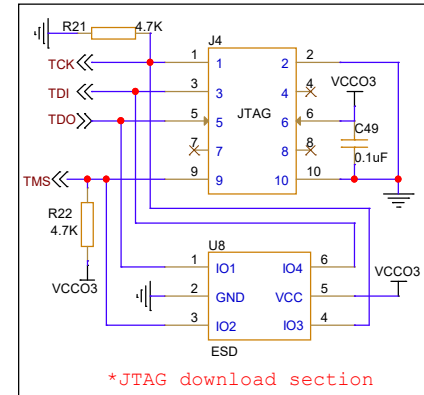
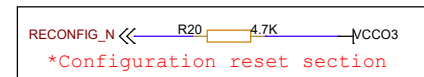
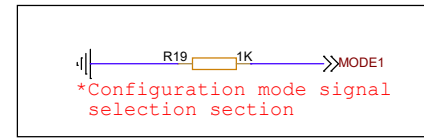
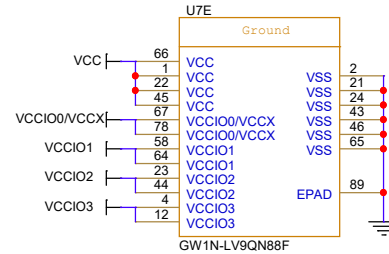
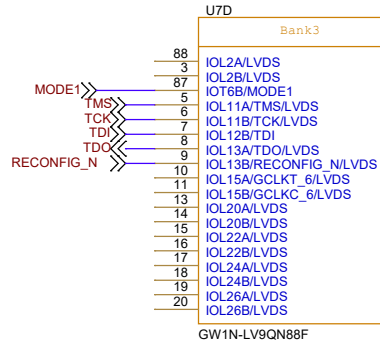
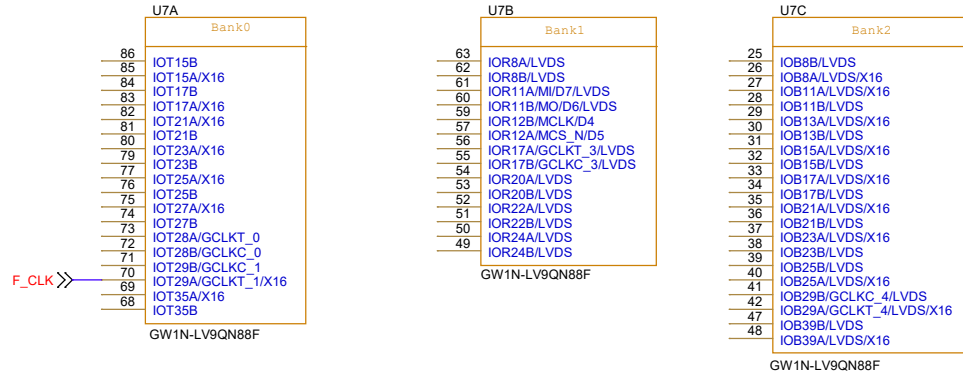
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Gowin FPGA-AOTOMOTIVE Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-LV4QN88	3.4
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GW1N-LV9QN60



- Notes:
- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
 - 3.It is recommended that add an ESD protection chip to the JTAG download circuit.

GW1N-LV9QN88F

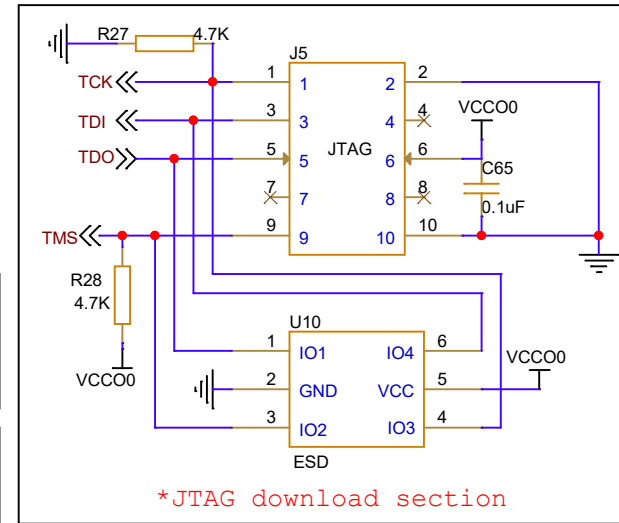
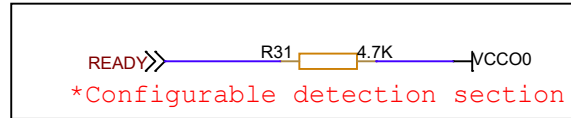
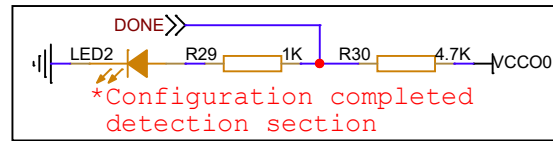
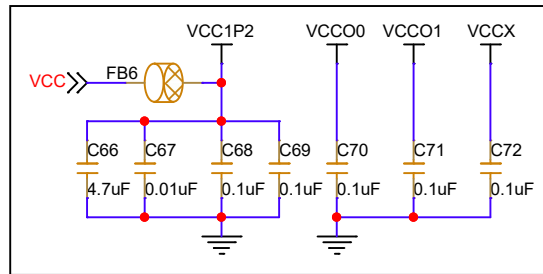
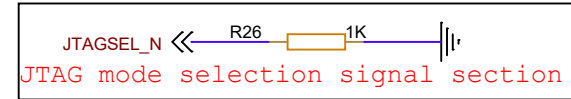
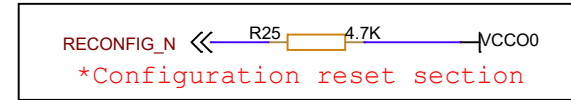
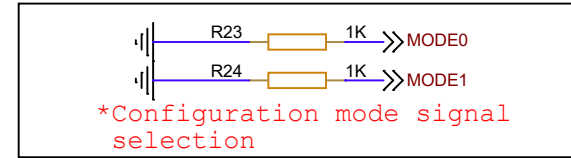
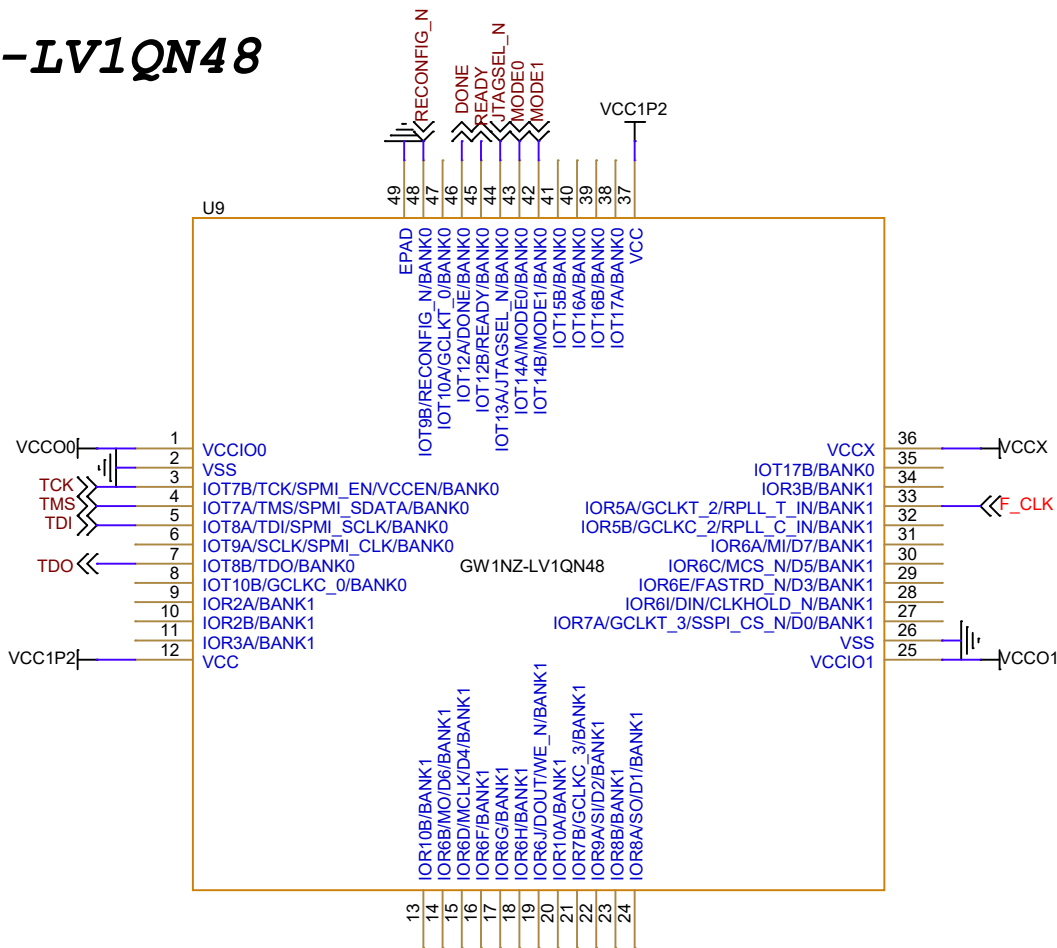


Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
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B	GW1N-LV9QN88F	3.4
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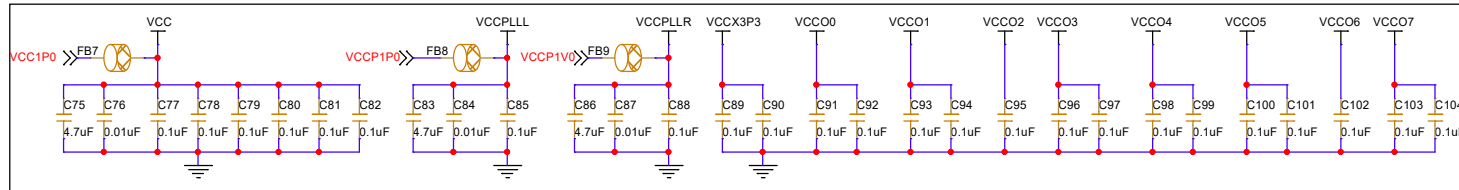
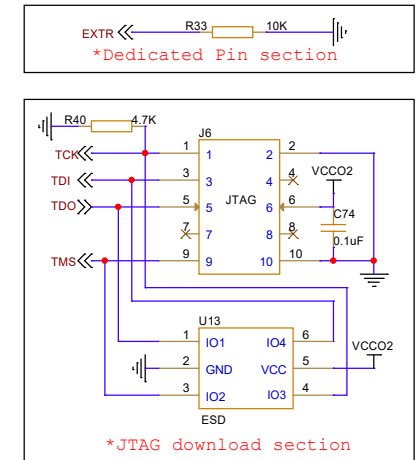
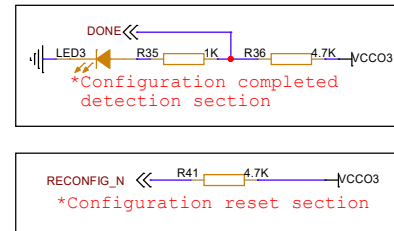
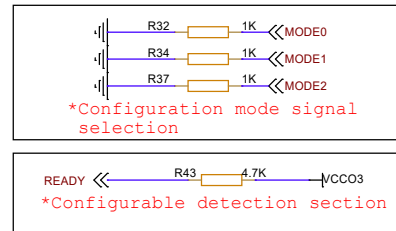
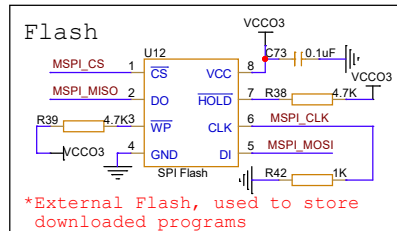
GW1NZ-LV1QN48



- Notes:
1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title			
Gowin FPGA-AOTOMOTIVE Minimum System Diagram			
Size	Document Number		Rev
A4	GW1NZ-LV1QN48		3.4
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GW2A-LV18PG256

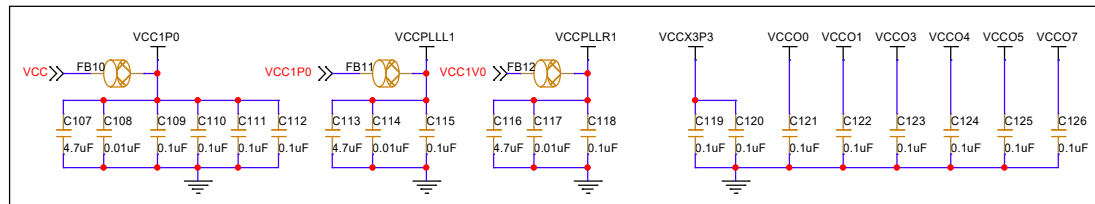
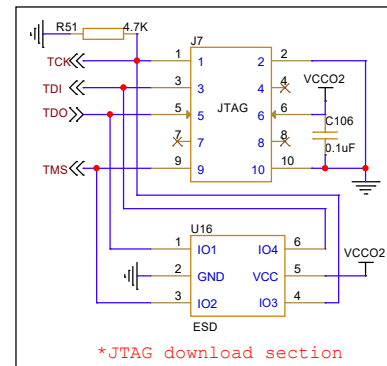
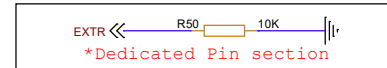
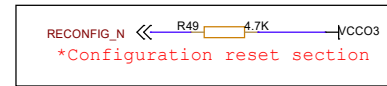
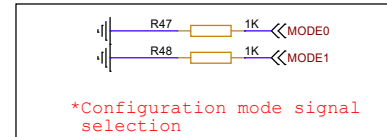
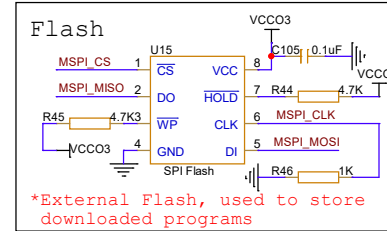
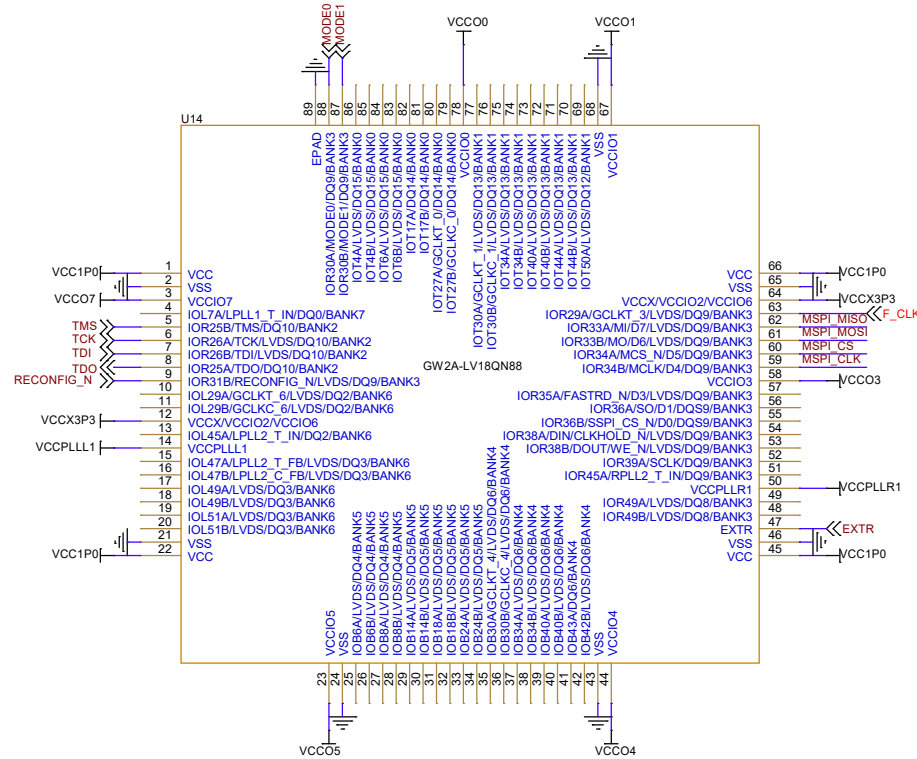


Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.

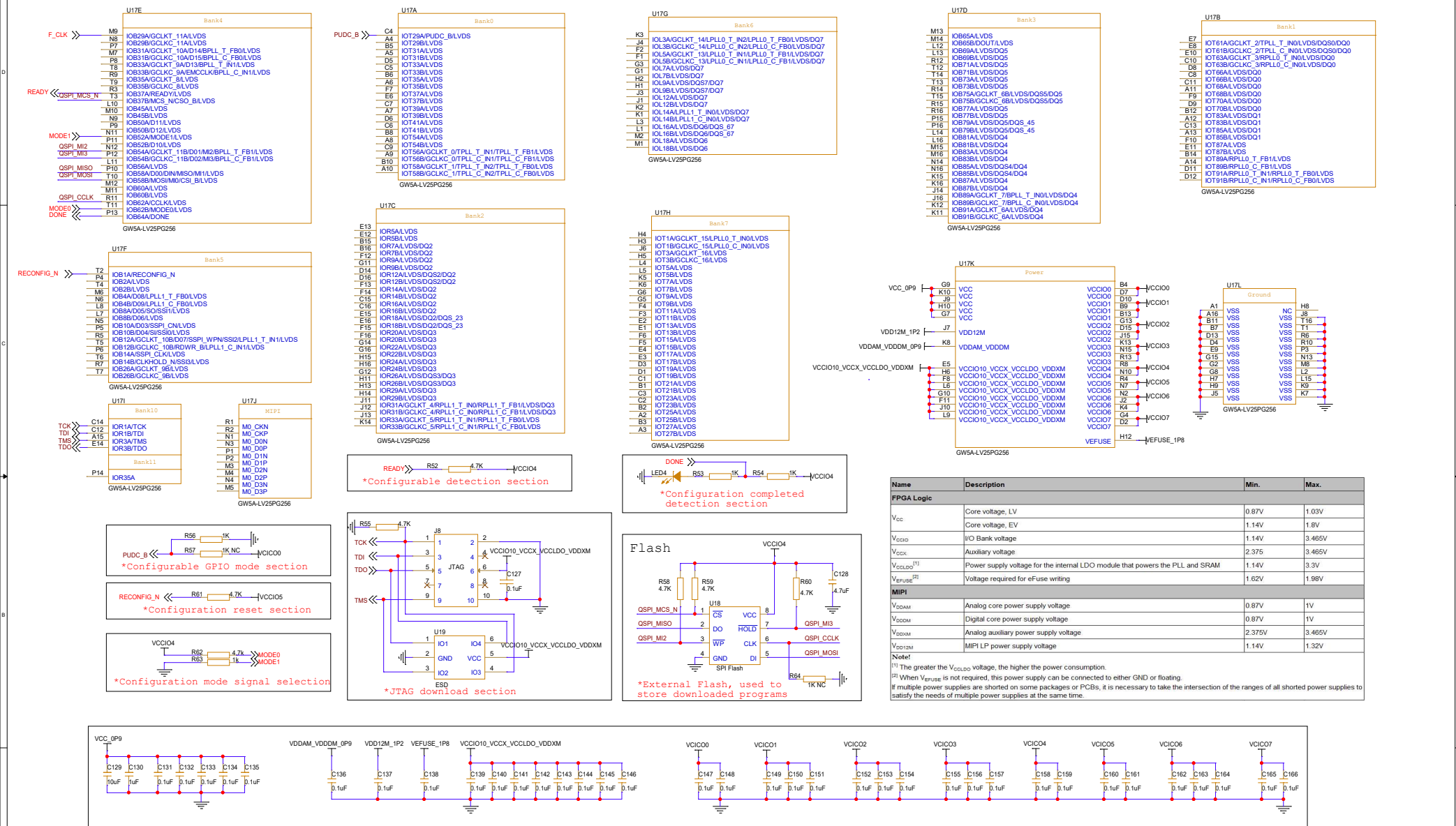
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Size	Document Number	Rev
A3	GW2A-LV18PG256	3.4
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GW2A-LV18QN88



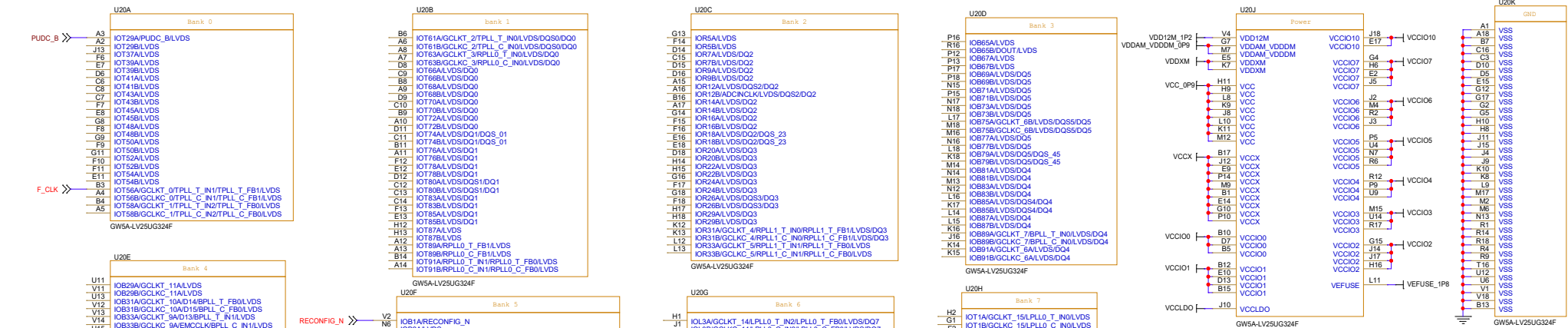
- Notes:
- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
 - 3.It is recommended that add an ESD protection chip to the JTAG download circuit.

GW5A-LV25PG256

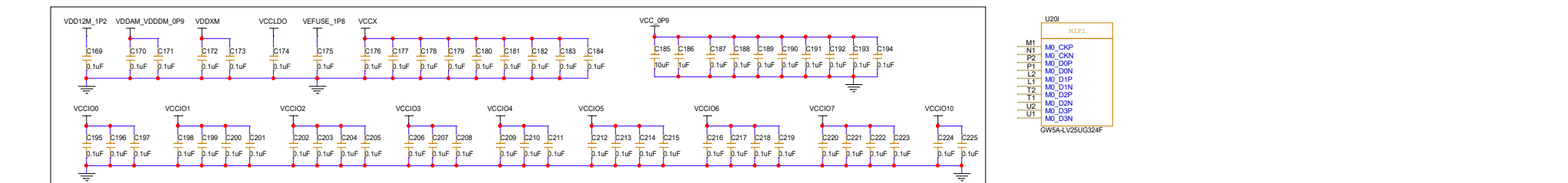
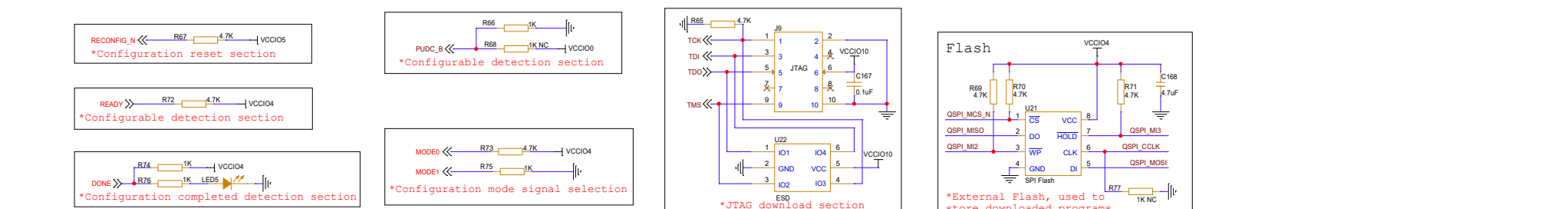


Title			
GOWIN Minimum System Diagram			
Size	Document Number	Rev	
C	GW5A-LV25PG256	3.4	
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GW5A-LV25UG324F



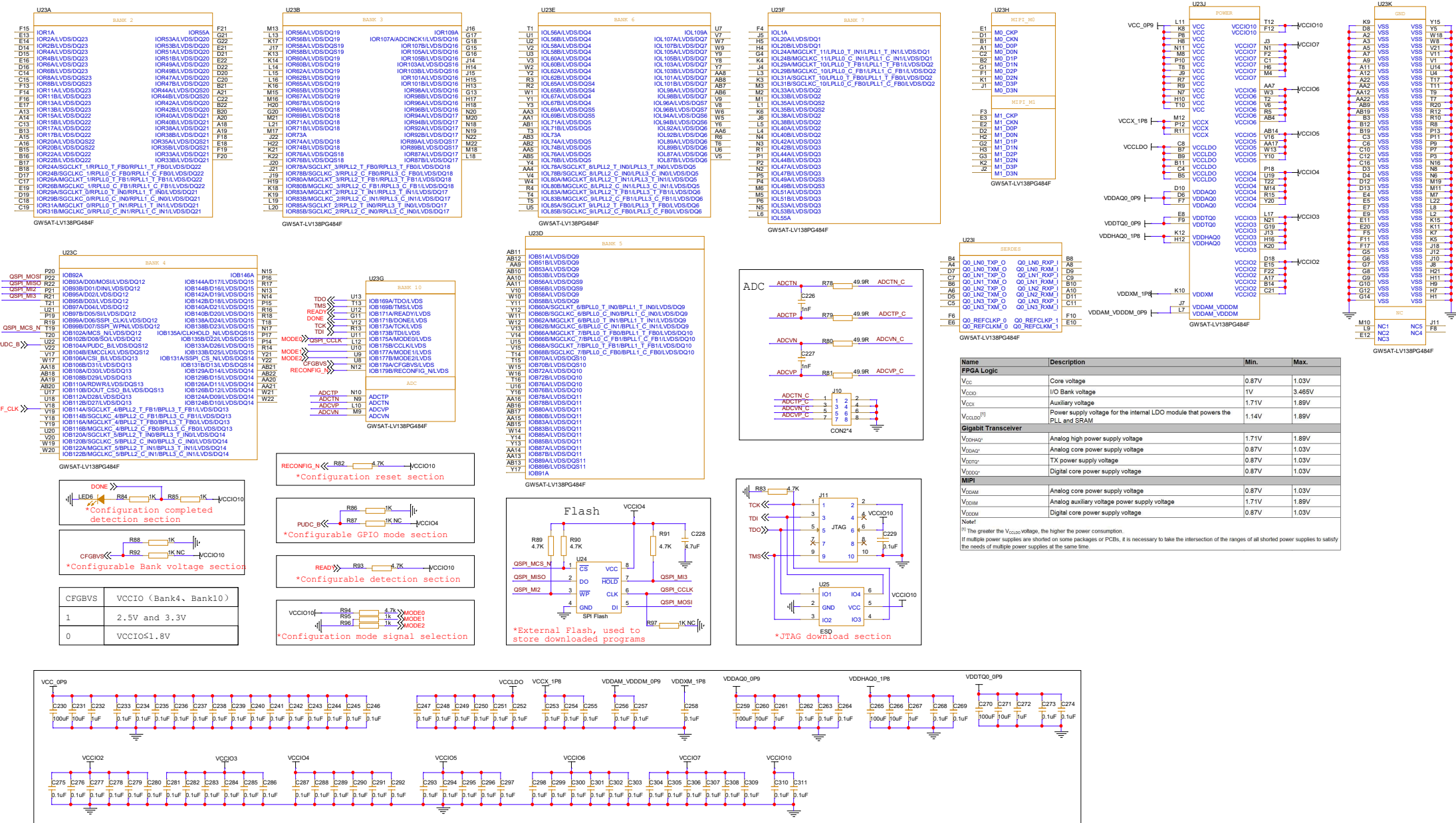
Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
V _{CC}	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCIO}	Auxiliary voltage	2.375V	3.465V
V _{CCIO} ^[1]	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{FUSE} ^[2]	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V _{DDAM}	Analog core power supply voltage	0.87V	1V
V _{DDCM}	Digital core power supply voltage	0.87V	1V
V _{DDCM}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{DDIO}	MIPI LP power supply voltage	1.14V	1.32V
Notes			
[1] The greater the V _{CCIO} voltage, the higher the power consumption.			
[2] When V _{FUSE} is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			



Notes:

- 1.F_CLK signal is an external input clock signal.
- It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.

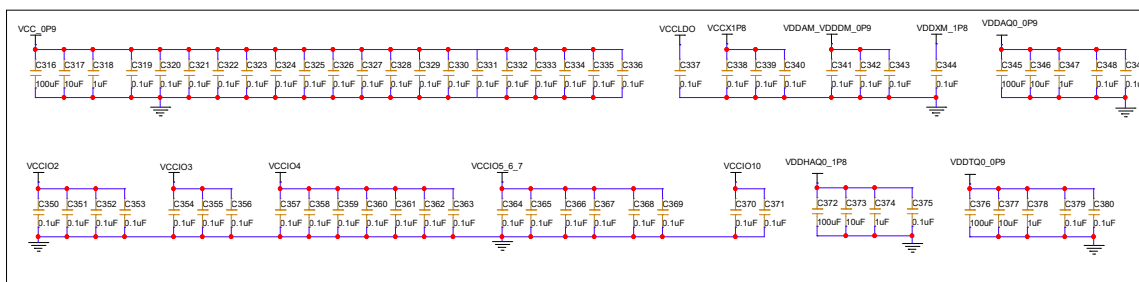
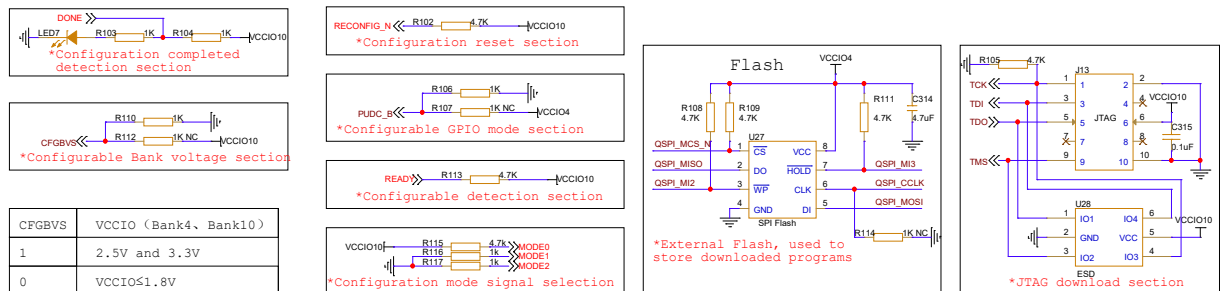
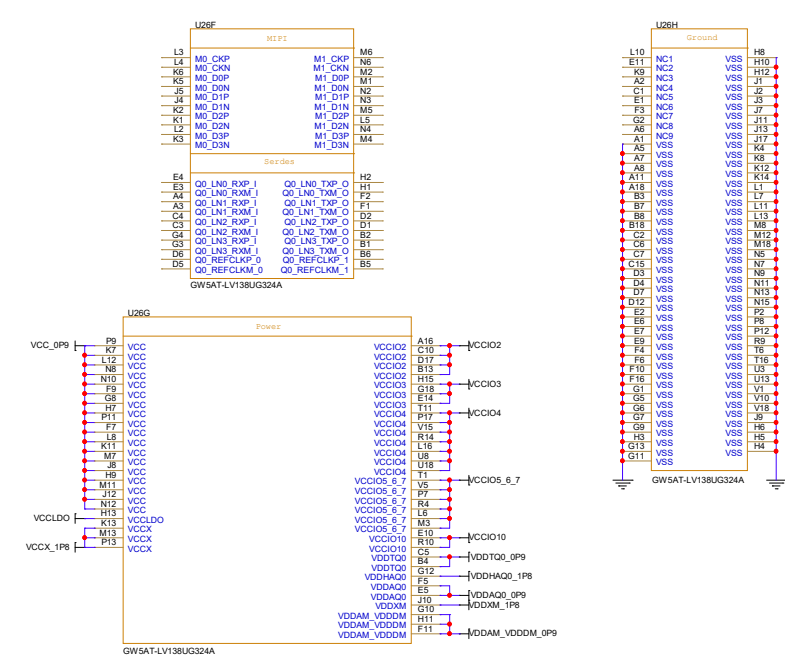
GW5AT-LV138PG484F



Notes:

- 1.F CLK signal is an external input clock signal.
- It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
- For details about SPI Flash memory selection, see "Chapter 4.5 SPI Flash Selection" in UG704, Arora V FPGA Products Programming and Configuration Guide.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, Arora V FPGA Products Programming and Configuration Guide.

GW5AT-LV138UG324A

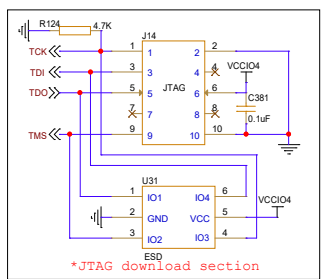
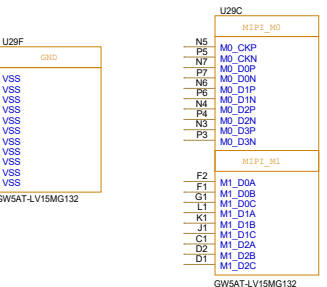
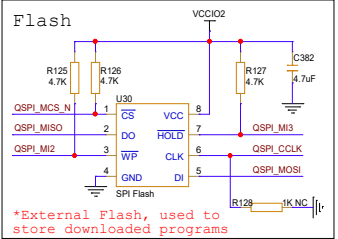
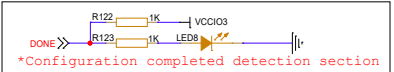
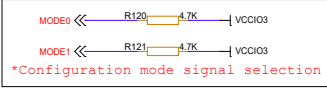
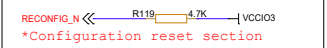
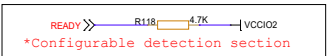
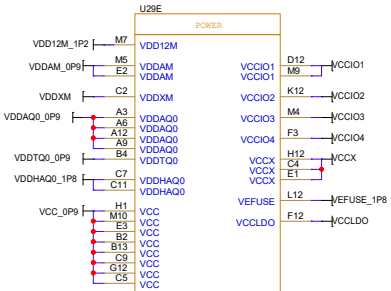
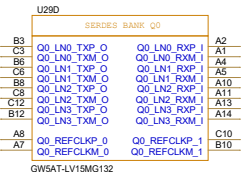
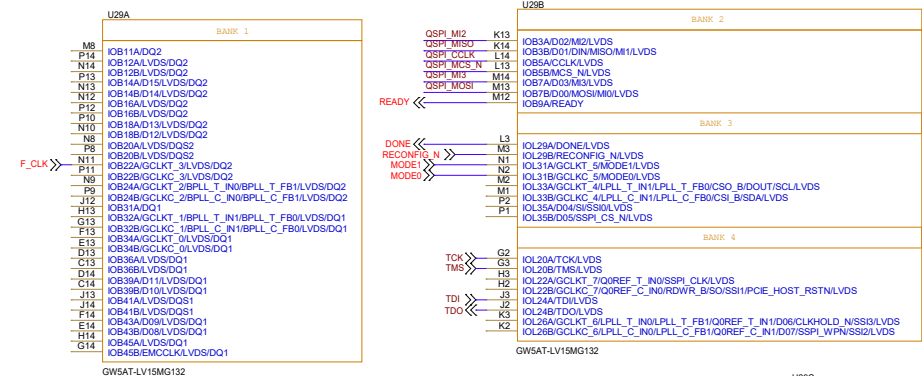


Notes:

1. F_CLK signal is an external input clock signal. It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs. For details about SPI Flash mode selection, see "Chapter 4.5 SPI Flash Selection" in UG704, *Arora V₂ FPGA Products Programming and Configuration Guide*.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. The core voltage requires a large current, so it is recommended to supply power separately.
5. The MODE pin is the GowinCONFIG configuration mode selection signal. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, *Arora V₂ FPGA Products Programming and Configuration Guide*.

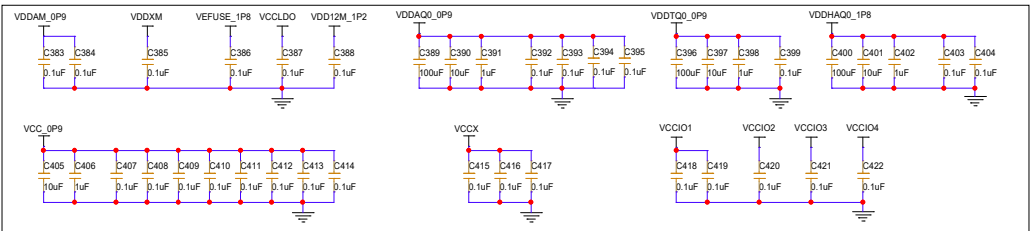
Name	Description	Min.	Max.
FPGA Logic			
V _{DD}	Core voltage	0.87V	1.03V
V _{CCIO}	I/O Bank voltage	1V	3.465V
V _{CCX}	Auxiliary voltage	1.71V	1.89V
V _{CCDDO} ^[1]	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	1.89V
Gigabit Transceiver			
V _{DDH242}	Analog high power supply voltage	1.71V	1.89V
V _{DDH242}	Analog core power supply voltage	0.87V	1.03V
V _{DDT242}	TX power supply voltage	0.87V	1.03V
V _{DDO242}	Digital core power supply voltage	0.87V	1.03V
MIPI			
V _{DDI0M}	Analog core power supply voltage	0.87V	1.03V
V _{DDI0M}	Analog auxiliary voltage power supply voltage	1.71V	1.89V
V _{DDI0M}	Digital core power supply voltage	0.87V	1.03V
Note!			
^[1] The greater the V _{CCDDO} voltage, the higher the power consumption.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			

GW5AT-LV15MG132



Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCX} ^[1]	Auxiliary voltage	1.71V	3.465V
V _{CCDDO}	SRAM and PLL Regulator voltage	1.14V	2.75V
V _{EFUSE} ^[2]	Voltage required for eFuse writing	1.62V	1.98V
Gigabit Transceiver			
V _{DDHAQ} *	Analog high power supply voltage	1.71V	1.89V
V _{DDAQ} *	Analog core power supply voltage	0.87V	1.03V
V _{DDTQ} *	Serdes transmitter power supply voltage	0.87V	1.03V
MIPI			
V _{DDAH}	Analog core power supply voltage	0.855V	1.08V
V _{DDXM}	Analog auxiliary voltage power supply voltage	1.71V	3.465V
V _{DDM}	Digital power supply voltage	0.87V	1.08V
V _{DD12M}	MIPI LP power supply voltage	1.14V	1.32V

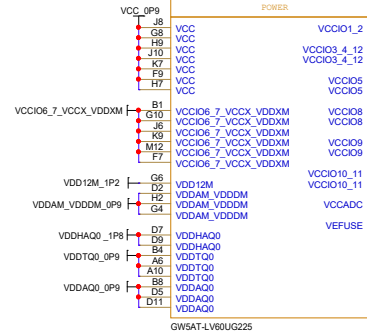
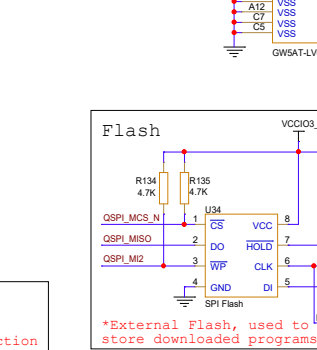
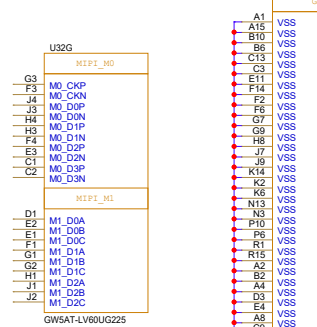
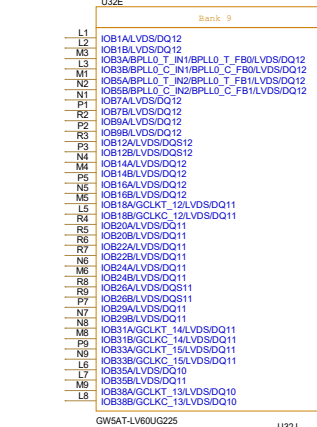
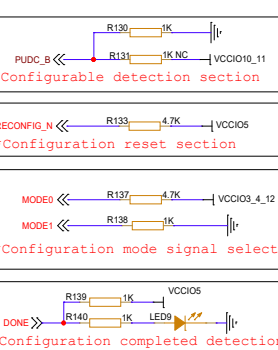
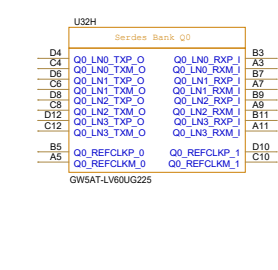
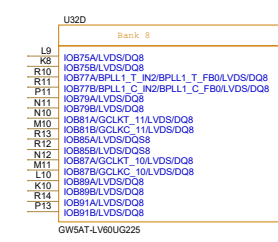
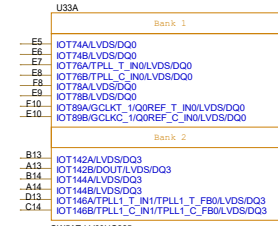
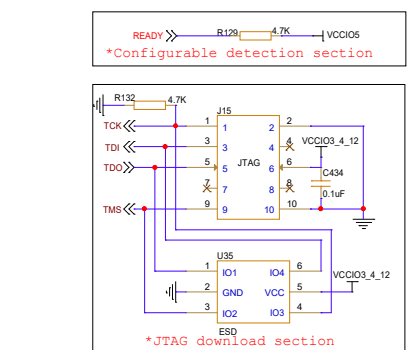
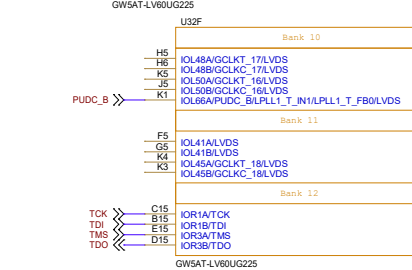
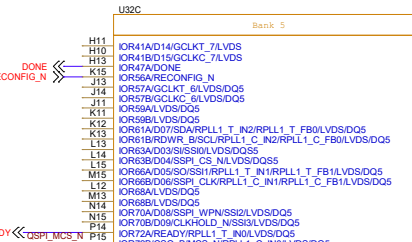
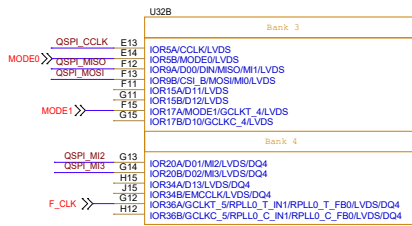
Note!
^[1] When internal differential termination resistors are required, V_{ccx} must be greater than or equal to 3V, the IO input-output F_{max} is limited when V_{ccx}=1.8V, and V_{ccx} needs to be greater than or equal to 2.5V for input-output applications with F_{max} greater than 600Mbps.
^[2] When V_{EFUSE} is not required, this power supply can be connected to either GND or floating.
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.



Notes:
1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG720, Arora V 15K FPGA Products Programming and Configuration Guide .
3.It is recommended that add an ESD protection chip to the JTAG download circuit.
4.VCC core voltage requires a large current, so it is recommended to supply power separately.
5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG720, Arora V 15K FPGA Products Programming and Configuration Guide.

Title			
GOWIN Minimum System Diagram			
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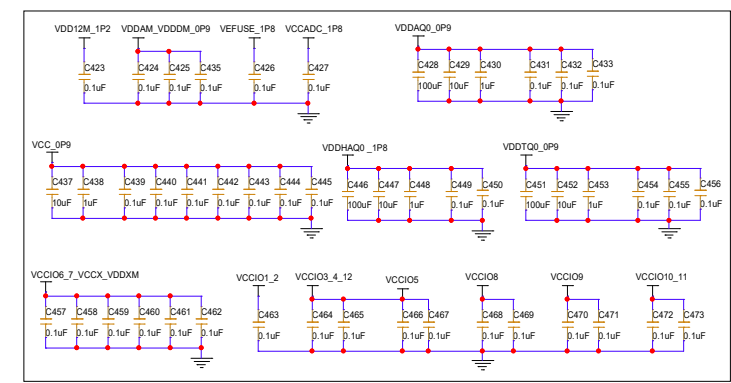
Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
V _{CCIO}	Core voltage, EV	1.14V	1.8V
V _{CCIO} ⁽¹⁾	I/O Bank voltage	1V	3.465V
V _{CCA} ⁽¹⁾	Auxiliary voltage	1.71V	3.465V
V _{EPUF} ⁽²⁾	Voltage required for eFUSE writing	1.62V	1.98V
Gigabit Transceiver			
V _{SDHAW2} ⁽³⁾	Analog high power supply voltage	1.71V	1.89V
V _{SDHAW1} ⁽³⁾	Analog core power supply voltage	0.87V	1.03V
V _{SDHIO2} ⁽³⁾	TX power supply voltage	0.87V	1.03V
V _{SDHIO1} ⁽³⁾	Digital power supply voltage	0.87V	1.03V
MIPI			
V _{DDMI1}	Analog core power supply voltage	0.87V	1.08V
V _{DDMI2}	Analog auxiliary power supply voltage	1.71V	3.465V
V _{DDMI3}	Digital power supply voltage	0.87V	1.08V
V _{DDI2M}	MIPI LP power supply voltage	1.14V	1.32V
ADC			
V _{CCADC}	ADC power supply voltage	1.62V	1.98V
V _{REFN}	ADC reference voltage	0V	0V
V _{REFP}	ADC reference voltage	0V	1.25V

Note!

[1] When internal differential termination resistors are required, V_{CCX} must be greater than or equal to 3V; the IO input-output F_{max} is limited when $V_{CCX}=1.8V$, and V_{CCX} needs to be greater than or equal to 2.5V for input-output applications with F_{max} greater than 600Mbps.

[2] When $VFUSE$ is not required, this power supply can be connected to either GND or floating.

If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.



Notes:

- 1.F CLK signal is an external input clock signal.
- 2.If it is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.

For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide .

- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.

For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.