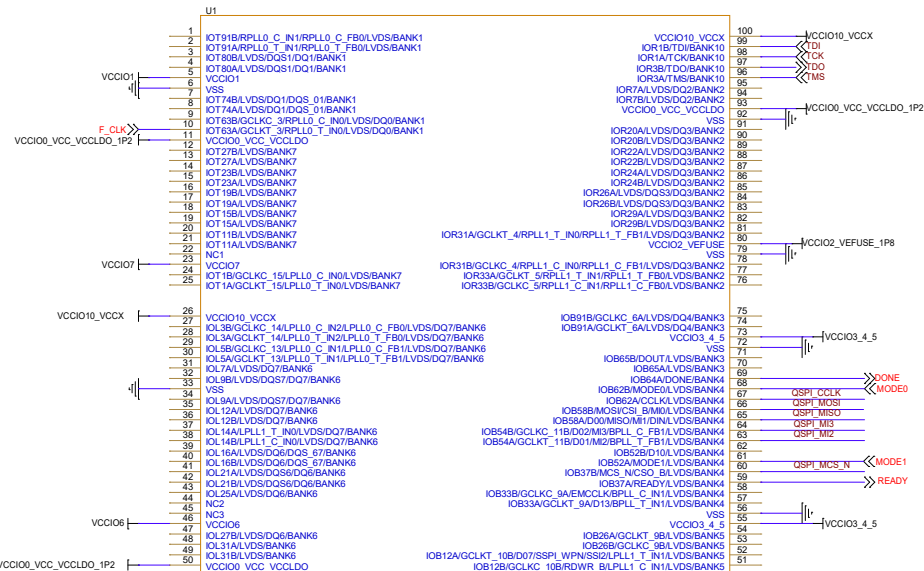
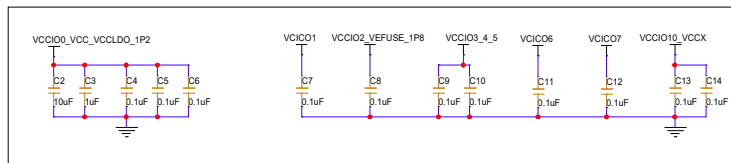


GW5A-EV25LQ100



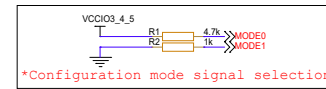
GW5A-EV25LQ100



Name	Description	Min.	Max.
PPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCIL}	Auxiliary voltage	2.375	3.465V
V _{CCDDO} ^[1]	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	1.3V
V _{EFUSE} ^[2]	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V _{DDAM}	Analog core power supply voltage	0.87V	1V
V _{DDDM}	Digital core power supply voltage	0.87V	1V
V _{DDIM}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{DD12M}	MIPI LP power supply voltage	1.14V	1.32V
Note:			
^[1] The greater the V _{CCDDO} voltage, the higher the power consumption.			
^[2] When V _{EFUSE} is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to ensure the correct voltage.			

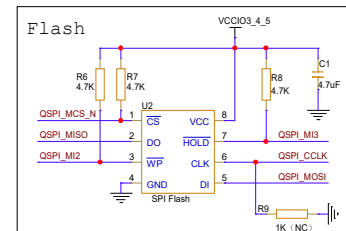
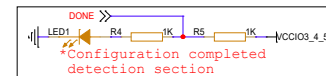
Notes:

1. F CLK signal is an external input clock signal.
- It is recommended that F CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. VCC core voltage requires a large current, so it is recommended to supply power separately.
5. The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.

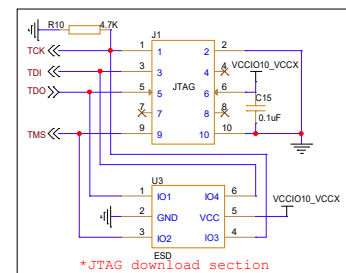


READY >>> R3 4.7K VCCIO3_4_5

*Configurable detection section

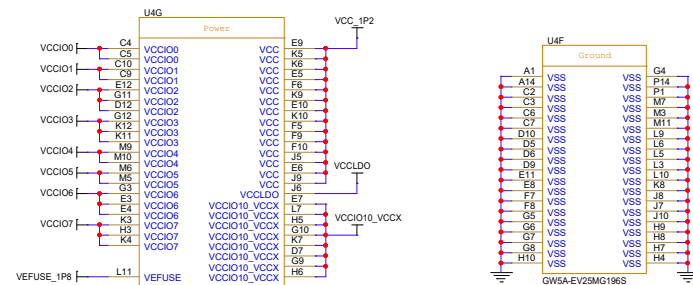
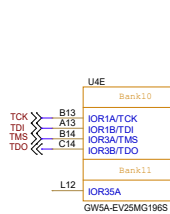
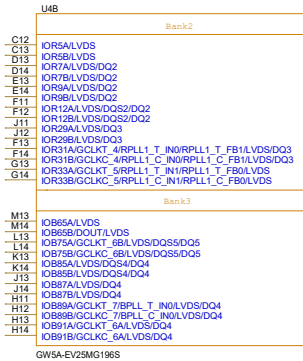


*External Flash, used to store downloaded programs



*JTAG download section

GW5A-EV25MG196S

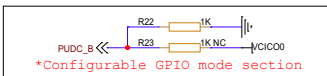
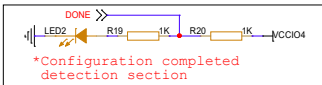
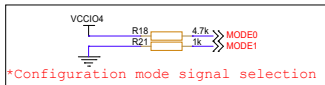
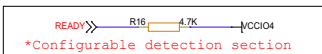
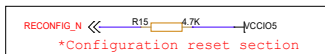
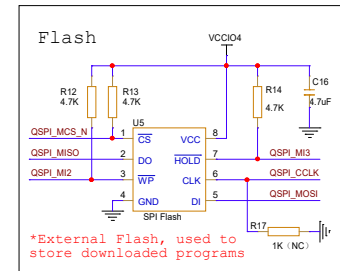
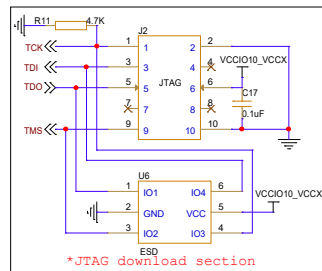


Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
V _{CCIO}	Core voltage, EV	1.14V	1.8V
V _{CCIOQ}	I/O Bank voltage	1.14V	3.465V
V _{CCX}	Auxiliary voltage	2.375	3.465V
V _{CCDDO} ^[1]	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{EFUSE} ^[2]	Voltage required for eFuse writing	1.62V	1.98V
MIP1			
V _{DDAM}	Analog core power supply voltage	0.87V	1V
V _{DDCM}	Digital core power supply voltage	0.87V	1V
V _{DDIM}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{DD12M}	MIP1 LP power supply voltage	1.14V	1.32V

^[1] The greater the V_{GCLDO} voltage, the higher the power consumption.

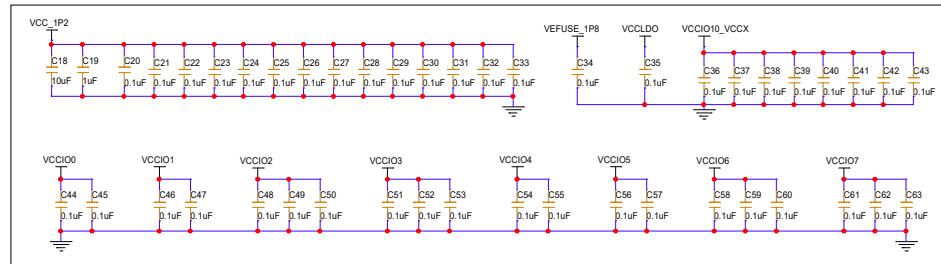
^[2] When V_{EFUSE} is not required, this power supply can be connected to either GND or floating

If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.

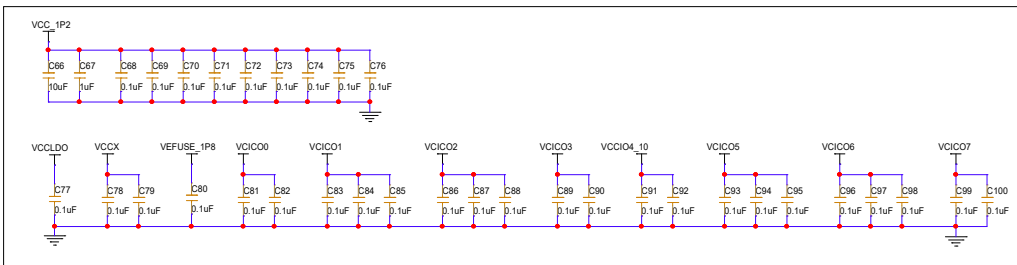
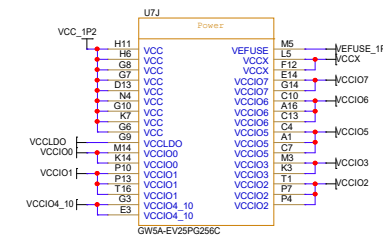
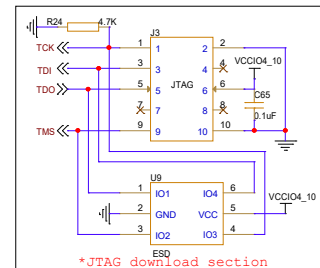
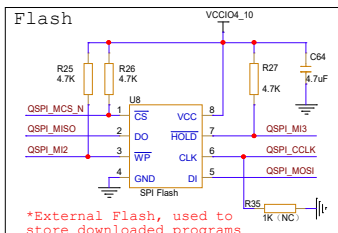
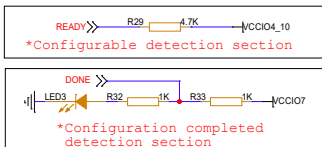
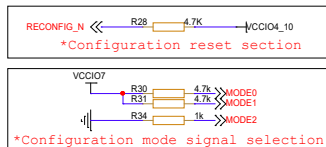
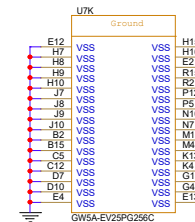
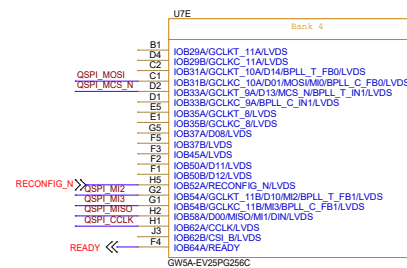
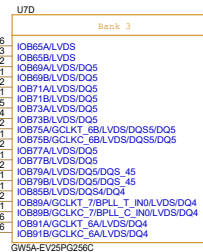
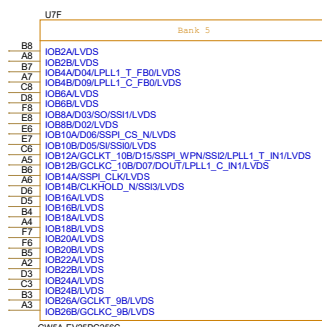
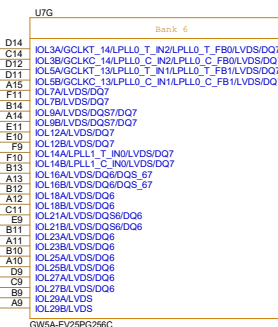
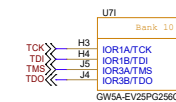
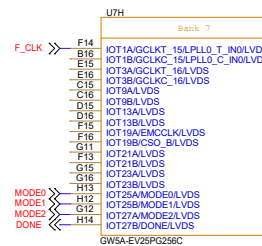
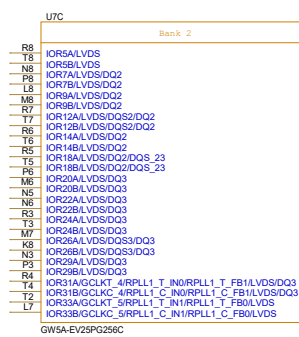
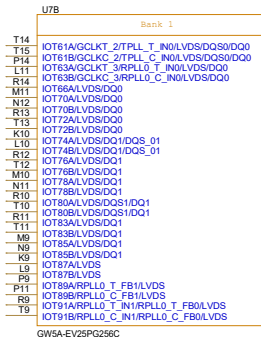
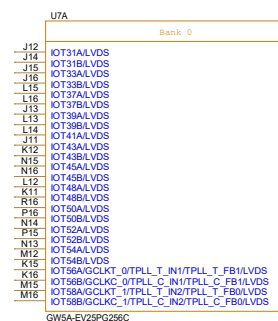


Notes:

- 1.F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.



GW5A-EV25PG256C



Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCIO}	Auxiliary voltage	2.375	3.465V
V _{CCOLD} ^[1]	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{EFUSE} ^[2]	Voltage required for eFuse writing	1.62V	1.98V
MIP1			
V _{DDMM}	Analog core power supply voltage	0.87V	1V
V _{DDOOM}	Digital core power supply voltage	0.87V	1V
V _{DDMM}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{DD12M}	MIP1 LP power supply voltage	1.14V	1.32V
Note!			
^[1] The greater the V _{CCOLD} voltage, the higher the power consumption.			
^[2] When V _{EFUSE} is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies as the range of the power supply voltage at the same time.			

Notes:

1.F CLK signal is an external input clock signal.

It is recommended that F CLK signal be provided through an active oscillator crystal.

2. External Flash memory is used to store downloaded programs.

For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714,

Arora V 25K FPGA Products Programming and Configuration Guide .

3. It is recommended that add an ESD protection chip to the JTAG download circuit.

4.VCC core voltage requires a large current, so it is recommended to supply power separately.

5. The MODE pin is the GowinCONFIG configuration mode selection signal.

For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714,

Arora V 25K FPGA Products Programming and Configuration Guide.

Model V Z8K ROM Products Programming and Configuration Guide.

GW5A-EV25PG256S

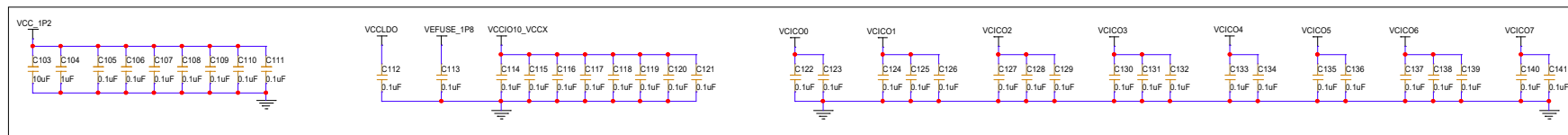


Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCUX}	Auxiliary voltage	2.375	3.465V
V _{CC_LDO} ⁽¹⁾	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{FUSE} ⁽²⁾	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V _{CCDAM}	Analog core power supply voltage	0.87V	1V
V _{CCDMM}	Digital core power supply voltage	0.87V	1V
V _{CCDMM}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{CC12M}	MIPI LP power supply voltage	1.14V	1.32V

^[1] The greater the V_{CCLO} voltage, the higher the power consumption.

[2] When V_{EFUSE} is not required, this power supply can be connected to either GND or floating

If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.



Notes:

1.F CLK signal is an external input clock signal.

It is recommended that F CLK signal be provided through an active oscillator crystal.

2. External Flash memory is used to store downloaded programs.

For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714.

For details about SPI flash model selection, see Chapter 4.3 of Arora V 25K FPGA Products Programming and Configuration Guide .

3. It is recommended that add an ESD protection chip to the JTAG download circuit.

4.VCC core voltage requires a large current, so it is recommended to s

5.The MODE pin is the GowinCONFIG configuration mode selection signal.

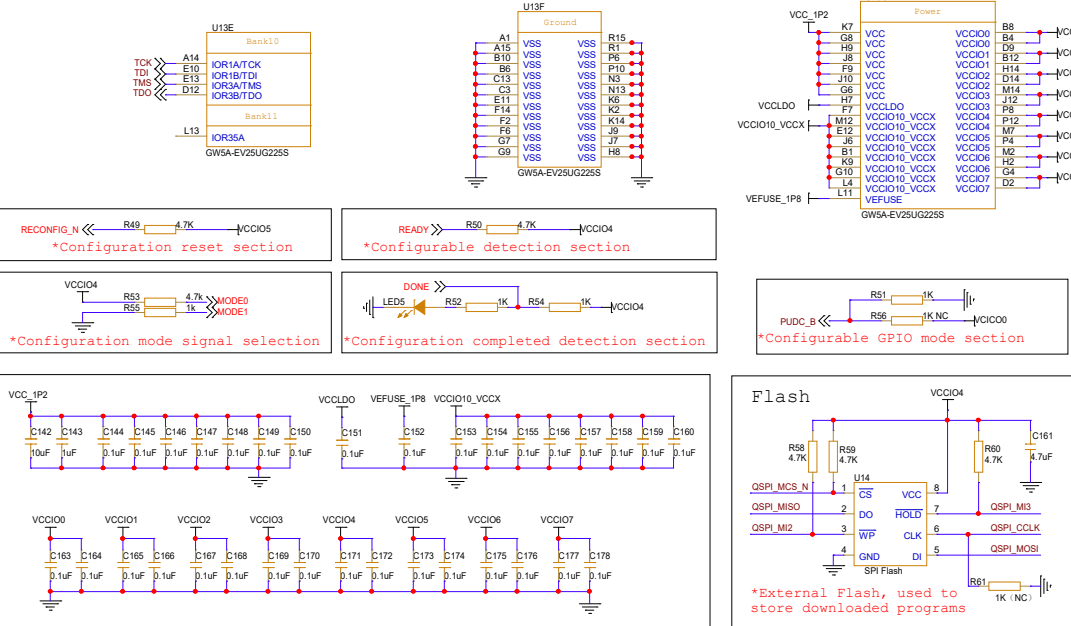
For details about how to select the Mode signal, see "Chapter 3.1 Conf

Arora V 25K FPGA Products Programming and Configuration Guide.

GW5A-EV25UG225S



Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCUX}	Auxiliary voltage	2.375	3.465V
V _{CCLOG} ^[1]	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{ERUSE} ^[2]	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V _{DDAM}	Analogue core power supply voltage	0.87V	1V
V _{DDDM}	Digital core power supply voltage	0.87V	1V
V _{DDOM}	Analogue auxiliary power supply voltage	2.375V	3.465V
V _{DD1.2M}	MIPI LP power supply voltage	1.14V	1.32V
Note ¹			
^[1] The greater the V _{CCLOG} voltage, the higher the power consumption. ^[2] When V _{ERUSE} is not required, this power supply can be connected to either GND or floating. If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			



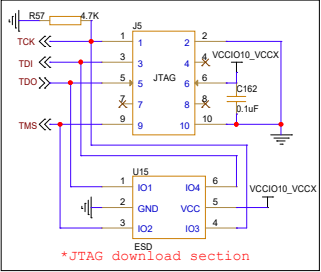
Notes:

- 1.F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.

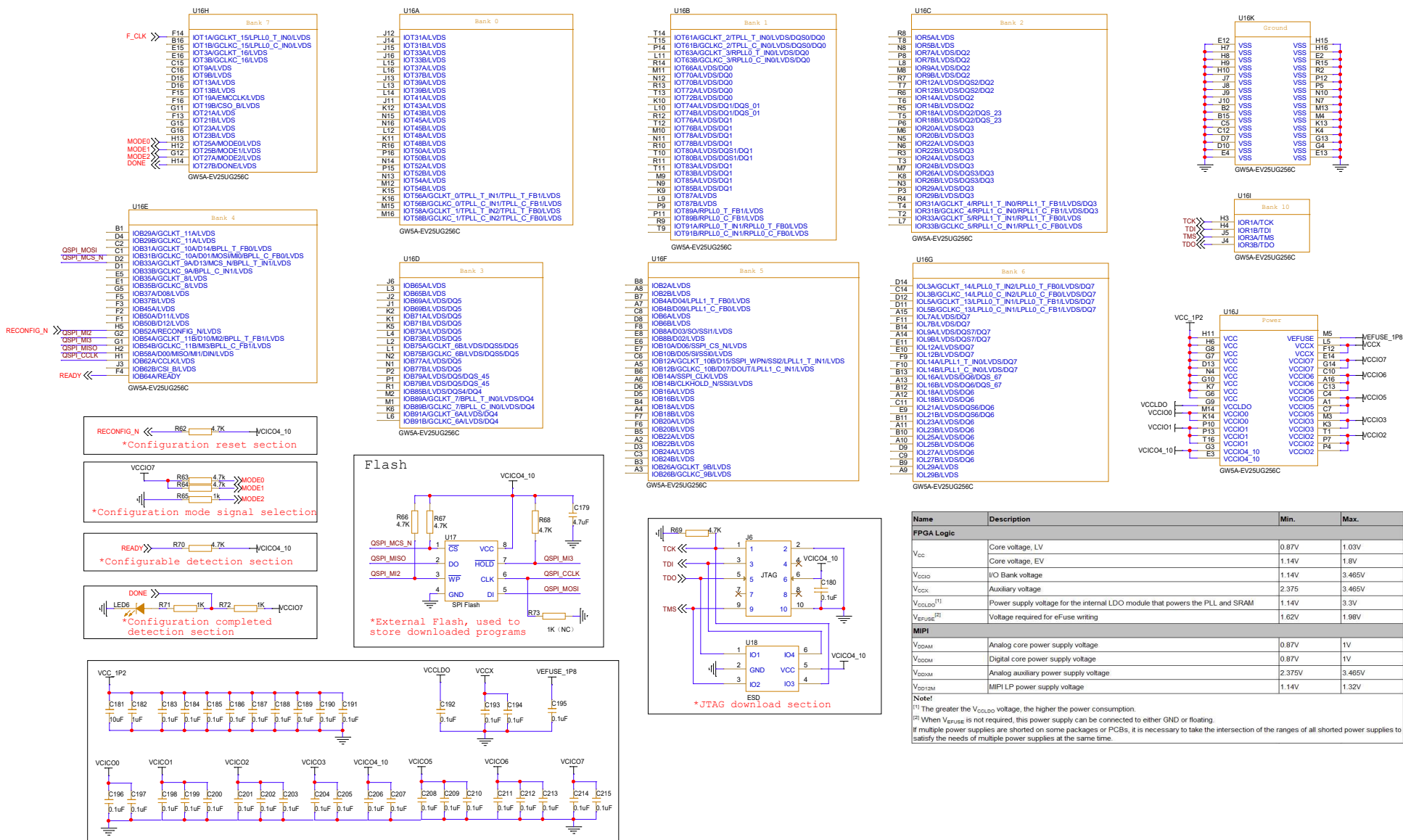
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.

- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.

For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.



GW5A-EV25UG256C

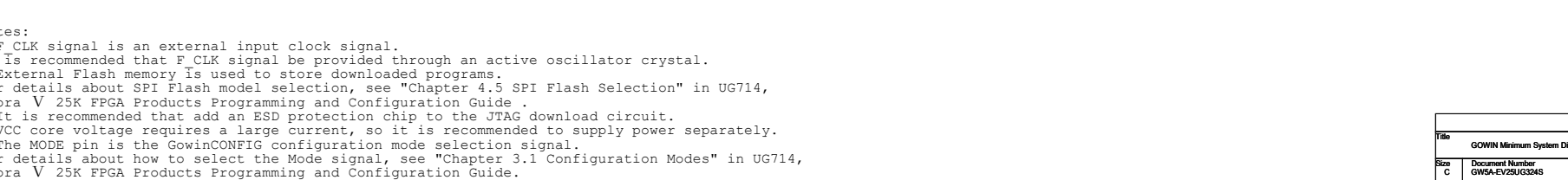
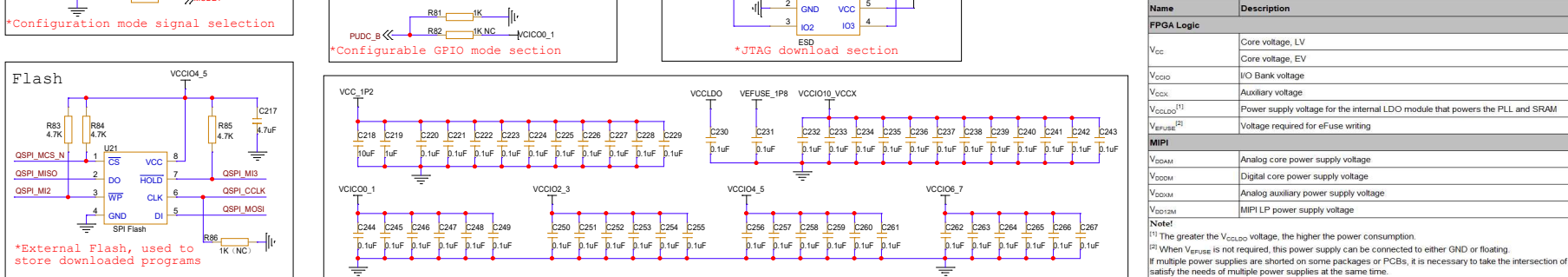
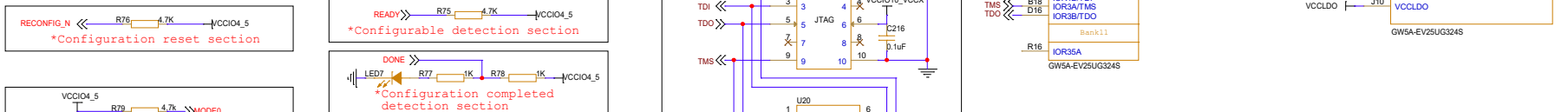
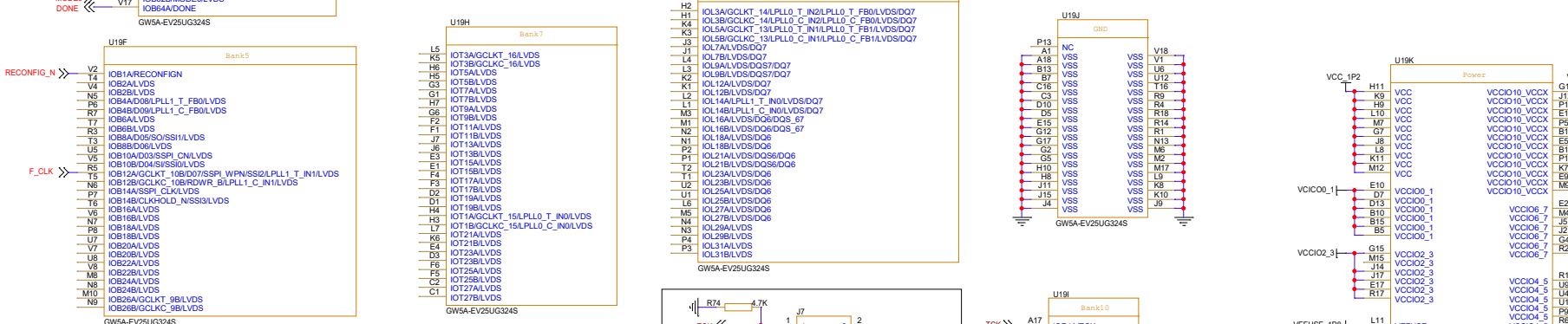
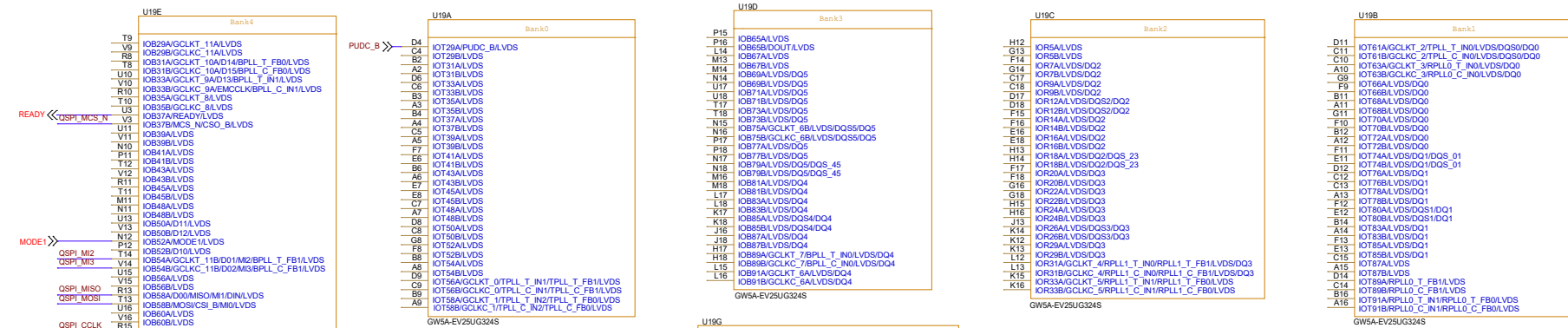


Notes:

- 1.F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.

Title			
GOWIN Minimum System Diagram			
Size	Document Number	Rev	
C	GW5A-EV25UG256C	2.6	
Date:	Friday, March 14, 2025	Sheet	6 of 17

GW5A-EV25UG324S



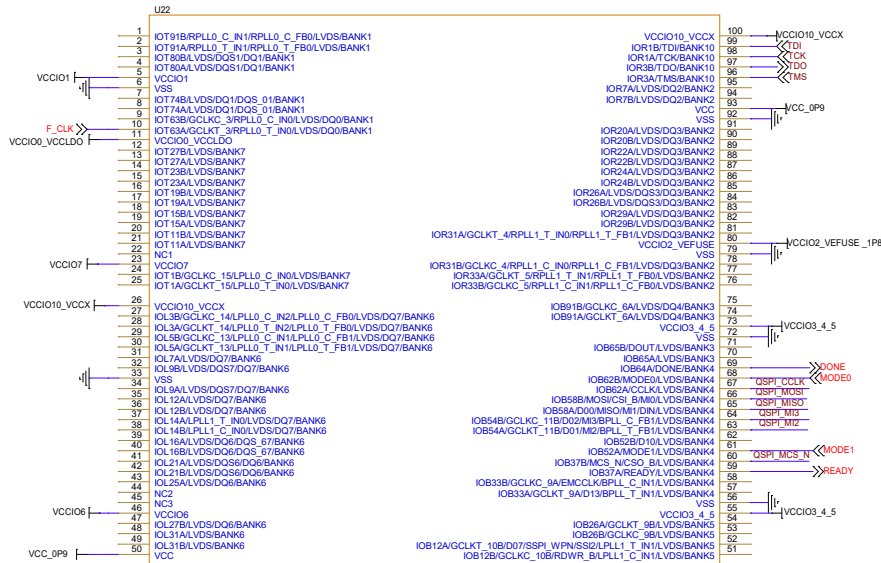
Notes:

- 1.F.CLK signal is an external input clock signal. It is recommended that F.CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.

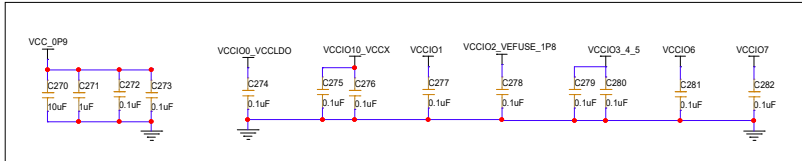
Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
V _{CC}	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCCL}	Auxiliary voltage	2.375	3.465V
V _{CCDDO} ^[1]	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{EFUSE} ^[2]	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V _{DDAM}	Analog core power supply voltage	0.87V	1V
V _{DDCM}	Digital core power supply voltage	0.87V	1V
V _{DDDM}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{DD12M}	MIPI LP power supply voltage	1.14V	1.32V

Note:
^[1] The greater the V_{CCDDO} voltage, the higher the power consumption.
^[2] When V_{EFUSE} is not required, this power supply can be connected to either GND or floating.
 If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.

GW5A-LV25LQ100



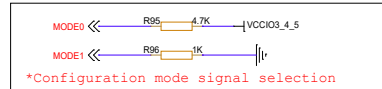
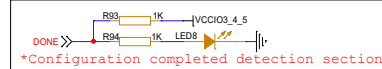
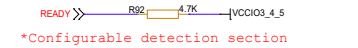
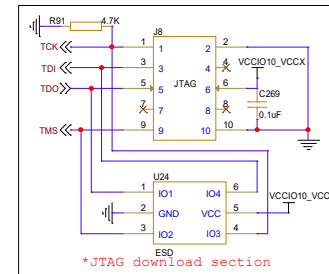
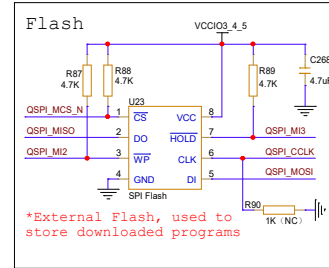
GW5A-LV25LQ100



Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCX}	Auxiliary voltage	2.375	3.465V
V _{CCLD0} ^[1]	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{EFUSE} ^[2]	Voltage required for eFUSE writing	1.62V	1.98V
MIPI			
V _{DDMI}	Analog core power supply voltage	0.87V	1V
V _{DDCM}	Digital core power supply voltage	0.87V	1V
V _{DDMI}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{DDI2M}	MIPI LP power supply voltage	1.14V	1.32V
Note!			
^[1] The greater the V _{CCLD0} voltage, the higher the power consumption.			
^[2] When V _{EFUSE} is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted (some packages or PCBs), it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			

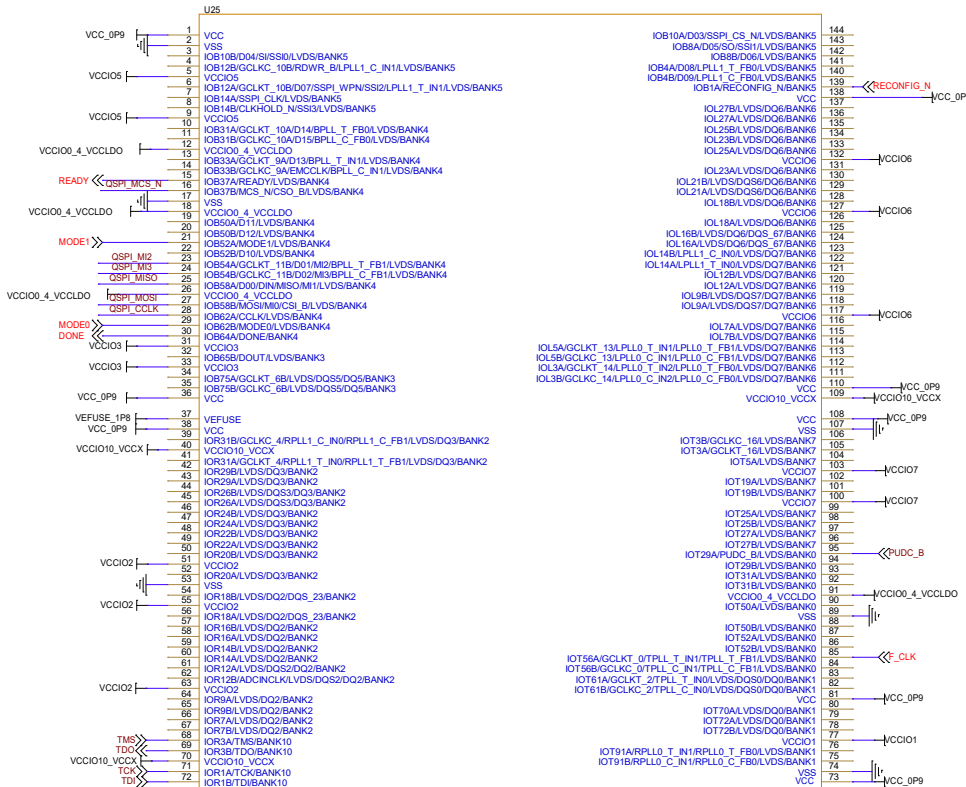
Notes:

- 1.F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.



Title GOWIN Minimum System Diagram			
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GW5A-LV25LQ144



GW5A-LV25LQ144

Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
V _{CC}	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCX}	Auxiliary voltage	2.375	3.465V
V _{CCLO} ^[1]	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{EFUSE} ^[2]	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V _{DDAM}	Analog core power supply voltage	0.87V	1V
V _{DDM}	Digital core power supply voltage	0.87V	1V
V _{DDM}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{DDI2M}	MIPI LP power supply voltage	1.14V	1.32V
Note:			
^[1] The greater the V _{CCLO} voltage, the higher the power consumption.			
^[2] When V _{EFUSE} is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			

Notes:

1.F.CLK signal is an external input clock signal.

2.It is recommended that F.CLK signal be provided through an active oscillator crystal.

2.External Flash memory is used to store downloaded programs.

For details about SPI Flash selection, see "Chapter 4.5 SPI Flash Selection" in UG714,

Arora V 25K FPGA Products Programming and Configuration Guide .

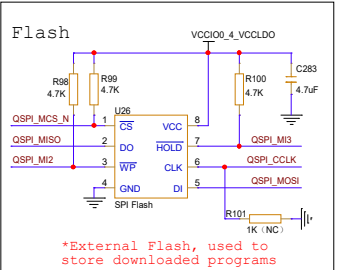
3.It is recommended that add an ESD protection chip to the JTAG download circuit.

4.VCC core voltage requires a large current, so it is recommended to supply power separately.

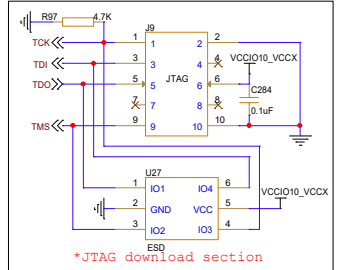
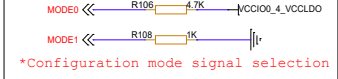
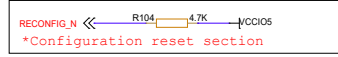
5.The MODE pin is the GowinCONFIG configuration mode selection signal.

For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714,

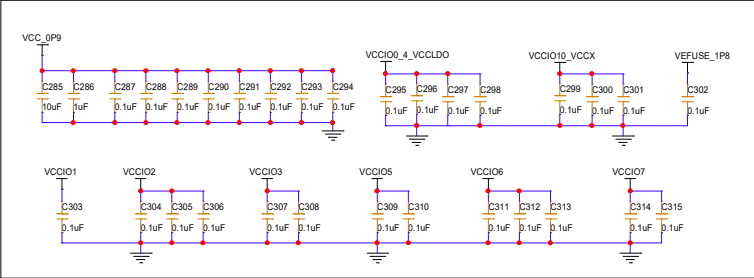
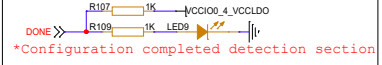
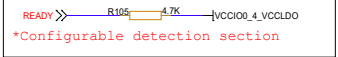
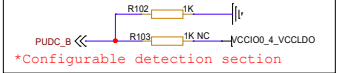
Arora V 25K FPGA Products Programming and Configuration Guide.



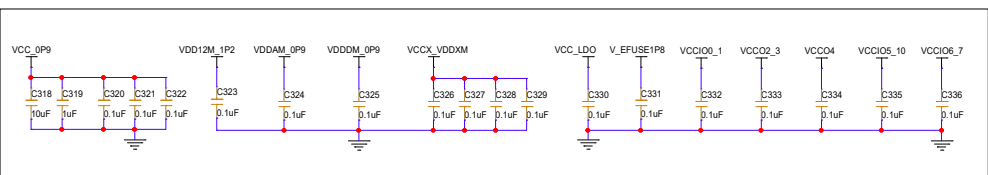
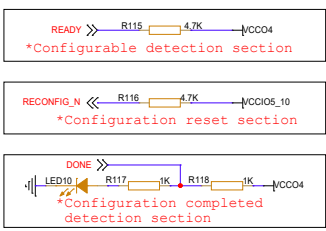
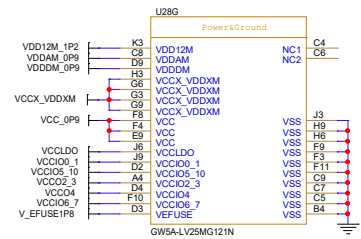
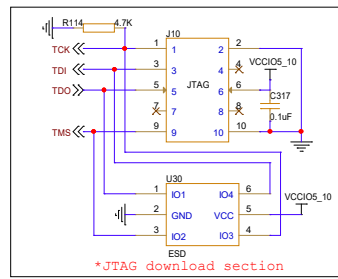
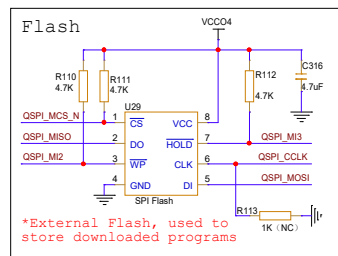
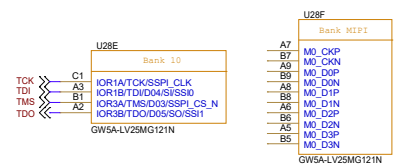
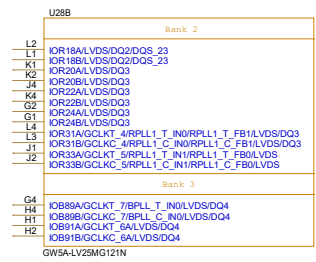
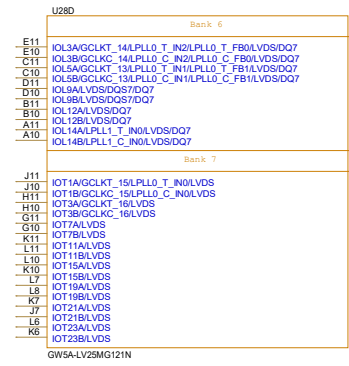
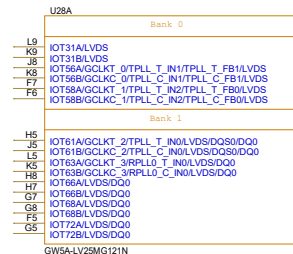
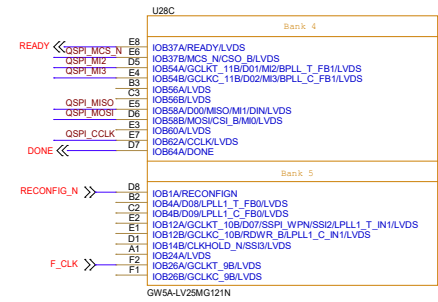
*External Flash, used to store downloaded programs



*JTAG download section



GW5A-LV25MG121N



Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
V _{CC}	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CC}	Auxiliary voltage	2.375V	3.465V
V _{CC}	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{CC}	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V _{CC}	Analog core power supply voltage	0.87V	1V
V _{CC}	Digital core power supply voltage	0.87V	1V
V _{CC}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{CC}	MIPI LP power supply voltage	1.14V	1.32V

Note!

[1] The greater the V_{CC} voltage, the higher the power consumption.

[2] When V_{CC} is not required, this power supply can be connected to either GND or floating.

If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.

Notes:

1.F CLK signal is an external input clock signal.

It is recommended that F CLK signal be provided through an active oscillator crystal.

2.External Flash memory is used to store downloaded programs.

For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .

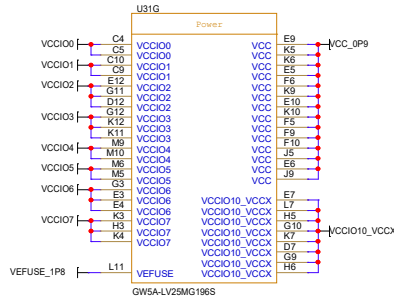
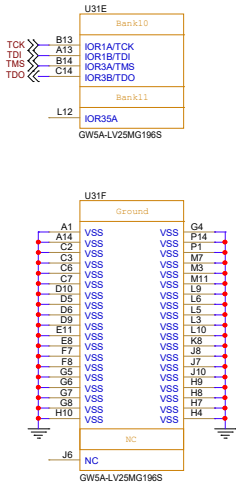
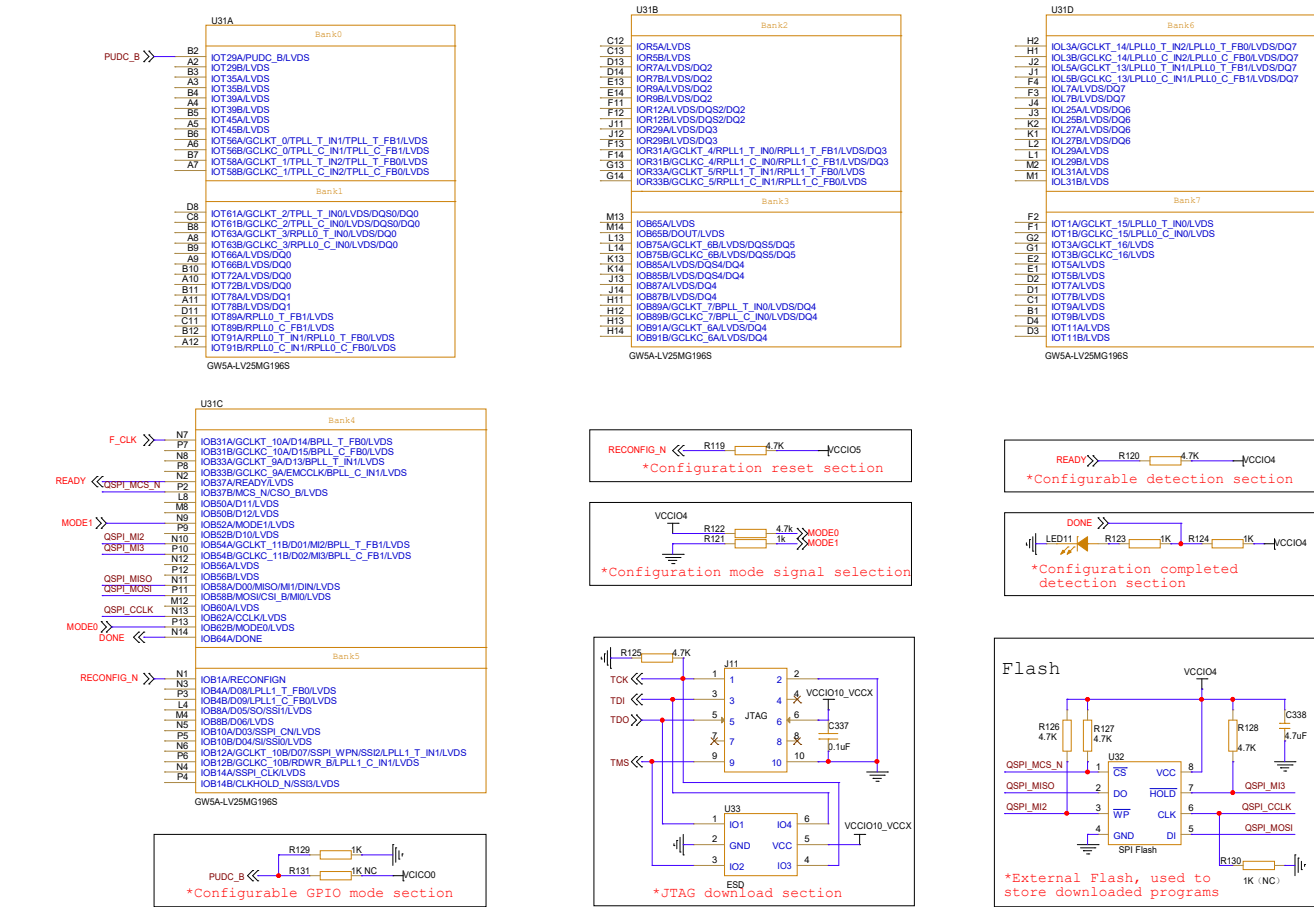
3.It is recommended that add an ESD protection chip to the JTAG download circuit.

4.VCC core voltage requires a large current, so it is recommended to supply power separately.

5.The MODE pin is the GowinCONFIG configuration mode selection signal.

For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.

GW5A-LV25MG196S



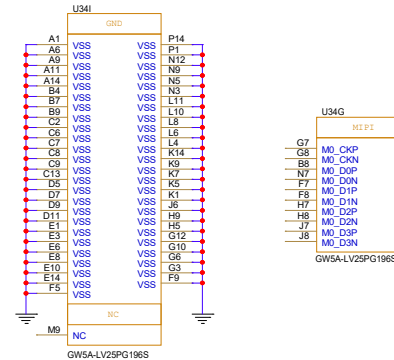
Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCX}	Auxiliary voltage	2.375	3.465V
V _{CCLOD} [1]	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{ERUSE} [2]	Voltage required for eFUSE writing	1.62V	1.98V
MIPI			
V _{DDAM}	Analog core power supply voltage	0.87V	1V
V _{DDDM}	Digital core power supply voltage	0.87V	1V
V _{DDXM}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{DD12M}	MIPI LP power supply voltage	1.14V	1.32V
Note!			
[1] The greater the V _{CCLOD} voltage, the higher the power consumption.			
[2] When V _{ERUSE} is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			

Notes:

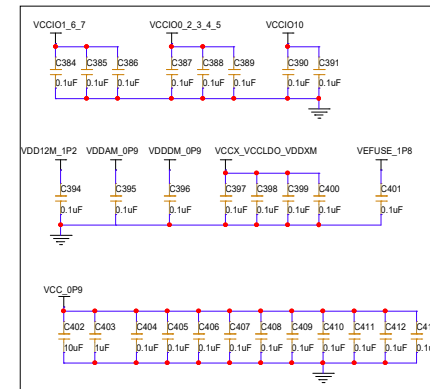
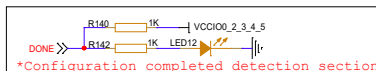
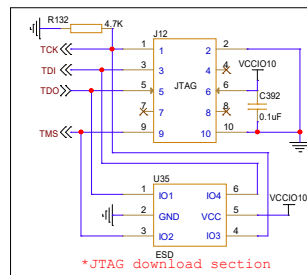
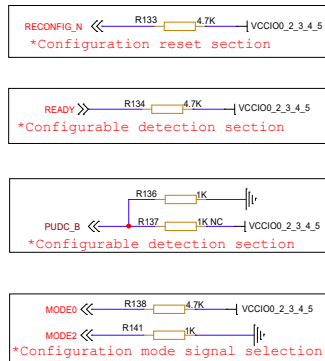
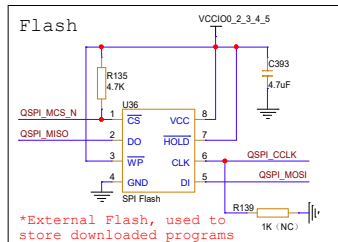
- 1.F_CLK signal is an external input clock signal. It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash mode selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arara V 25K FPGA Product Programming and Configuration Guide.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arara V 25K FPGA Products Programming and Configuration Guide.

Title			
GOWIN Minimum System Diagram			
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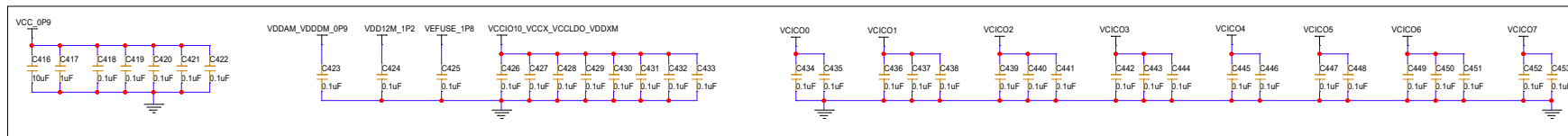
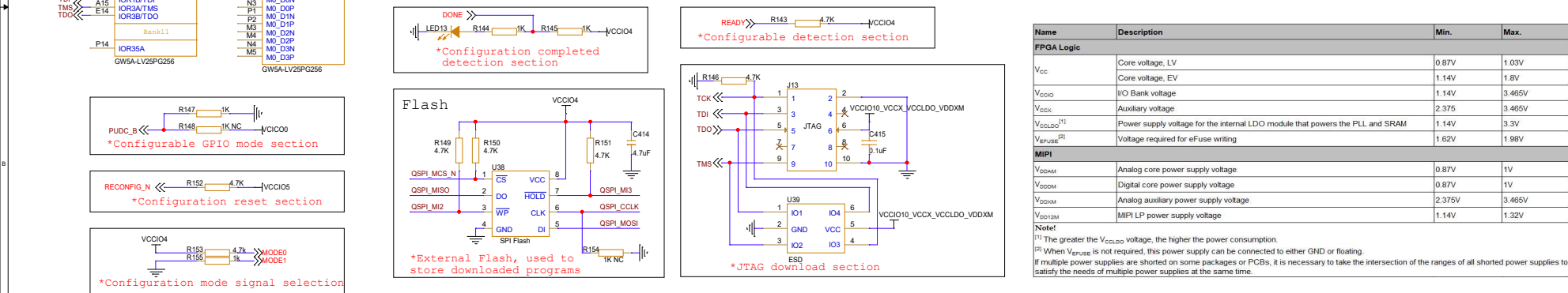
Name	Description	Min.	Max.
FPGA Logic			
V_{CC}	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V_{CCIO}	I/O Bank voltage	1.14V	3.465V
V_{CCM}	Auxiliary voltage	2.375	3.465V
$V_{CCDDO}^{(1)}$	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
$V_{EFUSE}^{(2)}$	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V_{DDMI}	Analog core power supply voltage	0.87V	1V
V_{DDDM}	Digital core power supply voltage	0.87V	1V
V_{DDMM}	Analog auxiliary power supply voltage	2.375V	3.465V
V_{DDI2M}	MIPI LP power supply voltage	1.14V	1.32V
Note!			
⁽¹⁾ The greater the V_{CCDDO} voltage, the higher the power consumption.			
⁽²⁾ When V_{EFUSE} is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			



Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arara V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arara V 25K FPGA Products Programming and Configuration Guide.

GW5A-LV25PG256

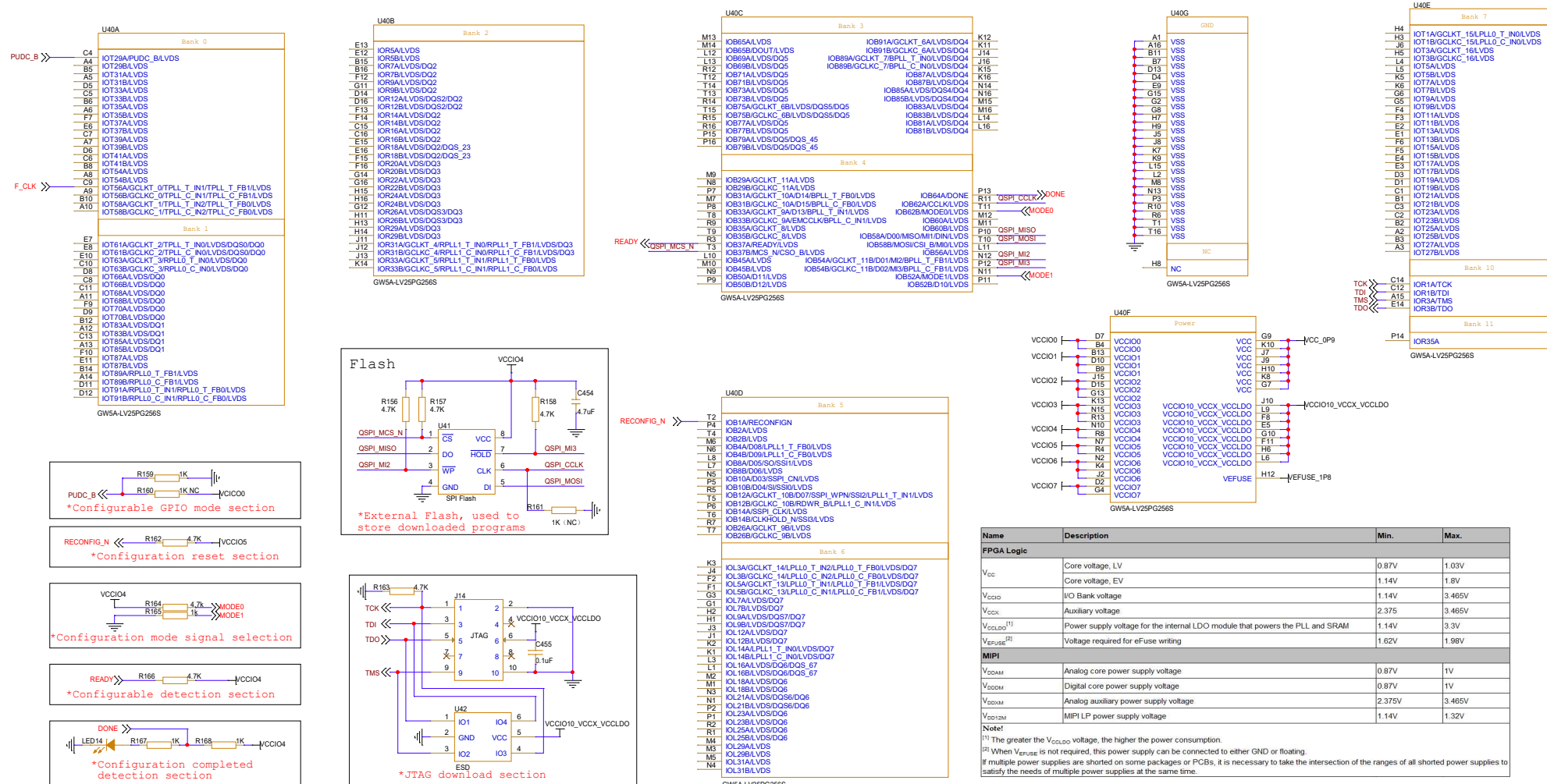


Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arara V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arara V 25K FPGA Products Programming and Configuration Guide.

Title				
GOWIN Minimum System Diagram				
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Notes:

1. F_CLK signal is an external input clock signal.
2. It is recommended that F_CLK signal be provided through an active oscillator crystal.
3. External Flash memory is used to store downloaded programs.
4. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
5. It is recommended that add an ESD protection chip to the JTAG download circuit.
6. VCC core voltage requires a large current, so it is recommended to supply power separately.
7. The MODE pin is the GowinCONFIG configuration mode selection signal.
8. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.

Title GOWIN Minimum System Diagram			
Size C	Document Number GW5A-LV25PG256S		Rev 2.6
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GW5A-LV25UG256C

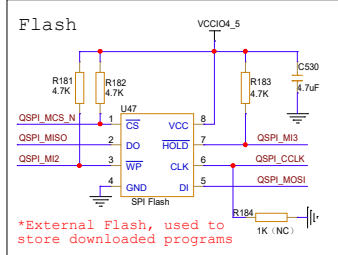
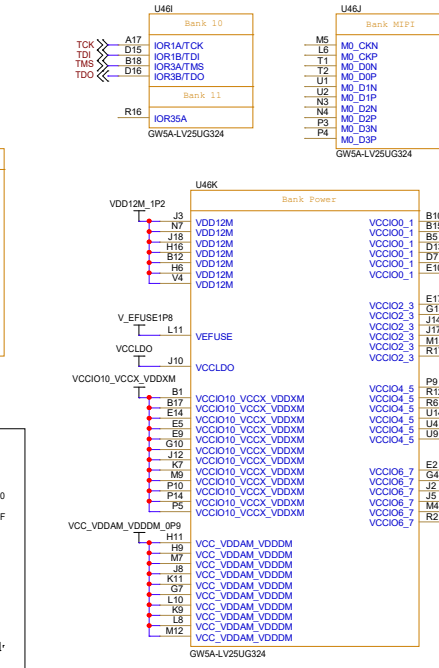
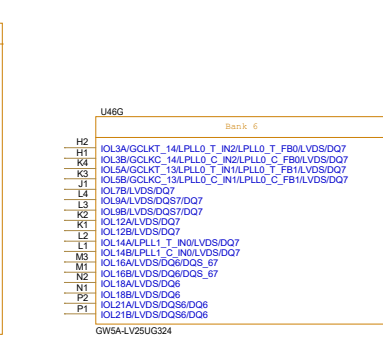
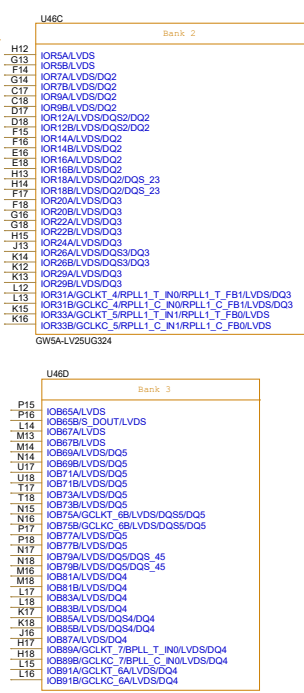
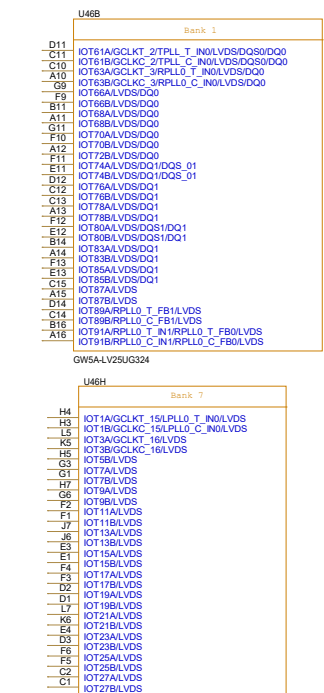
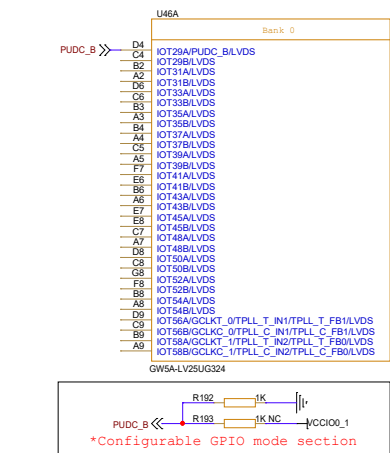
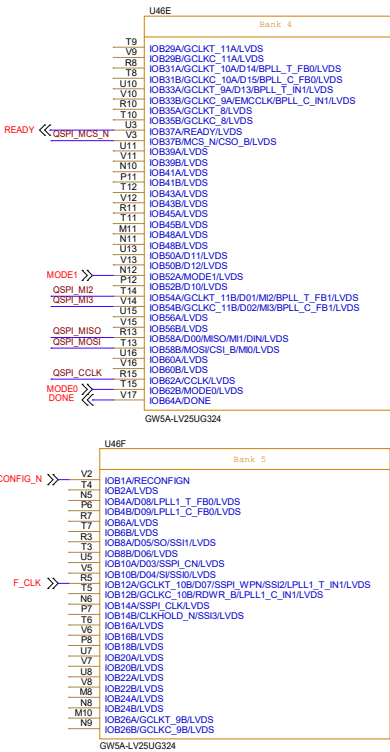


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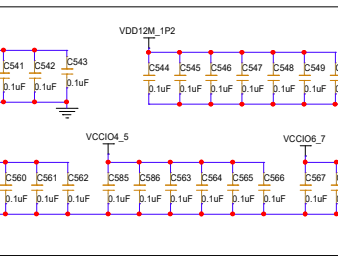
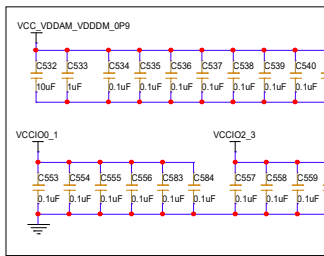
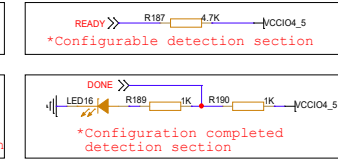
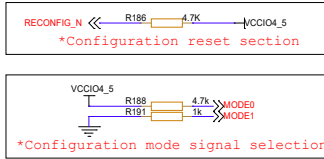
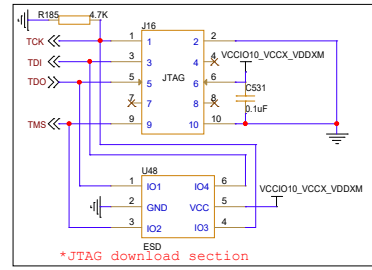
- 1.F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.

Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
V _{CC}	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CC2K}	Auxiliary voltage	2.375	3.465V
V _{CCLD0} ⁽¹⁾	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{EFUSE} ⁽²⁾	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V _{DDAH}	Analog core power supply voltage	0.87V	1V
V _{DDDM}	Digital core power supply voltage	0.87V	1V
V _{DDAM}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{DDI2M}	MIPI LP power supply voltage	1.14V	1.32V
Note!			
⁽¹⁾ The greater the V _{CCLD0} voltage, the higher the power consumption.			
⁽²⁾ When V _{EFUSE} is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			

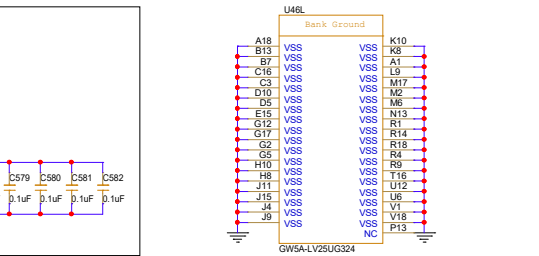
GW5A-LV25UG324



*External Flash, used to store downloaded programs



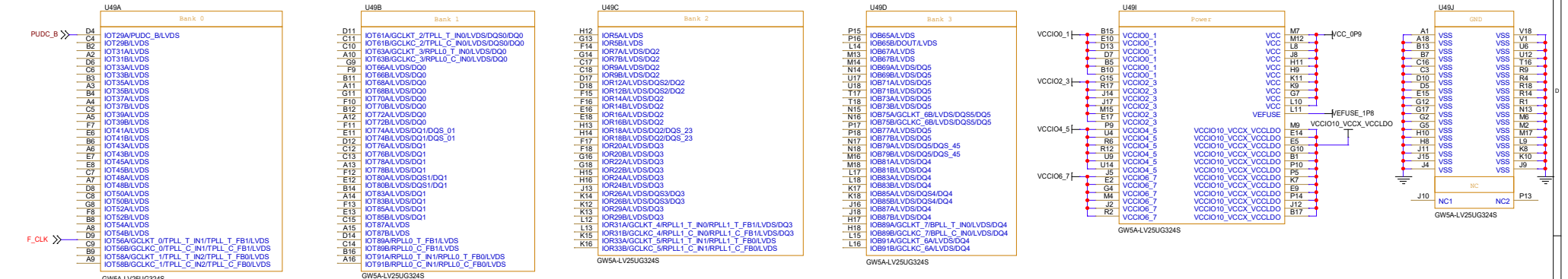
Power	Min.	Max.
V _{CC}	0.87V	1.02V
V _{CCIO}	1.14V	1.18V
V _{CCIO2}	1.14V	3.465V
V _{CCIO3}	2.375V	3.465V
V _{CCIO4}	1.14V	3.3V
V _{CCIO5}	1.62V	1.98V
V _{CCIO6}	0.87V	1V
V _{CCIO7}	0.87V	1V
V _{CCIO8}	2.375V	3.465V
V _{CCIO9}	1.14V	1.32V



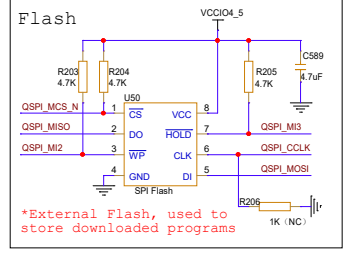
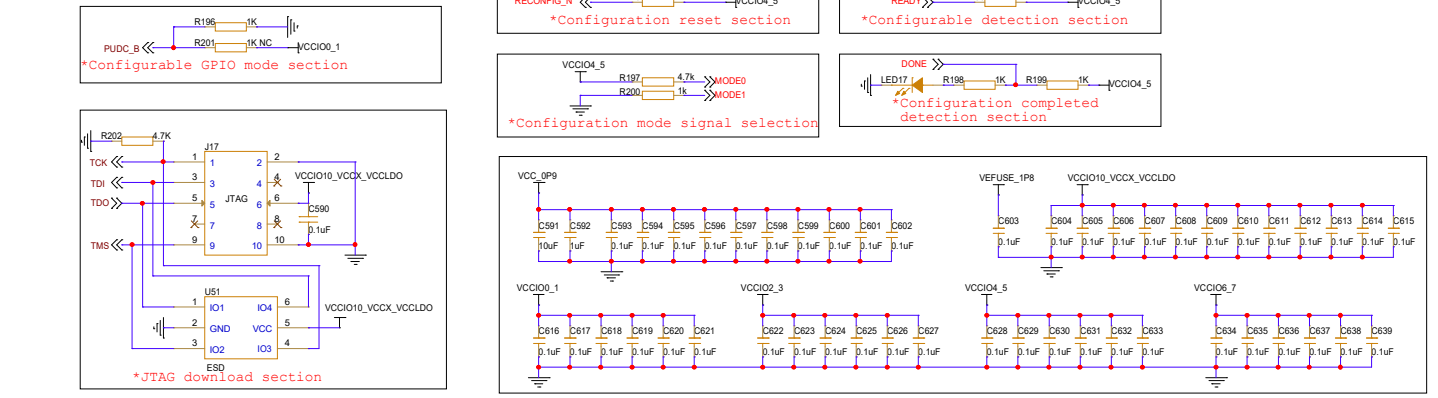
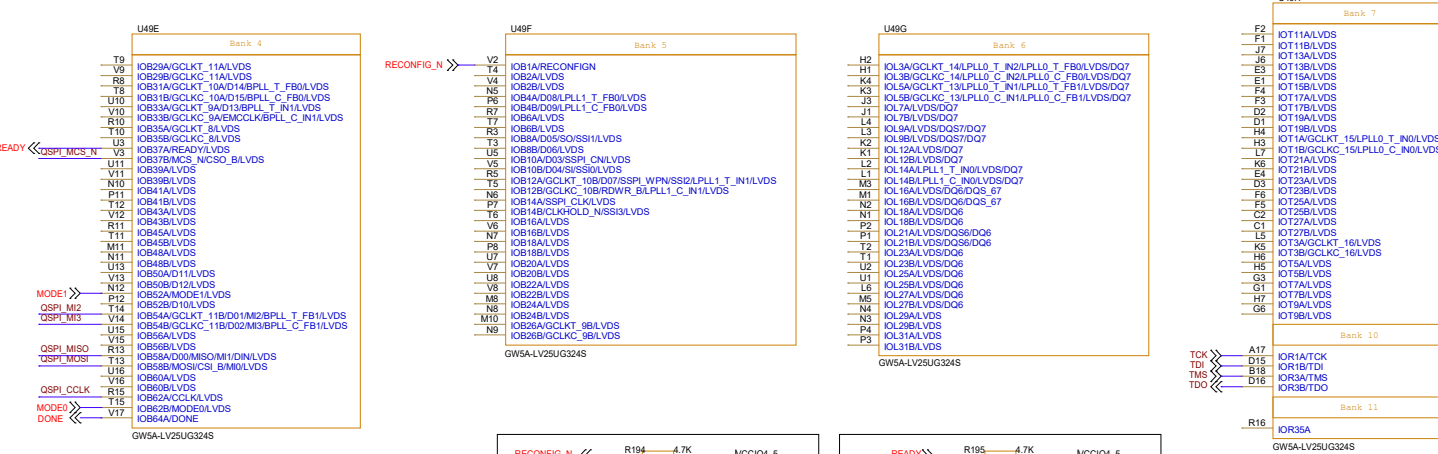
Notes:

- 1.F CLK signal is an external input clock signal.
- It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
- For details about SPI Flash Model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.

GW5A-LV25UG324S



Name	Description	Min.	Max.
Power			
V _{CC}	Core voltage, LV	0.87V	1.03V
V _{CC}	Core voltage, EV	1.14V	1.8V
V _{CCIO}	IO Bank voltage	1.14V	3.465V
V _{CCIO}	Auxiliary voltage	2.375	3.465V
V _{CCIO} ⁽¹⁾	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{REFUSE} ⁽²⁾	Voltage required for eFuse writing	1.62V	1.98V
MPI			
V _{CCIO}	Analog core power supply voltage	0.87V	1V
V _{CCIO}	Digital core power supply voltage	0.87V	1V
V _{CCIO}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{CCIO}	MPI LP power supply voltage	1.14V	1.32V
Note!			
⁽¹⁾ The greater the V _{CCIO} voltage, the higher the power consumption.			
⁽²⁾ When V _{REFUSE} is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			



Notes:

- 1.F CLK signal is an external input clock signal.
- It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.