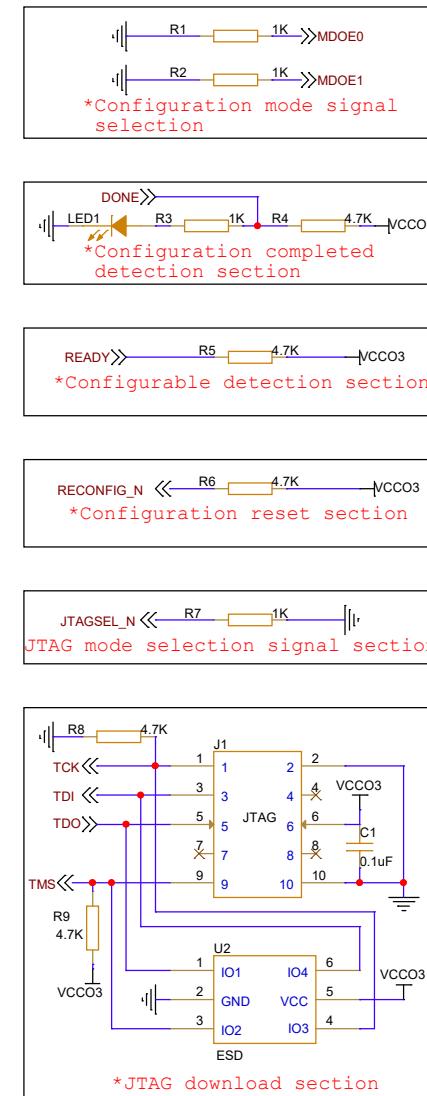


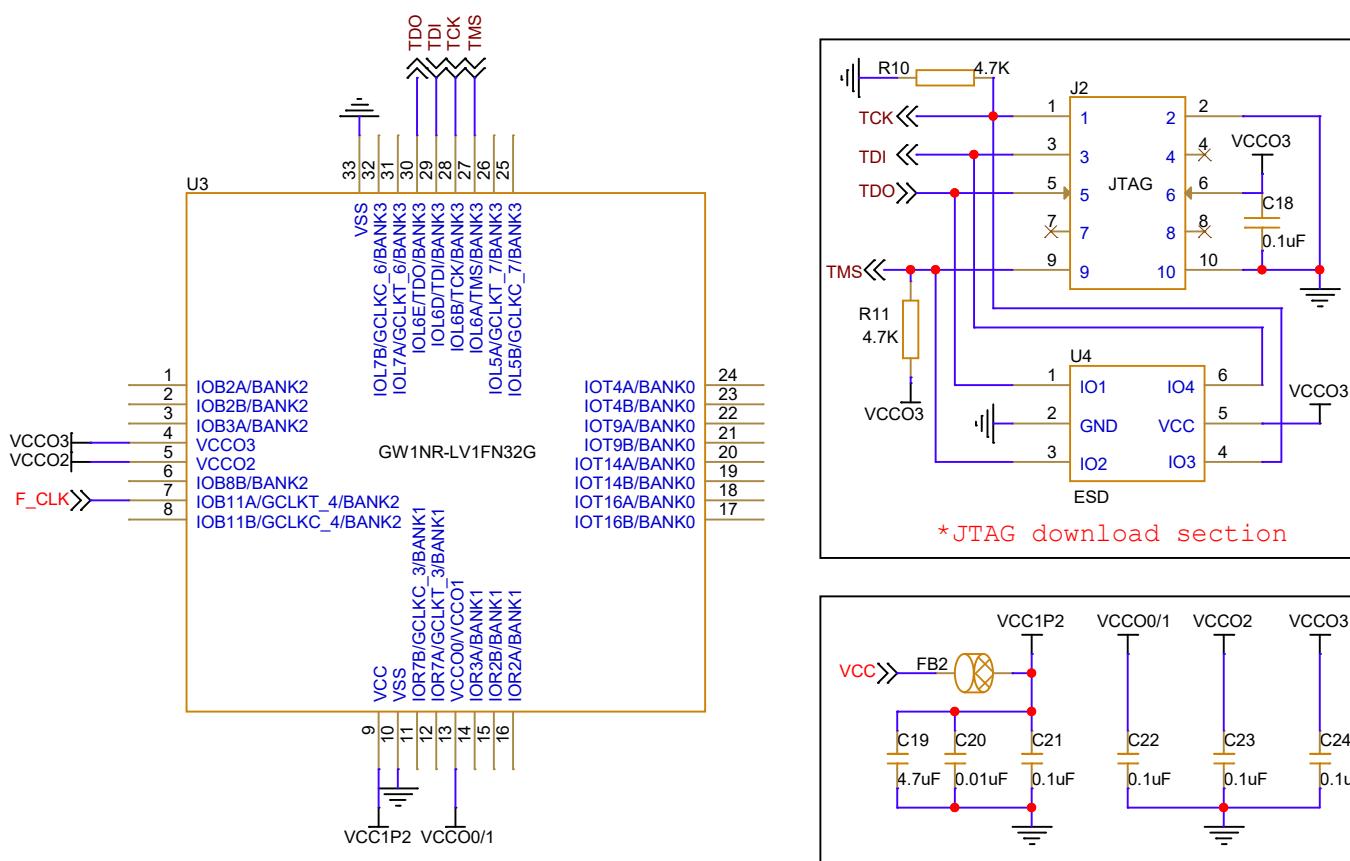
## Notes

- 1.F<sub>CLK</sub> signal is an external input clock signal.  
It is recommended that F<sub>CLK</sub> signal be provided through an active oscillator crystal  
2.It is recommended that add an ESD protection chip to the JTAG download circuit.



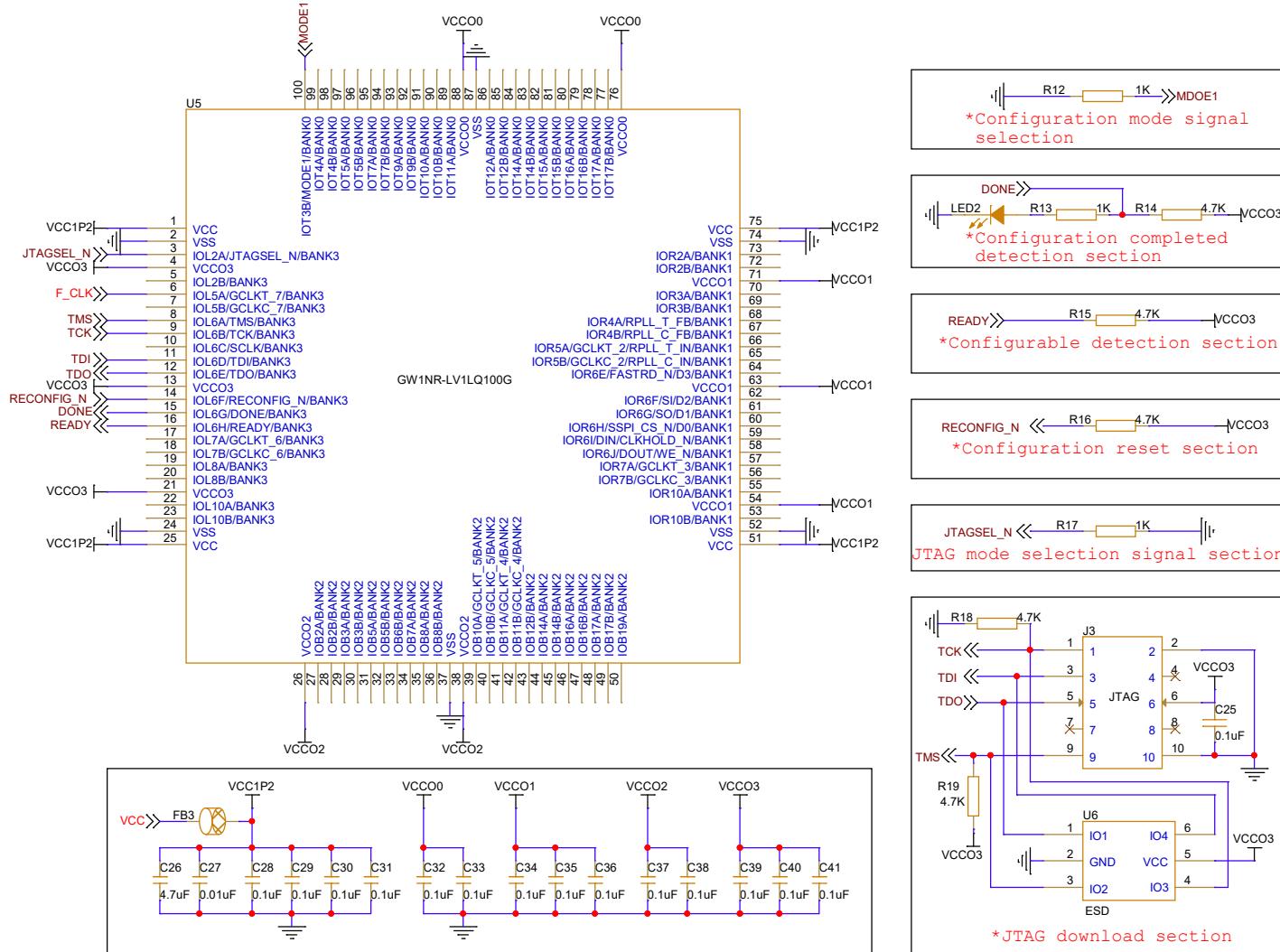
Title		GOWIN Minimum System Diagram		
Size	Document Number			
B	GW1NR-LV1EQ144G	Rev	2.1	
Date:	Wednesday, April 10, 2024	Sheet	1	of 5

# GW1NR-LV1FN32G



## Notes:

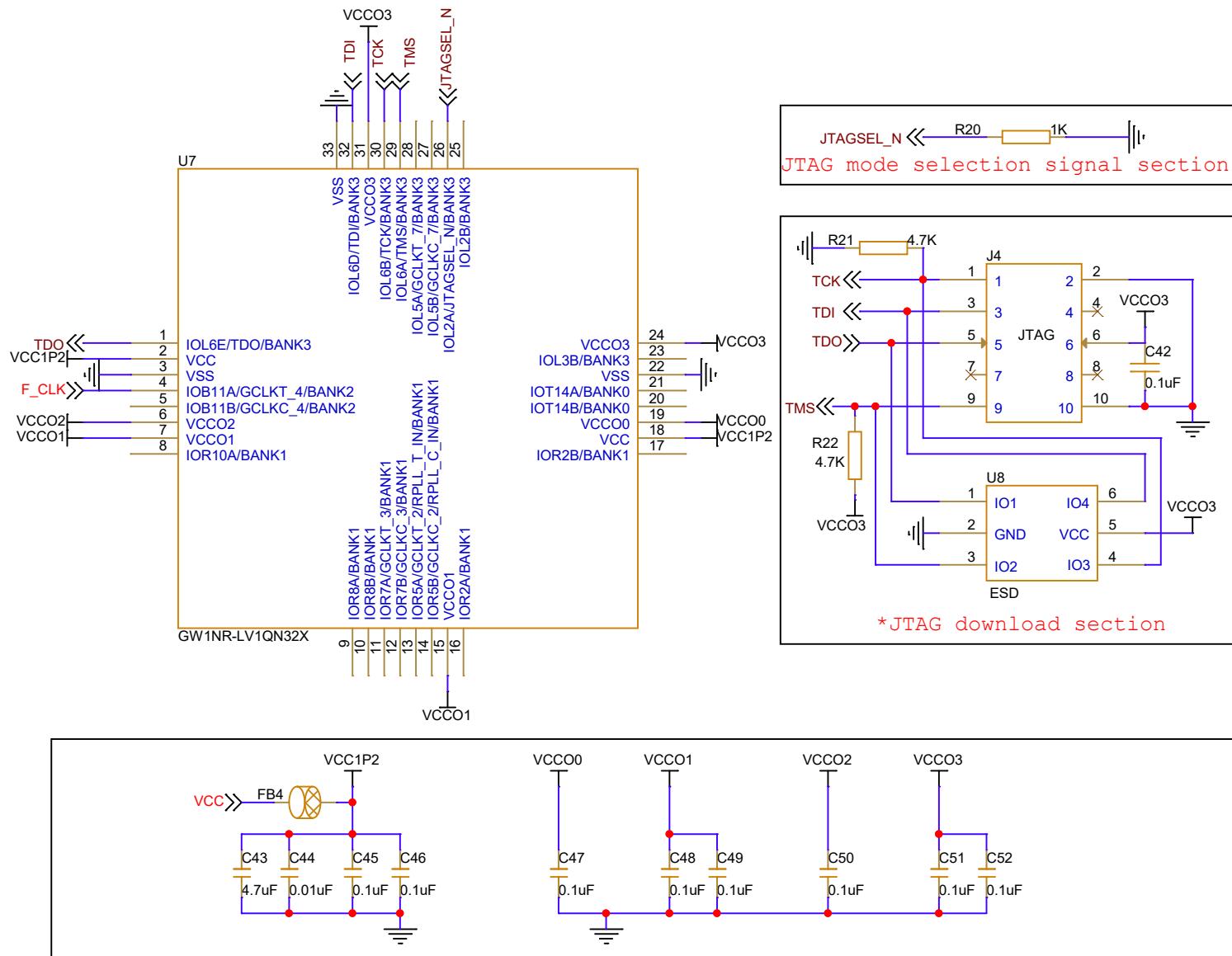
1. F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.



Title	
GOWIN Minimum System Diagram	
Size	Document Number
B	GW1NR-LV1LQ100G

Date: Wednesday, April 10, 2024 Sheet 3 of 5 Rev 2.1

# GW1NR-LV1QN32X



## Notes:

1. F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title  
GOWIN Minimum System Diagram

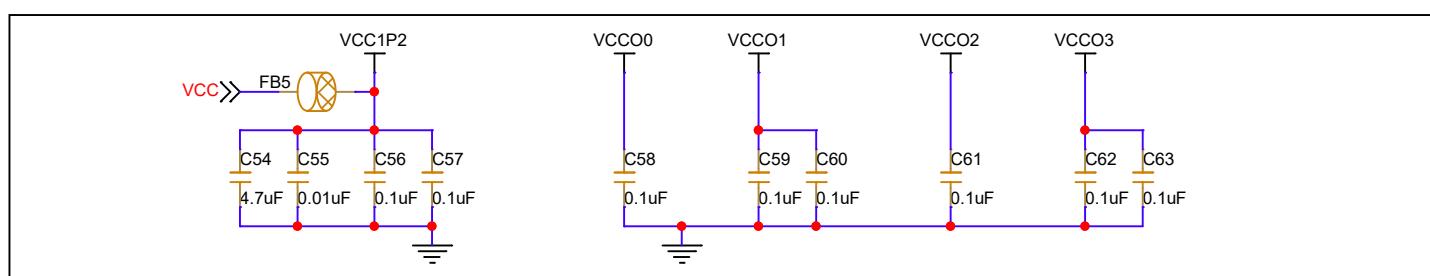
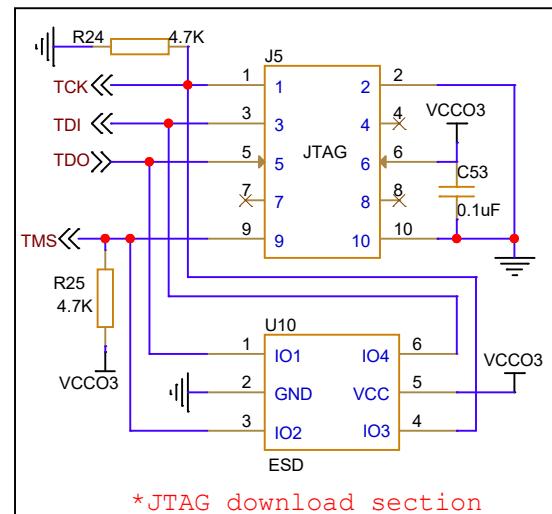
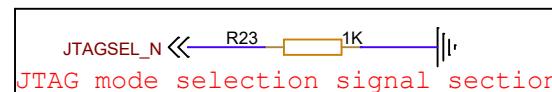
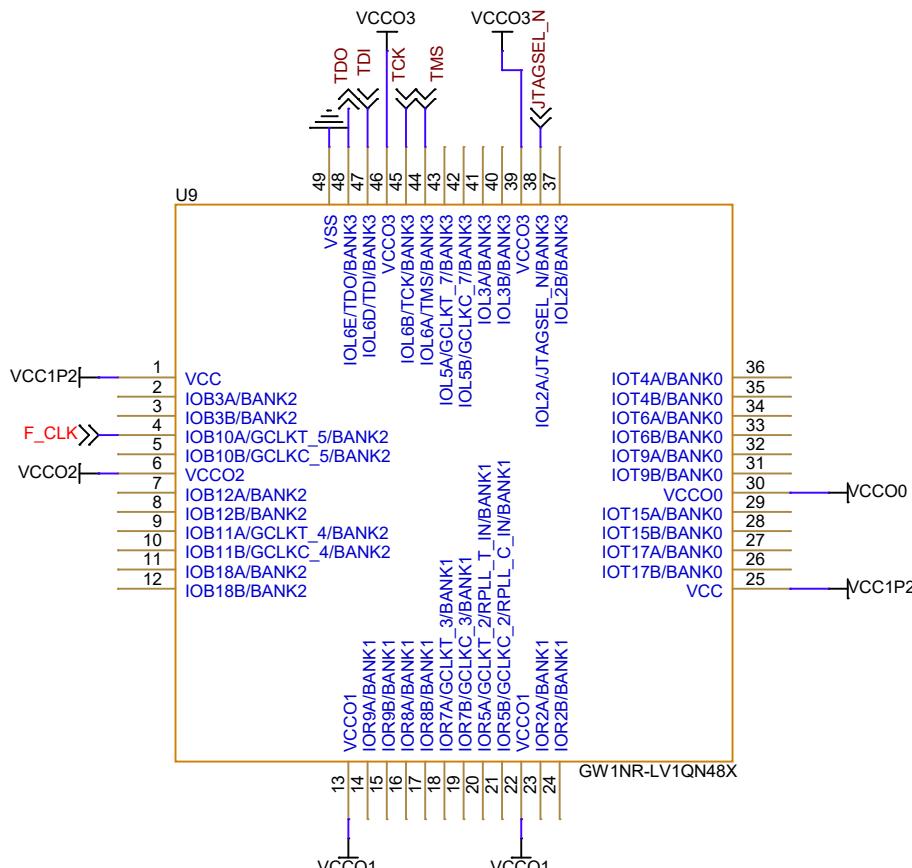
Size A4 Document Number  
GW1NR-LV1QN32X

Rev 2.1

Date: Wednesday, April 10, 2024

Sheet 4 of 5

# GW1NR-LV1QN48X



## Notes:

1. F\_CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title	
GOWIN Minimum System Diagram	
Size	Document Number
A4	GW1NR-LV1QN48X
Date:	Wednesday, April 10, 2024
Rev	2.1