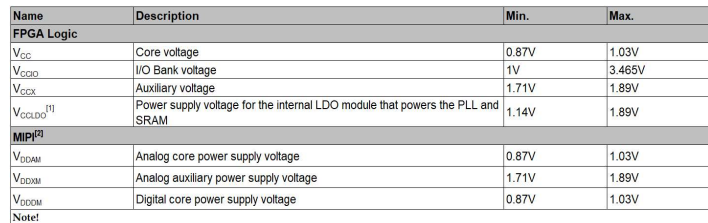
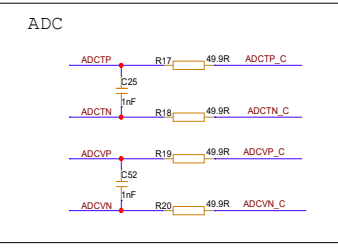
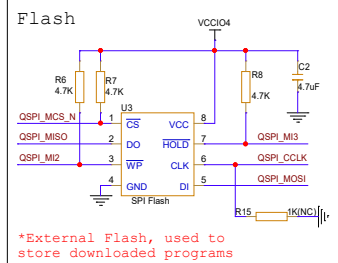
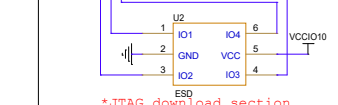
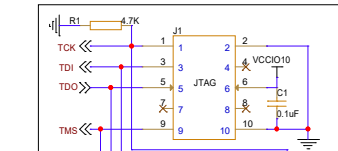
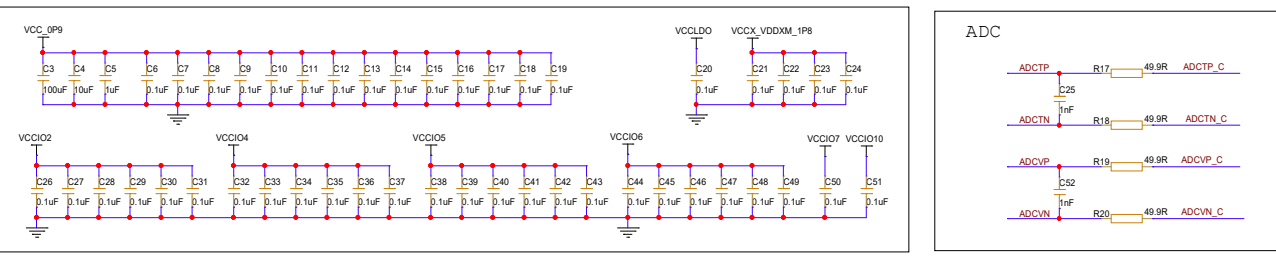
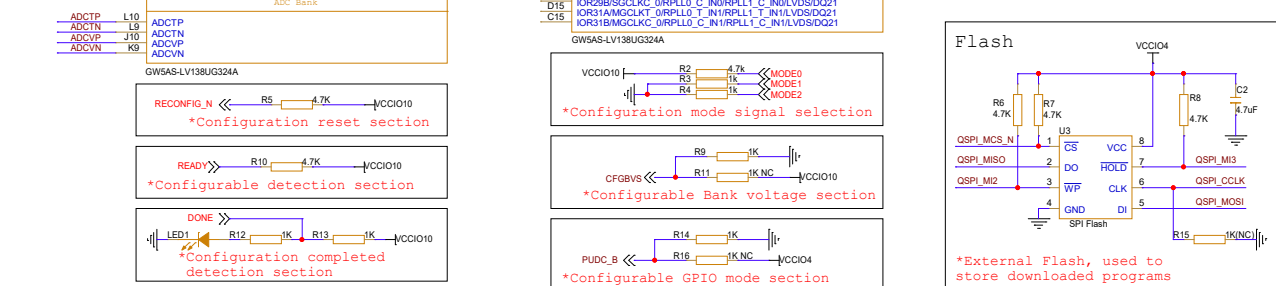
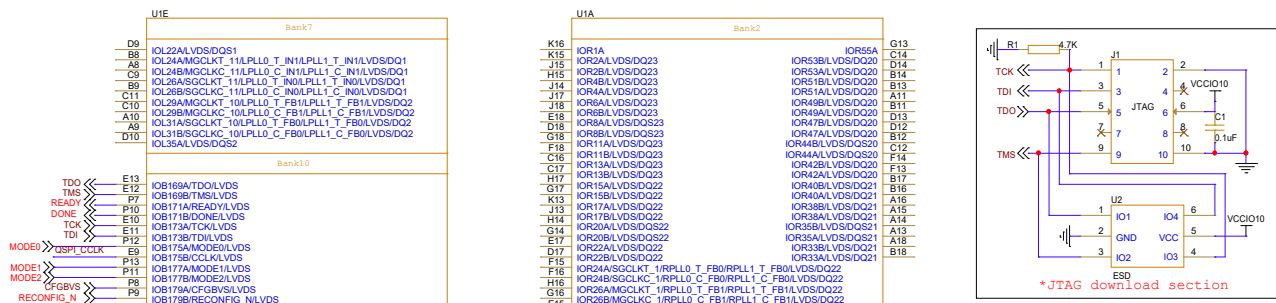
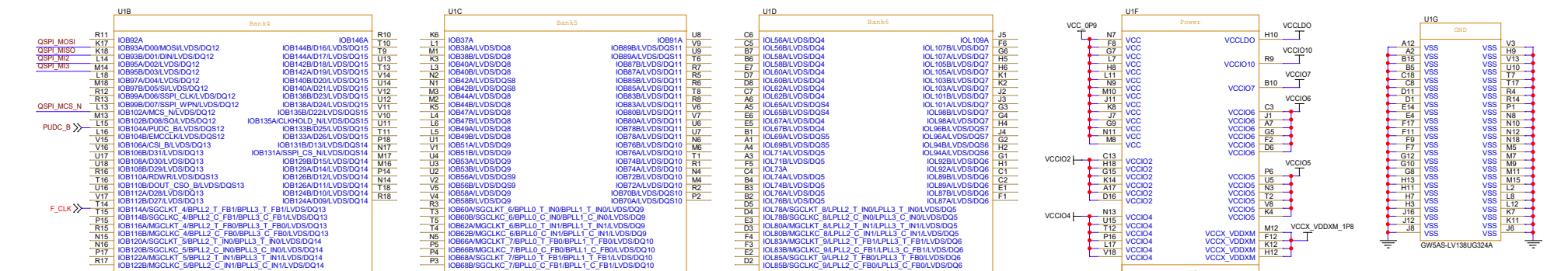
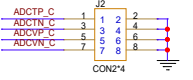


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[2] For packages that do not support MIPI hard core, the MIPI voltage can be excluded.
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.

| | |
|--------|----------------------|
| CFGVBS | VCCIO (Bank4、Bank10) |
| 1 | 2.5V and 3.3V |
| 0 | VCCIO≤1.8V |



- F_CLK signal is an external input clock signal.
- It is recommended that F_CLK signal be provided through an active oscillator crystal.
- External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG704, *Corax V FPGA Products Programming and Configuration Guide*.
- It is recommended that add an ESD protection chip to the JTAG download circuit.
- VCC core voltage requires a large current, so it is recommended to supply power separately.
- The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, *Corax V FPGA Products Programming and Configuration Guide*.