

## GW5ART-LV15CM90P

**U1A**

Pin	Signal	Bank
J3	QSPI_M2	Bank 2
K3	QSPI_MISO	Bank 2
J2	QSPI_CCLK	Bank 2
K2	QSPI_MCS_N	Bank 2
J1	QSPI_MIS	Bank 2
K1	QSPI_MOSI	Bank 2
H1	IOB8A/READY	Bank 2
D6	IOI29A/DONE/LVDS	Bank 3
C6	IOI29B/RECONFIG_N/LVDS	Bank 3
D9	IOI31A/GCLK_5/MODE0/LVDS	Bank 3
D8	IOI31B/GCLK_5/MODE0/LVDS	Bank 3
A7	IOI33A/GCLK_4/LPLL_T_IN1/LPLL_T_FB0/CS0_B/OUT/SC/LVDS	Bank 3
B7	IOI33B/GCLK_4/LPLL_C_IN1/LPLL_C_FB0/CS1_B/SDA/LVDS	Bank 3
A6	IOI35A/D05/SSPI_CS_N/LVDS	Bank 3
B6	IOI35B/D05/SSPI_CS_N/LVDS	Bank 3
A9	IOI20A/TCK/LVDS	Bank 4
B9	IOI20B/TMS/LVDS	Bank 4
A8	IOI22A/GCLK_7/Q0REF_T_IN0/SSPI_CLK/LVDS	Bank 4
B8	IOI22B/GCLK_7/Q0REF_T_IN0/SSPI_CLK/LVDS	Bank 4
C9	IOI24A/TDI/LVDS	Bank 4
D9	IOI24B/TDO/LVDS	Bank 4
C7	IOI26A/GCLK_6/LPLL_T_IN0/LPLL_T_FB1/Q0REF_T_IN1/D07/CLKHOLD_N/SSPI3/LVDS	Bank 4
D7	IOI26B/GCLK_6/LPLL_C_IN0/LPLL_C_FB1/Q0REF_T_IN1/D07/SSPI3/LVDS	Bank 4

**U1B**

Pin	Signal
G9	M0_CKP
E9	M0_CKN
E8	M0_D0P
F9	M0_D0N
F8	M0_D1P
H9	M0_D1N
H8	M0_D2P
J9	M0_D2N
J8	M0_D3P
J7	M0_D3N

**U1C**

Pin	Signal
A5	Q0_LN0_RXP_I
B5	Q0_LN0_RXM_I
A4	Q0_LN1_RXP_I
B4	Q0_LN1_RXM_I
A2	Q0_LN2_RXP_I
B2	Q0_LN2_RXM_I
A1	Q0_LN3_RXP_I
B1	Q0_LN3_RXM_I
A3	Q0_REFCLKP_0
B3	Q0_REFCLKM_0

**U1D**

Pin	Signal
D3	VDDAQ0_0P9
D2	VDDAQ0_0P9
E3	VDDTQ0_0P9
D4	VDDHAQ0_1P8
G2	VDDHAQ0_1P8
E2	VDDHAQ0_1P8
F2	VDDHAQ0_1P8
G4	VDDAM_0P9
H5	VCCX_VCCLD0_VDDXM
J5	VCCX_VCCLD0_VDDXM
J4	VCCX_VCCLD0_VDDXM
K4	VDD12M_1P2

**U1E**

Pin	Signal
K9	VSS
H7	VSS
J7	VSS
K7	VSS
F7	VSS
H6	VSS
J6	VSS
H5	VSS
J5	VSS
D5	VSS
C5	VSS
C3	VSS
C2	VSS
H2	VSS
H1	VSS
C1	VSS
D1	VSS
K6	VSS
F1	VSS
E1	VSS
G7	VSS
K8	NC1
F6	NC2
G1	NC3

**\*Configurable detection section**

**\*Configuration completed detection section**

**\*Configuration mode signal selection**

**\*Configuration reset section**

**\*JTAG download section**

**\*External Flash, used to store downloaded programs**

Name	Description	Min.	Max.
<b>FPGA Logic</b>			
V <sub>CC</sub>	Core voltage, LV	0.87V	1.03V
V <sub>CCIO</sub>	I/O Bank voltage	1.14V	3.465V
V <sub>CCX</sub> <sup>[1]</sup>	Auxiliary voltage	1.71V	3.465V
V <sub>CCLD0</sub>	Power supply voltage of internal LDO module that powers PLL and SRAM	1.14V	2.75V
V <sub>EFUSE</sub> <sup>[2]</sup>	Voltage required for eFuse writing	1.62V	1.98V
<b>Gigabit Transceiver</b>			
V <sub>DDHAQ*</sub>	Analog high power supply voltage	1.71V	1.89V
V <sub>DDAQ*</sub>	Analog core power supply voltage	0.87V	1.03V
V <sub>DDTQ*</sub>	Serdes transmitter power supply voltage	0.87V	1.03V
<b>MIPI</b>			
V <sub>DDAM</sub>	Analog core power supply voltage	0.855V	1.08V
V <sub>DDXM</sub>	Analog auxiliary power supply voltage	1.71V	3.465V
V <sub>DDDM</sub>	Digital core power supply voltage	0.87V	1.08V
V <sub>DD12M</sub>	MIPI LP power supply voltage	1.14V	1.32V
<b>PSRAM</b>			
V <sub>DDP</sub>	PSRAM power supply voltage	1.71V	1.89V
V <sub>DDQP</sub>	PSRAM data bus power supply voltage	1.71V	1.89V
<b>Note!</b>			
<sup>[1]</sup> When internal differential termination resistors are required, V <sub>CCX</sub> must be greater than or equal to 3V; the IO input-output F <sub>max</sub> is limited when V <sub>CCX</sub> =1.8V, and V <sub>CCX</sub> needs to be greater than or equal to 2.5V for input-output applications with F <sub>max</sub> greater than 600Mbps.			
<sup>[2]</sup> When V <sub>EFUSE</sub> is not required, this power			

## GW5ART-LV15CM90P

**U1A**

Pin	Signal	Bank
J3	QSPI_MISO	Bank 2
J2	QSPI_CCLK	Bank 2
J1	QSPI_MCS_N	Bank 2
K1	QSPI_MIS	Bank 2
K1	QSPI_MOSI	Bank 2
H1	IOB8A/READY	Bank 2
D6	IOL29A/DONE/LVDS	Bank 3
D5	IOL29B/RECONFIG_N/LVDS	Bank 3
D9	IOL31A/GCLK_5/MODE0/LVDS	Bank 3
D8	IOL31B/GCLK_5/MODE0/LVDS	Bank 3
A7	IOL33A/GCLK_4/LPLL_T_IN1/LPLL_T_FB0/CS0_B/OUT/SC/LVDS	Bank 3
A6	IOL33B/GCLK_4/LPLL_C_IN1/LPLL_C_FB0/CS1_B/SDA/LVDS	Bank 3
B6	IOL35A/D05/SSPI_CS_N/LVDS	Bank 3
A9	IOL20A/TCK/LVDS	Bank 4
B9	IOL20B/TMS/LVDS	Bank 4
B8	IOL22A/GCLK_7/Q0REF_T_IN0/SSPI_CLK/LVDS	Bank 4
C9	IOL22B/GCLK_7/Q0REF_C_IN0/RDWR_B/SQ/SSH/PCIE_HOST_RSTN/LVDS	Bank 4
C8	IOL24A/TDI/LVDS	Bank 4
C7	IOL24B/TDO/LVDS	Bank 4
D7	IOL36A/GCLK_6/LPLL_T_IN0/LPLL_T_FB1/Q0REF_T_IN1/D07/CLKHOLD_N/SSI3/LVDS	Bank 4
D7	IOL26B/GCLK_6/LPLL_C_IN0/LPLL_C_FB1/Q0REF_C_IN1/D07/SSPI_WPN/SSI2/LVDS	Bank 4

**U1B**

Pin	Signal
G9	M0_CKP
E9	M0_CKN
E8	M0_D0P
F9	M0_D0N
F8	M0_D1P
H9	M0_D1N
H8	M0_D2P
J9	M0_D2N
J8	M0_D3P
J8	M0_D3N

**U1C**

Pin	Signal
A5	Q0_LN0_RXP_I
B5	Q0_LN0_RXM_I
A4	Q0_LN1_RXP_I
B4	Q0_LN1_RXM_I
A2	Q0_LN2_RXP_I
B2	Q0_LN2_RXM_I
A1	Q0_LN3_RXP_I
B1	Q0_LN3_RXM_I
A3	Q0_REFCLKP_0
B3	Q0_REFCLKM_0

**U1D**

Pin	Signal
D3	VDDAQ0_0P9
D2	VDDAQ0
E3	VDDTQ0_0P9
D4	VDDHAQ0_1P8
G2	VDDHAQ0
E2	VCCIO1_VEFUSE_VDDP_VDDQP
F2	VCCIO1_VEFUSE_VDDP_VDDQP
G4	VDDAM_0P9
H5	VCCX_VCCLD0_VDDXM
J5	VCCX_VCCLD0_VDDXM
J4	VCCX_VCCLD0_VDDXM
K4	VDD12M_1P2

**U1E**

Pin	Signal
K9	VSS
H7	VSS
J7	VSS
K7	VSS
F7	VSS
H6	VSS
J6	VSS
D5	VSS
C5	VSS
C3	VSS
H2	VSS
H1	VSS
C1	VSS
D1	VSS
K5	VSS
F1	VSS
E1	VSS
G7	VSS
K8	NC1
F6	NC2
G1	NC3

**\*Configurable detection section**

**\*Configuration completed detection section**

**\*Configuration mode signal selection**

**\*Configuration reset section**

**\*JTAG download section**

**\*External Flash, used to store downloaded programs**

Name	Description	Min.	Max.
<b>FPGA Logic</b>			
V <sub>CC</sub>	Core voltage, LV	0.87V	1.03V
V <sub>CCIO</sub>	I/O Bank voltage	1.14V	3.465V
V <sub>CCX</sub> <sup>[1]</sup>	Auxiliary voltage	1.71V	3.465V
V <sub>CCLD0</sub>	Power supply voltage of internal LDO module that powers PLL and SRAM	1.14V	2.75V
V <sub>EFUSE</sub> <sup>[2]</sup>	Voltage required for eFuse writing	1.62V	1.98V
<b>Gigabit Transceiver</b>			
V <sub>DDHAQ*</sub>	Analog high power supply voltage	1.71V	1.89V
V <sub>DDAQ*</sub>	Analog core power supply voltage	0.87V	1.03V
V <sub>DDTQ*</sub>	Serdes transmitter power supply voltage	0.87V	1.03V
<b>MIPI</b>			
V <sub>DDAM</sub>	Analog core power supply voltage	0.855V	1.08V
V <sub>DDXM</sub>	Analog auxiliary power supply voltage	1.71V	3.465V
V <sub>DDDM</sub>	Digital core power supply voltage	0.87V	1.08V
V <sub>DD12M</sub>	MIPI LP power supply voltage	1.14V	1.32V
<b>PSRAM</b>			
V <sub>DDP</sub>	PSRAM power supply voltage	1.71V	1.89V
V <sub>DDQP</sub>	PSRAM data bus power supply voltage	1.71V	1.89V
<b>Note!</b>			
<sup>[1]</sup> When internal differential termination resistors are required, V <sub>CCX</sub> must be greater than or equal to 3V; the IO input-output F <sub>max</sub> is limited when V <sub>CCX</sub> =1.8V, and V <sub>CCX</sub> needs to be greater than or equal to 2.5V for input-output applications with F <sub>max</sub> greater than 600Mbps.			
<sup>[2]</sup> When V <sub>EFUSE</sub> is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			

</

## GW5ART-LV15CM90P

**U1A**

Pin	Signal	Bank
J3	QSPI_MISO	Bank 2
J2	QSPI_CCLK	Bank 2
J1	QSPI_MCS_N	Bank 2
K1	QSPI_MIS	Bank 2
K1	QSPI_MOSI	Bank 2
H1	IOB8A/READY	Bank 2
D6	IOL29A/DONE/LVDS	Bank 3
D5	IOL29B/RECONFIG_N/LVDS	Bank 3
D9	IOL31A/GCLK_5/MODE0/LVDS	Bank 3
D8	IOL31B/GCLK_5/MODE0/LVDS	Bank 3
A7	IOL33A/GCLK_4/LPLL_T_IN1/LPLL_T_FB0/CS0_B/OUT/SC/LVDS	Bank 3
A6	IOL33B/GCLK_4/LPLL_C_IN1/LPLL_C_FB0/CS1_B/SDA/LVDS	Bank 3
B6	IOL35A/D05/SSPI_CS_N/LVDS	Bank 3
A9	IOL20A/TCK/LVDS	Bank 4
B9	IOL20B/TMS/LVDS	Bank 4
B8	IOL22A/GCLK_7/Q0REF_T_IN0/SSPI_CLK/LVDS	Bank 4
C9	IOL22B/GCLK_7/Q0REF_C_IN0/RDWR_B/SQ/SSH/PCIE_HOST_RSTN/LVDS	Bank 4
C8	IOL24A/TDI/LVDS	Bank 4
C7	IOL24B/TDO/LVDS	Bank 4
D7	IOL36A/GCLK_6/LPLL_T_IN0/LPLL_T_FB1/Q0REF_T_IN1/D07/CLKHOLD_N/SSI3/LVDS	Bank 4
D7	IOL26B/GCLK_6/LPLL_C_IN0/LPLL_C_FB1/Q0REF_C_IN1/D07/SSPI_WPN/SSI2/LVDS	Bank 4

**U1B**

Pin	Signal
G9	M0_CKP
E9	M0_CKN
E8	M0_D0P
F9	M0_D0N
F8	M0_D1P
H9	M0_D1N
H8	M0_D2P
J9	M0_D2N
J8	M0_D3P
J8	M0_D3N

**U1C**

Pin	Signal
A5	Q0_LN0_RXP_I
B5	Q0_LN0_RXM_I
A4	Q0_LN1_RXP_I
B4	Q0_LN1_RXM_I
A2	Q0_LN2_RXP_I
B2	Q0_LN2_RXM_I
A1	Q0_LN3_RXP_I
B1	Q0_LN3_RXM_I
A3	Q0_REFCLKP_0
B3	Q0_REFCLKM_0

**U1D**

Pin	Signal
D3	VDDAQ0_0P9
D2	VDDAQ0_0P9
E3	VDDTQ0_0P9
D4	VDDHAQ0_1P8
G2	VDDHAQ0_1P8
E2	VDDHAQ0_1P8
F2	VDDHAQ0_1P8
G4	VDDAM_0P9
H5	VCCX_VCCLD0_VDDXM
J5	VCCX_VCCLD0_VDDXM
J4	VCCX_VCCLD0_VDDXM
K4	VDD12M_1P2

**U1E**

Pin	Signal
K9	VSS
H7	VSS
J7	VSS
K7	VSS
F7	VSS
H6	VSS
J6	VSS
D5	VSS
C5	VSS
C3	VSS
H2	VSS
H1	VSS
C1	VSS
D1	VSS
K5	VSS
F1	VSS
E1	VSS
G7	VSS
K8	NC1
F6	NC2
G1	NC3

**\*Configurable detection section**

**\*Configuration completed detection section**

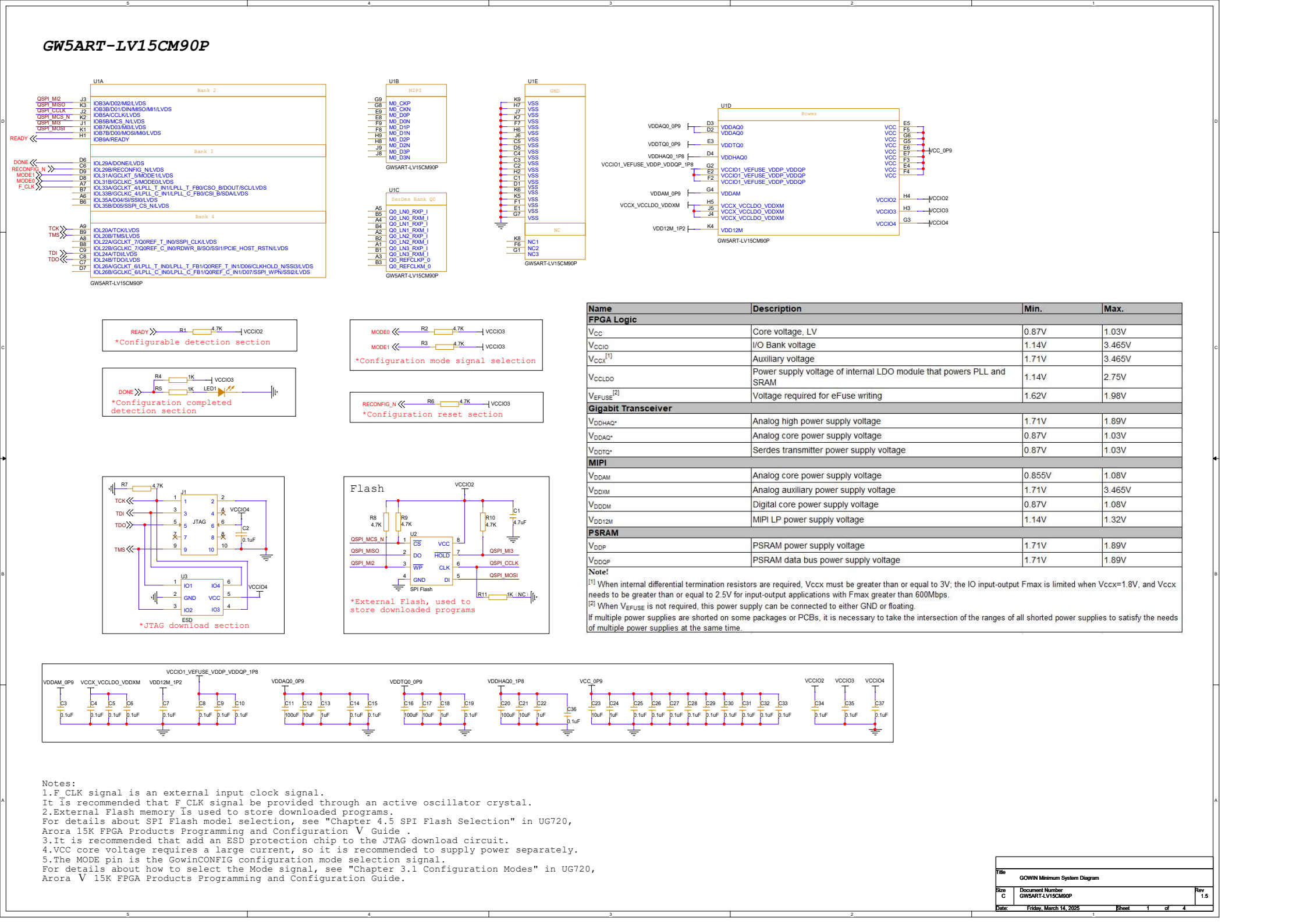
**\*Configuration mode signal selection**

**\*Configuration reset section**

**\*JTAG download section**

**\*External Flash, used to store downloaded programs**

Name	Description	Min.	Max.
<b>FPGA Logic</b>			
V <sub>CC</sub>	Core voltage, LV	0.87V	1.03V
V <sub>CCIO</sub>	I/O Bank voltage	1.14V	3.465V
V <sub>CCX</sub> <sup>[1]</sup>	Auxiliary voltage	1.71V	3.465V
V <sub>CCLD0</sub>	Power supply voltage of internal LDO module that powers PLL and SRAM	1.14V	2.75V
V <sub>EFUSE</sub> <sup>[2]</sup>	Voltage required for eFuse writing	1.62V	1.98V
<b>Gigabit Transceiver</b>			
V <sub>DDHAQ*</sub>	Analog high power supply voltage	1.71V	1.89V
V <sub>DDAQ*</sub>	Analog core power supply voltage	0.87V	1.03V
V <sub>DDTQ*</sub>	Serdes transmitter power supply voltage	0.87V	1.03V
<b>MIPI</b>			
V <sub>DDAM</sub>	Analog core power supply voltage	0.855V	1.08V
V <sub>DDXM</sub>	Analog auxiliary power supply voltage	1.71V	3.465V
V <sub>DDDM</sub>	Digital core power supply voltage	0.87V	1.08V
V <sub>DD12M</sub>	MIPI LP power supply voltage	1.14V	1.32V
<b>PSRAM</b>			
V <sub>DDP</sub>	PSRAM power supply voltage	1.71V	1.89V
V <sub>DDQP</sub>	PSRAM data bus power supply voltage	1.71V	1.89V
<b>Note!</b>			
<sup>[1]</sup> When internal differential termination resistors are required, V <sub>CCX</sub> must be greater than or equal to 3V; the IO input-output F <sub>max</sub> is limited when V <sub>CCX</sub> =1.8V, and V <sub>CCX</sub> needs to be greater than or equal to 2.5V for input-output applications with F <sub>max</sub> greater than 600Mbps.			
<sup>[2]</sup> When V <sub>EFUSE</sub> is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			



## GW5ART-LV15CM90P

The diagram shows the pinout for the GW5ART-LV15CM90P device, organized into five blocks: U1A, U1B, U1C, U1D, and U1E.

- U1A:** Contains pins for Bank 2, Bank 3, and Bank 4. Bank 2 pins include QSPI\_MISO, QSPI\_CCLK, QSPI\_MCS\_N, QSPI\_MIS, QSPI\_MOSI, QSPI\_READY, QSPI\_DONE, QSPI\_RECONF\_N, QSPI\_MODE0, QSPI\_MODE1, QSPI\_F\_CLK, TCK, TMS, TD0, and TD1. Bank 3 pins include IOL29A/DONE/LVDS, IOL29B/RECONFIG\_N/LVDS, IOL31A/GCLK\_5/MODE0/LVDS, IOL31B/GCLK\_5/MODE0/LVDS, IOL33A/GCLK\_4/LPLL\_T\_IN1/LPLL\_T\_FB0/CS0\_B/OUT/SC/LVDS, IOL33B/GCLK\_4/LPLL\_C\_IN1/LPLL\_C\_FB0/CS1\_B/SDA/LVDS, IOL35A/D05/SSPI\_CS\_N/LVDS, IOL20A/TCK/LVDS, IOL20B/TMS/LVDS, IOL22A/GCLK\_7/Q0REF\_T\_IN0/SSPI\_CLK/LVDS, IOL22B/GCLK\_7/Q0REF\_C\_IN0/RDWR\_B/SQ/SSH/PCIE\_HOST\_RSTN/LVDS, IOL24A/TDI/LVDS, IOL24B/TDO/LVDS, IOL26A/GCLK\_6/LPLL\_T\_IN0/LPLL\_T\_FB1/Q0REF\_T\_IN1/D07/CLKHOLD\_N/SSI3/LVDS, and IOL26B/GCLK\_6/LPLL\_C\_IN0/LPLL\_C\_FB1/Q0REF\_C\_IN1/D07/SSPI\_WPN/SSI2/LVDS.
- U1B:** Contains pins for Bank 2, Bank 3, and Bank 4. Bank 2 pins include QSPI\_MISO, QSPI\_CCLK, QSPI\_MCS\_N, QSPI\_MIS, QSPI\_MOSI, QSPI\_READY, QSPI\_DONE, QSPI\_RECONF\_N, QSPI\_MODE0, QSPI\_MODE1, QSPI\_F\_CLK, TCK, TMS, TD0, and TD1. Bank 3 pins include IOL29A/DONE/LVDS, IOL29B/RECONFIG\_N/LVDS, IOL31A/GCLK\_5/MODE0/LVDS, IOL31B/GCLK\_5/MODE0/LVDS, IOL33A/GCLK\_4/LPLL\_T\_IN1/LPLL\_T\_FB0/CS0\_B/OUT/SC/LVDS, IOL33B/GCLK\_4/LPLL\_C\_IN1/LPLL\_C\_FB0/CS1\_B/SDA/LVDS, IOL35A/D05/SSPI\_CS\_N/LVDS, IOL20A/TCK/LVDS, IOL20B/TMS/LVDS, IOL22A/GCLK\_7/Q0REF\_T\_IN0/SSPI\_CLK/LVDS, IOL22B/GCLK\_7/Q0REF\_C\_IN0/RDWR\_B/SQ/SSH/PCIE\_HOST\_RSTN/LVDS, IOL24A/TDI/LVDS, IOL24B/TDO/LVDS, IOL26A/GCLK\_6/LPLL\_T\_IN0/LPLL\_T\_FB1/Q0REF\_T\_IN1/D07/CLKHOLD\_N/SSI3/LVDS, and IOL26B/GCLK\_6/LPLL\_C\_IN0/LPLL\_C\_FB1/Q0REF\_C\_IN1/D07/SSPI\_WPN/SSI2/LVDS.
- U1C:** Contains pins for Bank 2, Bank 3, and Bank 4. Bank 2 pins include QSPI\_MISO, QSPI\_CCLK, QSPI\_MCS\_N, QSPI\_MIS, QSPI\_MOSI, QSPI\_READY, QSPI\_DONE, QSPI\_RECONF\_N, QSPI\_MODE0, QSPI\_MODE1, QSPI\_F\_CLK, TCK, TMS, TD0, and TD1. Bank 3 pins include IOL29A/DONE/LVDS, IOL29B/RECONFIG\_N/LVDS, IOL31A/GCLK\_5/MODE0/LVDS, IOL31B/GCLK\_5/MODE0/LVDS, IOL33A/GCLK\_4/LPLL\_T\_IN1/LPLL\_T\_FB0/CS0\_B/OUT/SC/LVDS, IOL33B/GCLK\_4/LPLL\_C\_IN1/LPLL\_C\_FB0/CS1\_B/SDA/LVDS, IOL35A/D05/SSPI\_CS\_N/LVDS, IOL20A/TCK/LVDS, IOL20B/TMS/LVDS, IOL22A/GCLK\_7/Q0REF\_T\_IN0/SSPI\_CLK/LVDS, IOL22B/GCLK\_7/Q0REF\_C\_IN0/RDWR\_B/SQ/SSH/PCIE\_HOST\_RSTN/LVDS, IOL24A/TDI/LVDS, IOL24B/TDO/LVDS, IOL26A/GCLK\_6/LPLL\_T\_IN0/LPLL\_T\_FB1/Q0REF\_T\_IN1/D07/CLKHOLD\_N/SSI3/LVDS, and IOL26B/GCLK\_6/LPLL\_C\_IN0/LPLL\_C\_FB1/Q0REF\_C\_IN1/D07/SSPI\_WPN/SSI2/LVDS.
- U1D:** Contains pins for Bank 2, Bank 3, and Bank 4. Bank 2 pins include QSPI\_MISO, QSPI\_CCLK, QSPI\_MCS\_N, QSPI\_MIS, QSPI\_MOSI, QSPI\_READY, QSPI\_DONE, QSPI\_RECONF\_N, QSPI\_MODE0, QSPI\_MODE1, QSPI\_F\_CLK, TCK, TMS, TD0, and TD1. Bank 3 pins include IOL29A/DONE/LVDS, IOL29B/RECONFIG\_N/LVDS, IOL31A/GCLK\_5/MODE0/LVDS, IOL31B/GCLK\_5/MODE0/LVDS, IOL33A/GCLK\_4/LPLL\_T\_IN1/LPLL\_T\_FB0/CS0\_B/OUT/SC/LVDS, IOL33B/GCLK\_4/LPLL\_C\_IN1/LPLL\_C\_FB0/CS1\_B/SDA/LVDS, IOL35A/D05/SSPI\_CS\_N/LVDS, IOL20A/TCK/LVDS, IOL20B/TMS/LVDS, IOL22A/GCLK\_7/Q0REF\_T\_IN0/SSPI\_CLK/LVDS, IOL22B/GCLK\_7/Q0REF\_C\_IN0/RDWR\_B/SQ/SSH/PCIE\_HOST\_RSTN/LVDS, IOL24A/TDI/LVDS, IOL24B/TDO/LVDS, IOL26A/GCLK\_6/LPLL\_T\_IN0/LPLL\_T\_FB1/Q0REF\_T\_IN1/D07/CLKHOLD\_N/SSI3/LVDS, and IOL26B/GCLK\_6/LPLL\_C\_IN0/LPLL\_C\_FB1/Q0REF\_C\_IN1/D07/SSPI\_WPN/SSI2/LVDS.
- U1E:** Contains pins for Bank 2, Bank 3, and Bank 4. Bank 2 pins include QSPI\_MISO, QSPI\_CCLK, QSPI\_MCS\_N, QSPI\_MIS, QSPI\_MOSI, QSPI\_READY, QSPI\_DONE, QSPI\_RECONF\_N, QSPI\_MODE0, QSPI\_MODE1, QSPI\_F\_CLK, TCK, TMS, TD0, and TD1. Bank 3 pins include IOL29A/DONE/LVDS, IOL29B/RECONFIG\_N/LVDS, IOL31A/GCLK\_5/MODE0/LVDS, IOL31B/GCLK\_5/MODE0/LVDS, IOL33A/GCLK\_4/LPLL\_T\_IN1/LPLL\_T\_FB0/CS0\_B/OUT/SC/LVDS, IOL33B/GCLK\_4/LPLL\_C\_IN1/LPLL\_C\_FB0/CS1\_B/SDA/LVDS, IOL35A/D05/SSPI\_CS\_N/LVDS, IOL20A/TCK/LVDS, IOL20B/TMS/LVDS, IOL22A/GCLK\_7/Q0REF\_T\_IN0/SSPI\_CLK/LVDS, IOL22B/GCLK\_7/Q0REF\_C\_IN0/RDWR\_B/SQ/SSH/PCIE\_HOST\_RSTN/LVDS, IOL24A/TDI/LVDS, IOL24B/TDO/LVDS, IOL26A/GCLK\_6/LPLL\_T\_IN0/LPLL\_T\_FB1/Q0REF\_T\_IN1/D07/CLKHOLD\_N/SSI3/LVDS, and IOL26B/GCLK\_6/LPLL\_C\_IN0/LPLL\_C\_FB1/Q0REF\_C\_IN1/D07/SSPI\_WPN/SSI2/LVDS.

Circuit diagram for the Configurable detection section. It shows a pull-up resistor R1 connected to VCCIO2 and a detection pin (READY) connected to ground through a 4.7K resistor.

**\*Configurable detection section**

Circuit diagram for the Configuration completed detection section. It shows a pull-up resistor R4 connected to VCCIO3 and a detection pin (DONE) connected to ground through a 1K resistor. A 1K resistor R5 is also connected to VCCIO3.

**\*Configuration completed detection section**

Circuit diagram for the Configuration mode signal selection section. It shows a pull-up resistor R2 connected to VCCIO3 and a detection pin (MODE0) connected to ground through a 4.7K resistor. A 4.7K resistor R3 is also connected to VCCIO3.

**\*Configuration mode signal selection**

Circuit diagram for the Configuration reset section. It shows a pull-up resistor R6 connected to VCCIO3 and a detection pin (RECONF\_N) connected to ground through a 4.7K resistor.

**\*Configuration reset section**

Circuit diagram for the JTAG download section. It shows a JTAG connector (J1) connected to the device pins. A pull-up resistor R7 is connected to VCCIO4. A 0.1uF capacitor C2 is connected to ground. A 4.7K resistor R8 is connected to VCCIO4.

**\*JTAG download section**

Circuit diagram for the Flash section. It shows a SPI Flash memory (U2) connected to the device pins. A pull-up resistor R9 is connected to VCCIO2. A 4.7K resistor R10 is connected to VCCIO2. A 4.7uF capacitor C1 is connected to ground. A 1K resistor R11 is connected to VCCIO2.

**\*External Flash, used to store downloaded programs**

Name	Description	Min.	Max.
<b>FPGA Logic</b>			
V <sub>CC</sub>	Core voltage, LV	0.87V	1.03V
V <sub>CCIO</sub>	I/O Bank voltage	1.14V	3.465V
V <sub>CCX</sub> <sup>[1]</sup>	Auxiliary voltage	1.71V	3.465V
V <sub>CCLD0</sub>	Power supply voltage of internal LDO module that powers PLL and SRAM	1.14V	2.75V
V <sub>EFUSE</sub> <sup>[2]</sup>	Voltage required for eFuse writing	1.62V	1.98V
<b>Gigabit Transceiver</b>			
V <sub>DDHAQ</sub> *	Analog high power supply voltage	1.71V	1.89V
V <sub>DDAQ</sub> *	Analog core power supply voltage	0.87V	1.03V
V <sub>DDTQ</sub> *	Serdes transmitter power supply voltage	0.87V	1.03V
<b>MIPI</b>			
V <sub>DDAM</sub>	Analog core power supply voltage	0.855V	1.08V
V <sub>DDXM</sub>	Analog auxiliary power supply voltage	1.71V	3.465V
V <sub>DDDM</sub>	Digital core power supply voltage	0.87V	1.08V
V <sub>DD12M</sub>	MIPI LP power supply voltage	1.14V	1.32V
<b>PSRAM</b>			
V <sub>DDP</sub>	PSRAM power supply voltage	1.71V	1.89V
V <sub>DDQP</sub>	PSRAM data bus power supply voltage	1.71V	1.89V
<b>Note!</b>			
<sup>[1]</sup> When internal differential termination resistors are required, V <sub>CCX</sub> must be greater			

## GW5ART-LV15CM90P

**U1A**

Pin	Signal	Bank
J3	QSPI_M2	Bank 2
K3	QSPI_MISO	Bank 2
J2	QSPI_CCLK	Bank 2
K2	QSPI_MCS_N	Bank 2
J1	QSPI_MIS	Bank 2
K1	QSPI_MOSI	Bank 2
H1	IOB8A/READY	Bank 2
D6	IOL29A/DONE/LVDS	Bank 3
C6	IOL29B/RECONFIG_N/LVDS	Bank 3
D9	IOL31A/GCLK_5/MODE0/LVDS	Bank 3
D8	IOL31B/GCLK_5/MODE0/LVDS	Bank 3
A7	IOL33A/GCLK_4/LPLL_T_IN1/LPLL_T_FB0/CS0_B/OUT/SC/LVDS	Bank 3
B7	IOL33B/GCLK_4/LPLL_C_IN1/LPLL_C_FB0/CS1_B/SDA/LVDS	Bank 3
A6	IOL35A/D05/SSPI_CS_N/LVDS	Bank 3
B6	IOL35B/D05/SSPI_CS_N/LVDS	Bank 3
A9	IOL20A/TCK/LVDS	Bank 4
B9	IOL20B/TMS/LVDS	Bank 4
A8	IOL22A/GCLK_7/Q0REF_T_IN0/SSPI_CLK/LVDS	Bank 4
B8	IOL22B/GCLK_7/Q0REF_C_IN0/RDWR_B/SQ/SSH/PCIE_HOST_RSTN/LVDS	Bank 4
C9	IOL24A/TDI/LVDS	Bank 4
D9	IOL24B/TDO/LVDS	Bank 4
C7	IOL26A/GCLK_6/LPLL_T_IN0/LPLL_T_FB1/Q0REF_T_IN1/D07/CLKHOLD_N/SSI3/LVDS	Bank 4
D7	IOL26B/GCLK_6/LPLL_C_IN0/LPLL_C_FB1/Q0REF_C_IN1/D07/SSPI_WPN/SSI2/LVDS	Bank 4

**U1B**

Pin	Signal
G9	M0_CKP
E9	M0_CKN
E8	M0_D0P
F9	M0_D0N
F8	M0_D1P
H9	M0_D1N
H8	M0_D2P
J9	M0_D2N
J8	M0_D3P
J7	M0_D3N

**U1C**

Pin	Signal
A5	Q0_LN0_RXP_I
B5	Q0_LN0_RXM_I
A4	Q0_LN1_RXP_I
B4	Q0_LN1_RXM_I
A2	Q0_LN2_RXP_I
B2	Q0_LN2_RXM_I
A1	Q0_LN3_RXP_I
B1	Q0_LN3_RXM_I
A3	Q0_REFCLKP_0
B3	Q0_REFCLKM_0

**U1E**

Pin	Signal
K9	VSS
H7	VSS
J7	VSS
K7	VSS
F7	VSS
H6	VSS
J6	VSS
D5	VSS
C5	VSS
C4	VSS
D3	VSS
C3	VSS
H2	VSS
H1	VSS
C1	VSS
D1	VSS
K6	VSS
F1	VSS
E1	VSS
G7	VSS
K8	NC1
F6	NC2
G1	NC3

**U1D**

Pin	Signal
D3	VDDAQ0_0P9
D2	VDDAQ0_0P9
E3	VDDTQ0_0P9
D4	VDDHAQ0_1P8
G2	VDDHAQ0_1P8
E2	VDDHAQ0_1P8
F2	VDDHAQ0_1P8
G4	VDDAM_0P9
H5	VCCX_VCCLD0_VDDXM
J5	VCCX_VCCLD0_VDDXM
J4	VCCX_VCCLD0_VDDXM
K4	VDD12M_1P2
E5	VCC
F5	VCC
G5	VCC
H5	VCC
E7	VCC
F7	VCC
E6	VCC
F6	VCC
E4	VCC
F4	VCC
H4	VCCIO2
H3	VCCIO3
G3	VCCIO4

**\*Configurable detection section**

**\*Configuration completed detection section**

**\*Configuration mode signal selection**

**\*Configuration reset section**

**\*JTAG download section**

**\*External Flash, used to store downloaded programs**

Name	Description	Min.	Max.
<b>FPGA Logic</b>			
V <sub>CC</sub>	Core voltage, LV	0.87V	1.03V
V <sub>CCIO</sub>	I/O Bank voltage	1.14V	3.465V
V <sub>CCX</sub> <sup>[1]</sup>	Auxiliary voltage	1.71V	3.465V
V <sub>CCLD0</sub>	Power supply voltage of internal LDO module that powers PLL and SRAM	1.14V	2.75V
V <sub>EFUSE</sub> <sup>[2]</sup>	Voltage required for eFuse writing	1.62V	1.98V
<b>Gigabit Transceiver</b>			
V <sub>DDHAQ*</sub>	Analog high power supply voltage	1.71V	1.89V
V <sub>DDAQ*</sub>	Analog core power supply voltage	0.87V	1.03V
V <sub>DDTQ*</sub>	Serdes transmitter power supply voltage	0.87V	1.03V
<b>MIPI</b>			
V <sub>DDAM</sub>	Analog core power supply voltage	0.855V	1.08V
V <sub>DDXM</sub>	Analog auxiliary power supply voltage	1.71V	3.465V
V <sub>DDDM</sub>	Digital core power supply voltage	0.87V	1.08V
V <sub>DD12M</sub>	MIPI LP power supply voltage	1.14V	1.32V
<b>PSRAM</b>			
V <sub>DDP</sub>	PSRAM power supply voltage	1.71V	1.89V
V <sub>DDQP</sub>	PSRAM data bus power supply voltage	1.71V	1.89V
<b>Note!</b>			

<sup>[1]</sup> When internal differential termination resistors are required, V<sub>CCX</sub> must be greater than or equal to 3V; the IO input-output F<sub>max</sub> is limited when V<sub>CCX</sub>=1.8V, and V<sub>CCX</sub> needs to be greater than or equal to 2.5V for input-output applications with F<sub>max</sub> greater than 600Mbps.

<sup>[2]</sup> When V<sub>EFUSE</sub> is not required, this power supply can be connected to either GND or floating.

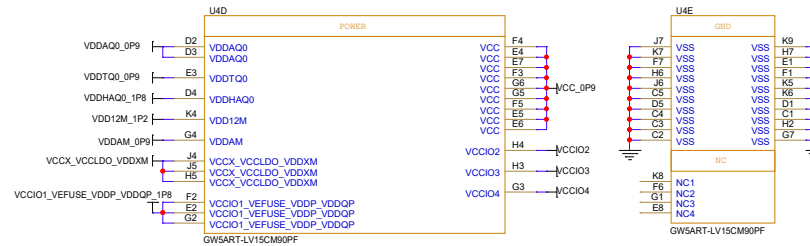
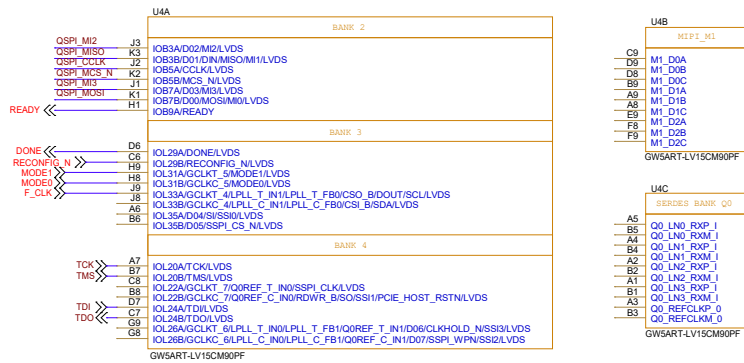
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.

Notes:

- 1.F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG720, Arora 15K FPGA Products Programming and Configuration V Guide.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG720, Arora V 15K FPGA Products Programming and Configuration Guide.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
C	GW5ART-LV15CM90P	1.5
Date:	Friday, March 14, 2025	Sheet 1 of 4

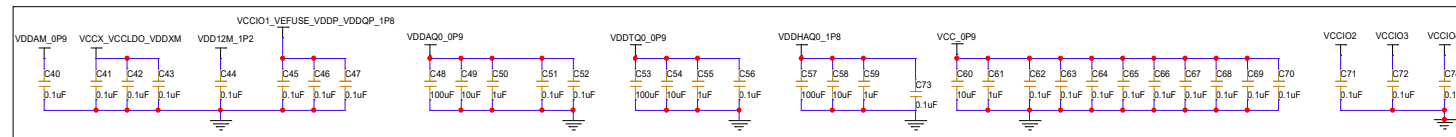
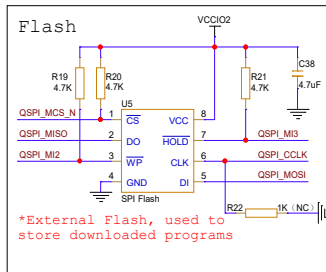
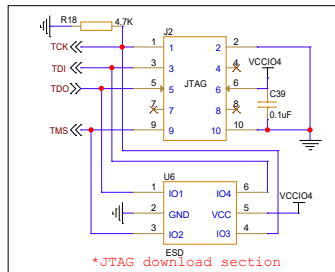
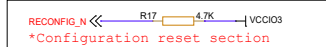
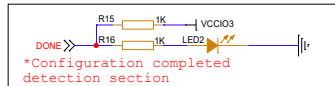
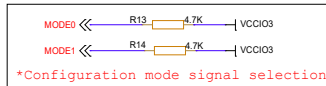
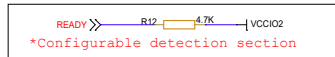
***GW5ART-LV15CM90PF***



Name	Description	Min.	Max.
<b>FPGA Logic</b>			
V <sub>CC</sub>	Core voltage, LV	0.87V	1.03V
V <sub>CCIO</sub>	I/O Bank voltage	1.14V	3.465V
V <sub>CCX</sub> <sup>[1]</sup>	Auxiliary voltage	1.71V	3.465V
V <sub>CCLD0</sub>	Power supply voltage of internal LDO module that powers PLL and SRAM	1.14V	2.75V
V <sub>EFUSE</sub> <sup>[2]</sup>	Voltage required for eFuse writing	1.62V	1.98V
<b>Gigabit Transceiver</b>			
V <sub>DDHAQ*</sub>	Analog high power supply voltage	1.71V	1.89V
V <sub>DDAQ*</sub>	Analog core power supply voltage	0.87V	1.03V
V <sub>DDTQ*</sub>	Serdes transmitter power supply voltage	0.87V	1.03V
<b>MIPI</b>			
V <sub>DDAM</sub>	Analog core power supply voltage	0.855V	1.08V
V <sub>DDXM</sub>	Analog auxiliary power supply voltage	1.71V	3.465V
V <sub>DDDM</sub>	Digital core power supply voltage	0.87V	1.08V
V <sub>DD12M</sub>	MIPI LP power supply voltage	1.14V	1.32V
<b>PSRAM</b>			
V <sub>DDP</sub>	PSRAM power supply voltage	1.71V	1.89V
V <sub>DDQP</sub>	PSRAM data bus power supply voltage	1.71V	1.89V

[1] When internal differential termination resistors are required, Vccx must be greater than or equal to 3V; the IO input-output Fmax is limited when Vccx=1.8V, and Vccx needs to be greater than or equal to 2.5V for input-output applications with Fmax greater than 600Mbps.

[2] When  $V_{EFUSE}$  is not required, this power supply can be connected to either GND or floating.  
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.

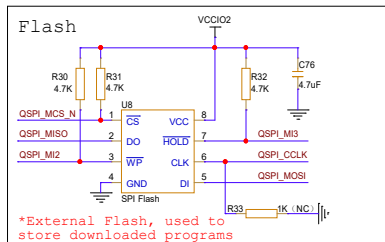
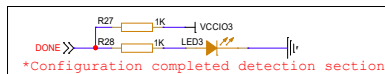
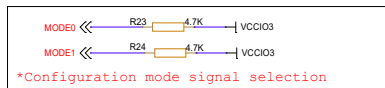
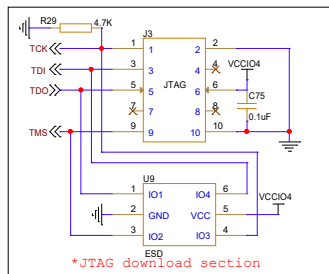
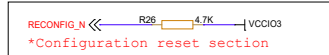
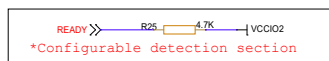
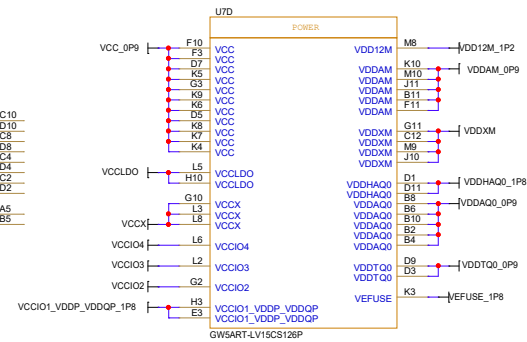
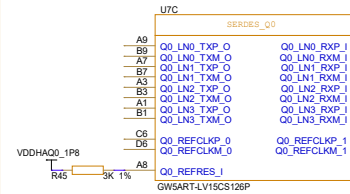
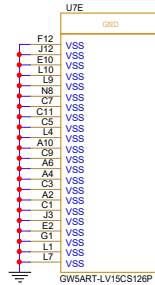
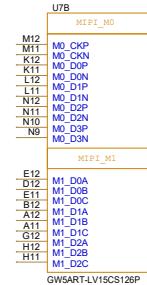
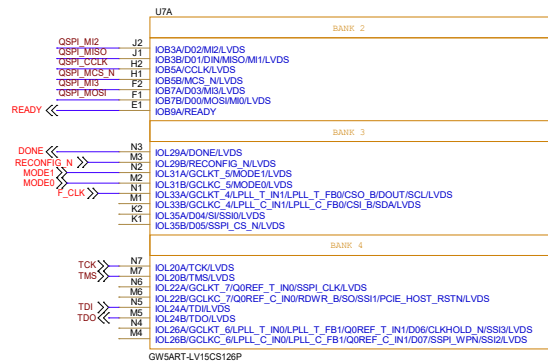


Notes:

1. F\_CLK signal is an external input clock signal.
- It is recommended that F\_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG720, Arora 15K FPGA Products Programming and Configuration V Guide.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. VCC core voltage requires a large current, so it is recommended to supply power separately.
5. The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG720, Arora V 15K FPGA Products Programming and Configuration Guide.

Title GOWIN Minimum System Diagram			
Size C	Document Number GWSART-LV15CM90PF		Rev 1.5
Part No.	Field No.	Sheet No.	Total No.

***GW5ART-LV15CS126P***

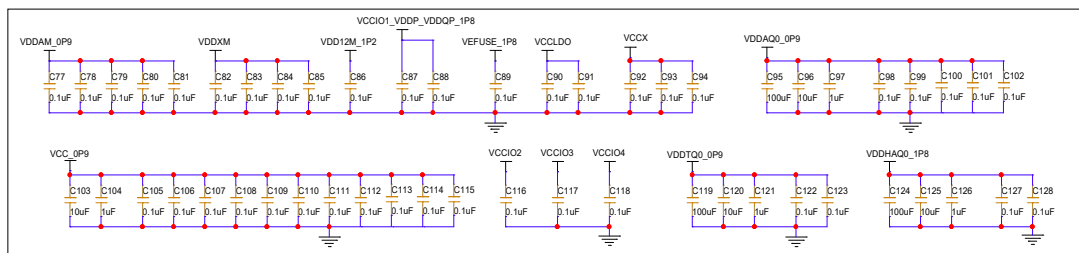


Name	Description	Min.	Max.
<b>FPGA Logic</b>			
V <sub>CC</sub>	Core voltage, LV	0.87V	1.03V
V <sub>CCIO</sub>	I/O Bank voltage	1.14V	3.465V
V <sub>CCX</sub> <sup>[1]</sup>	Auxiliary voltage	1.71V	3.465V
V <sub>CC_LDO</sub>	Power supply voltage of internal LDO module that powers PLL and SRAM	1.14V	2.75V
V <sub>EFUSE</sub> <sup>[2]</sup>	Voltage required for eFuse writing	1.62V	1.98V
<b>Gigabit Transceiver</b>			
V <sub>DDHAG*</sub>	Analog high power supply voltage	1.71V	1.89V
V <sub>DDAG*</sub>	Analog core power supply voltage	0.87V	1.03V
V <sub>DDTG*</sub>	Serdes Transmitter power supply voltage	0.87V	1.03V
<b>MIPI</b>			
V <sub>DDAM</sub>	Analog core power supply voltage	0.855V	1.08V
V <sub>DDIM</sub>	Analog auxiliary power supply voltage	1.71V	3.465V
V <sub>DDDM</sub>	Digital core power supply voltage	0.87V	1.08V
V <sub>DDI2M</sub>	MIPI LP power supply voltage	1.14V	1.32V
<b>PSRAM</b>			
V <sub>DDP</sub>	PSRAM power supply voltage	1.71V	1.89V
V <sub>DDQP</sub>	PSRAM data bus power supply voltage	1.71V	1.89V

[1] When internal differential termination resistors are required, Vccx must be greater than or equal to 3V; the IO input-output Fmax is limited when Vccx=1.8V, and Vccx needs to be greater than or equal to 2.5V for input-output applications with Fmax greater than 600Mbps.

[2] When  $V_{EFUSE}$  is not required, this power supply can be connected to either GND or floating.

If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.

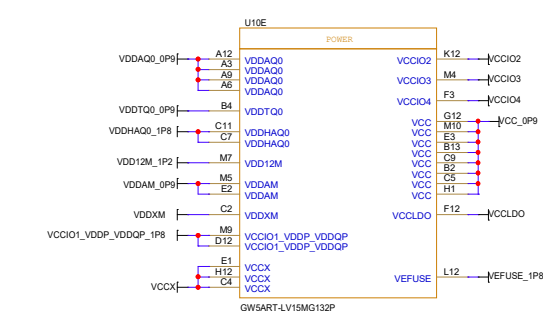
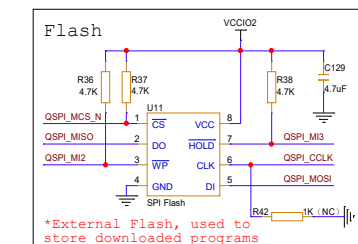
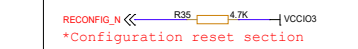
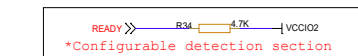
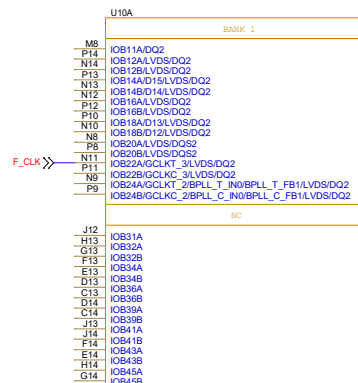
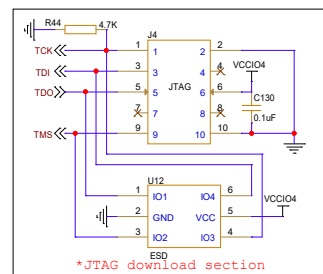
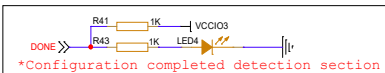
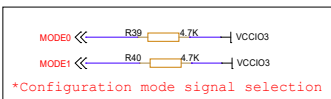
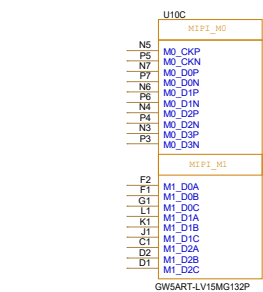
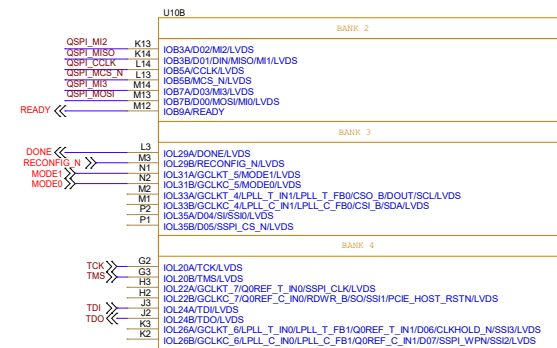


Notes:

1. F\_CLK signal is an external input clock signal.
- It is recommended that F\_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG720, Arora 15K FPGA Products Programming and Configuration V Guide.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. VCC core voltage requires a large current, so it is recommended to supply power separately.
5. The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG720, Arora V 15K FPGA Products Programming and Configuration Guide.

Title				
GOWIN Minimum System Diagram				
Size	Document Number			Rev
C	GWSART-LV1SCS126P			1.5
Date:	Friday, March 14, 2025	Sheet	3	of 4

***GW5ART-LV15MG132P***



Name	Description	Min.	Max.
<b>FPGA Logic</b>			
V <sub>CC</sub>	Core voltage, LV	0.87V	1.03V
V <sub>CCIO</sub>	I/O Bank voltage	1.14V	3.465V
V <sub>CCA</sub> <sup>[1]</sup>	Auxiliary voltage	1.71V	3.465V
V <sub>CCLD0</sub>	Power supply voltage of internal LDO module that powers PLL and SRAM	1.14V	2.75V
V <sub>EFUSE</sub> <sup>[2]</sup>	Voltage required for eFuse writing	1.62V	1.98V
<b>Gigabit Transceiver</b>			
V <sub>DDHAQ*</sub>	Analog high power supply voltage	1.71V	1.89V
V <sub>DDAQ*</sub>	Analog core power supply voltage	0.87V	1.03V
V <sub>DDTC*</sub>	Serdes transmitter power supply voltage	0.87V	1.03V
<b>MIPI</b>			
V <sub>DDAM</sub>	Analog core power supply voltage	0.855V	1.08V
V <sub>DDXM</sub>	Analog auxiliary power supply voltage	1.71V	3.465V
V <sub>DDDM</sub>	Digital core power supply voltage	0.87V	1.08V
V <sub>DD12M</sub>	MIPI LP power supply voltage	1.14V	1.32V
<b>PSRAM</b>			
V <sub>DDP</sub>	PSRAM power supply voltage	1.71V	1.89V
V <sub>DDQP</sub>	PSRAM data bus power supply voltage	1.71V	1.89V
<b>Note!</b>			
<sup>[1]</sup> When internal differential termination resistors are required, V <sub>CCA</sub> must be greater than or equal to 3V; the IO input-output F <sub>max</sub> is limited when V <sub>CCA</sub> =1.8V, and V <sub>CCA</sub> needs to be greater than or equal to 2.5V for input-output applications with F <sub>max</sub> greater than 600Mbps. <sup>[2]</sup> When V <sub>EFUSE</sub> is not required, this power supply can be connected to either GND or floating. If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the need of multiple power supplies at the same time.			

Notes:

- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.  
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG720, Arora 15K FPGA Products Programming and Configuration V Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.  
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG720, Arora V 15K FPGA Products Programming and Configuration Guide.