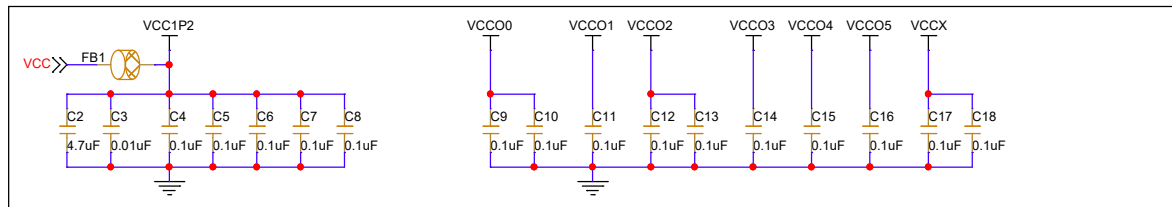
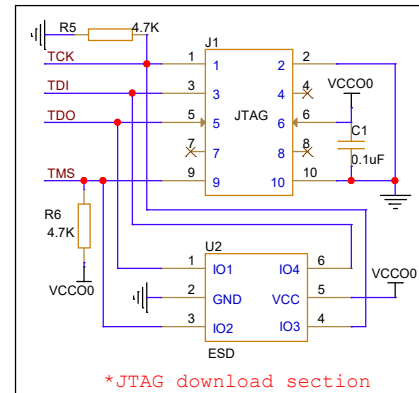
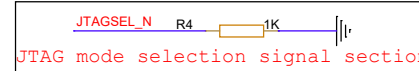
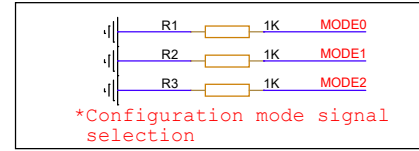
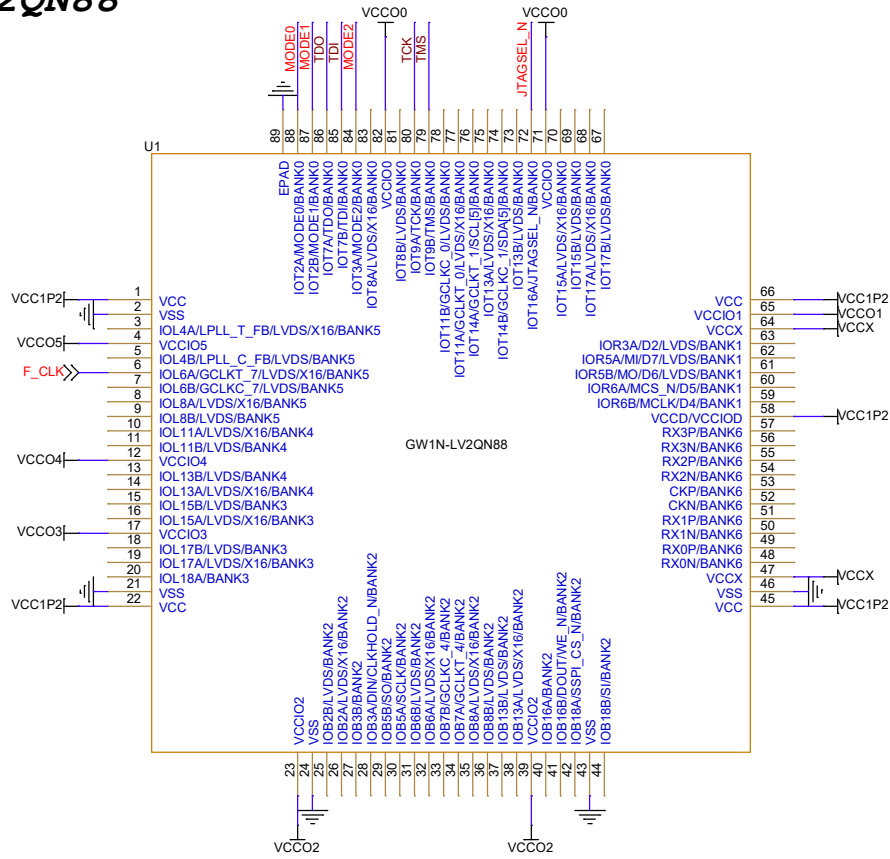


GW1N-LV2QN88

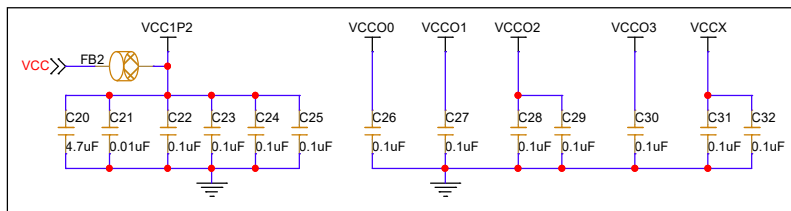
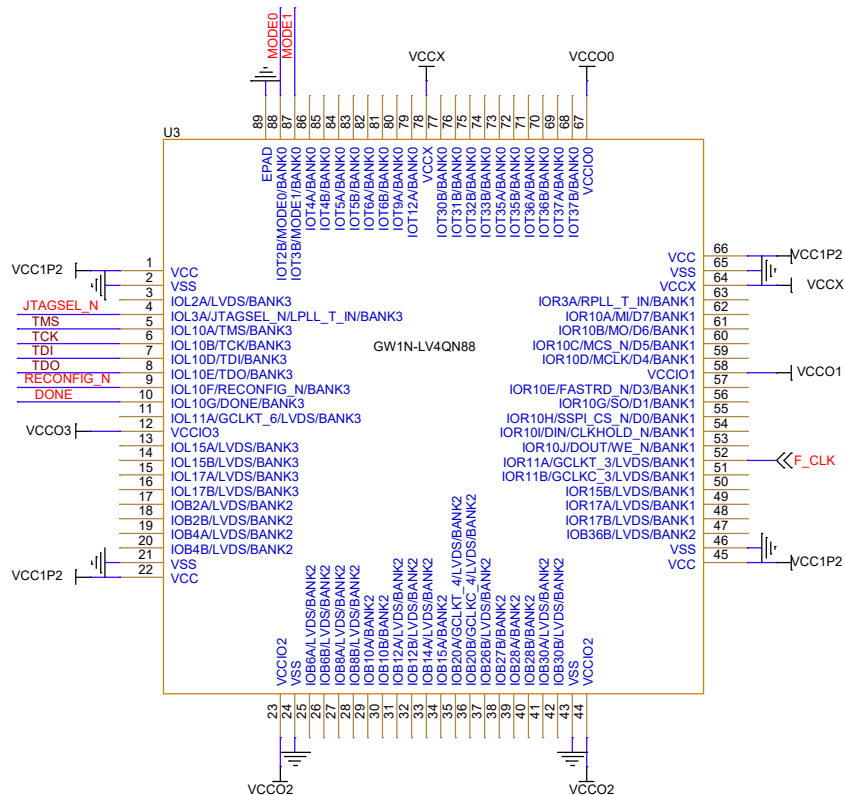


Notes:

- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

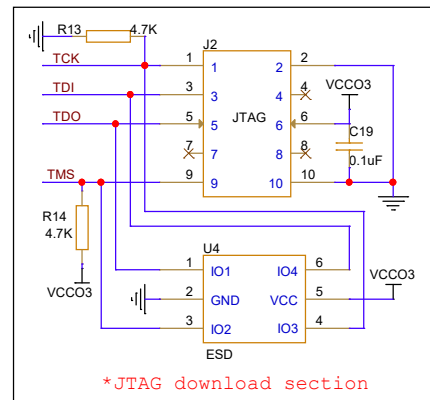
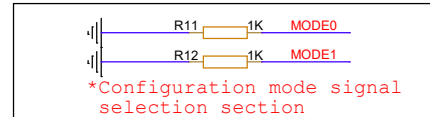
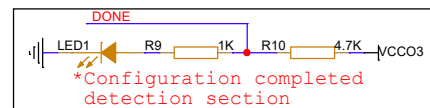
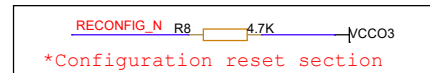
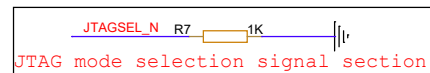
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GOWIN Minimum System Diagram			
Size B	Document Number GW1N-LV2QN88		Rev 3.5
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GW1N-LV4QN88



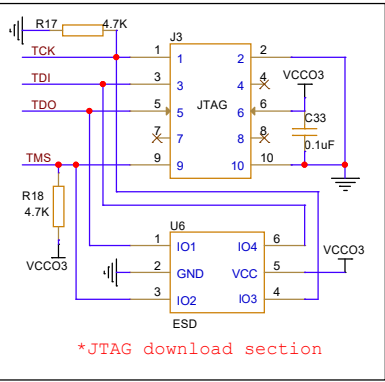
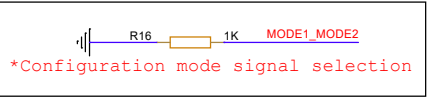
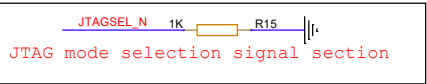
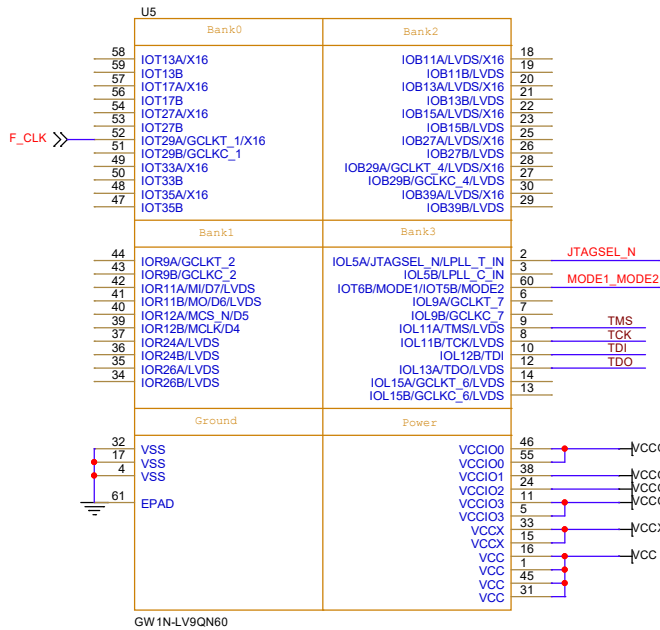
Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



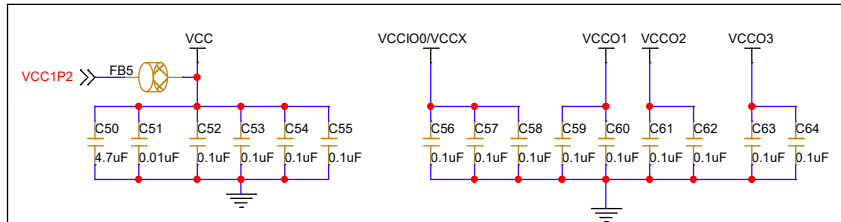
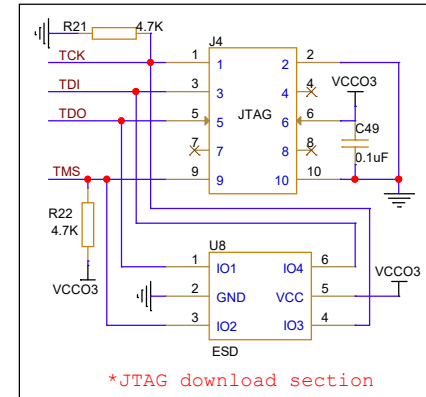
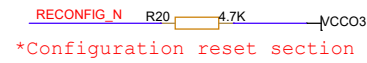
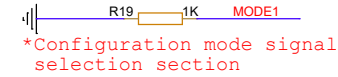
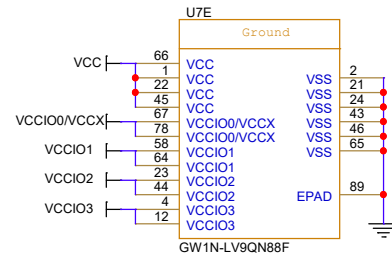
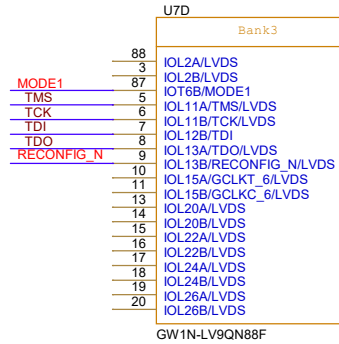
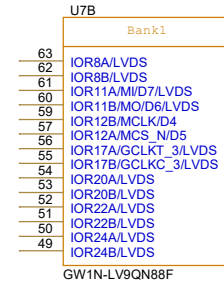
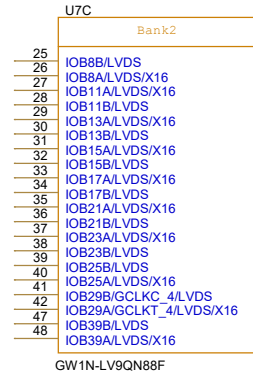
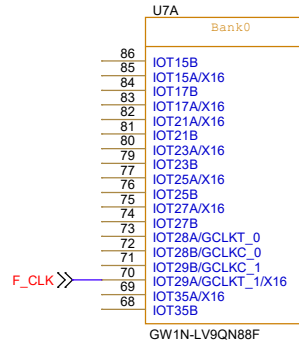
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Gowin FPGA-AOTOMOTIVE Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-LV4QN88	3.5
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GW1N-LV9QN60



- Notes:
- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
 - 3.It is recommended that add an ESD protection chip to the JTAG download circuit.

GW1N-LV9QN88F

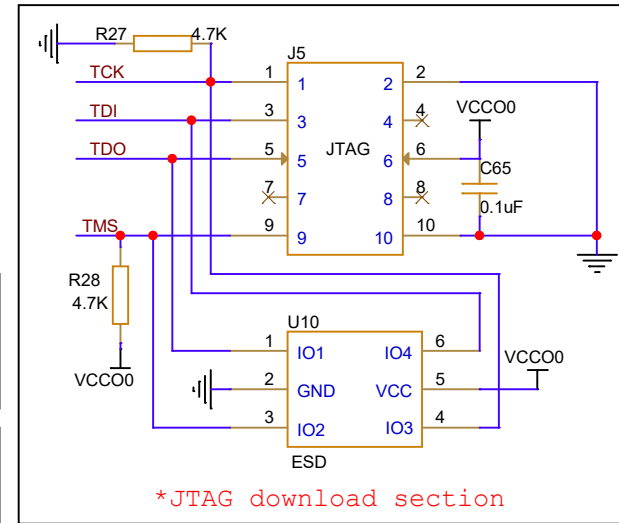
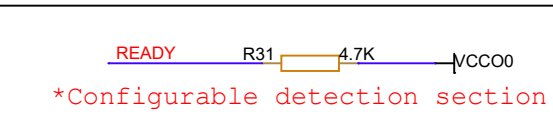
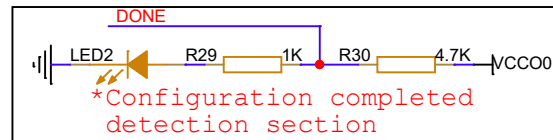
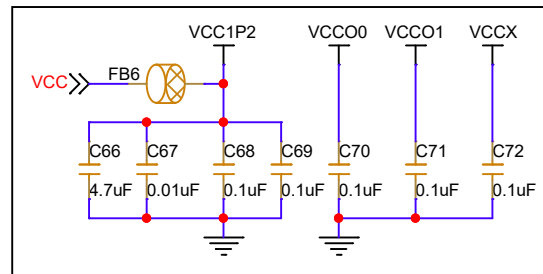
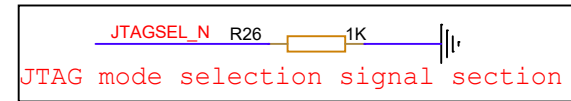
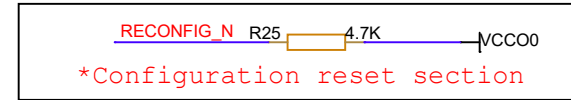
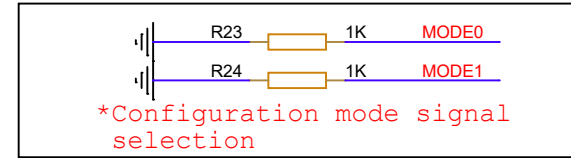
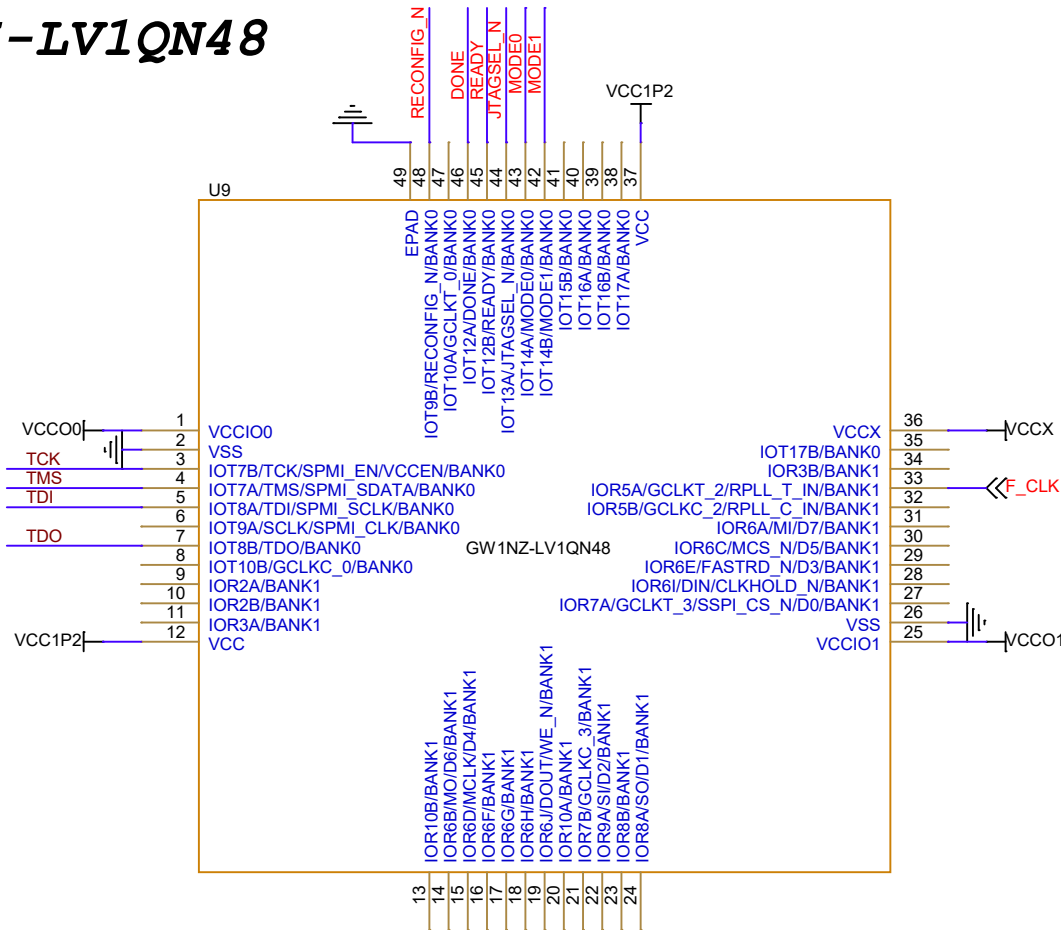


Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator circuit.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-LV9QN88F	3.5
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GW1NZ-LV1QN48



- Notes:
1. F_CLK signal is an external input clock signal. It is recommended that F_CLK signal be provided through an active oscillator crystal.
 2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
Gowin FPGA-AOTOMOTIVE Minimum System Diagram		
Size	Document Number	Rev
A4	GW1NZ-LV1QN48	3.5
Date:	Wednesday, May 07, 2025	Sheet 5 of 13

Notes:

1.F CLK signal is an external input clock signal.

It is recommended that F CLK signal be provided through an active oscillator crystal.

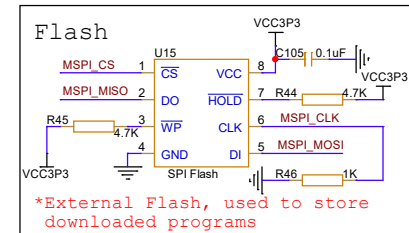
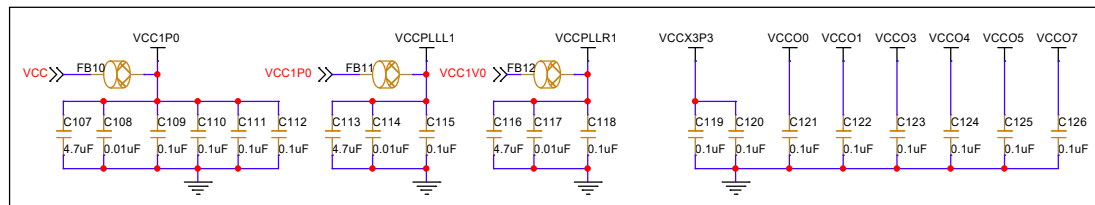
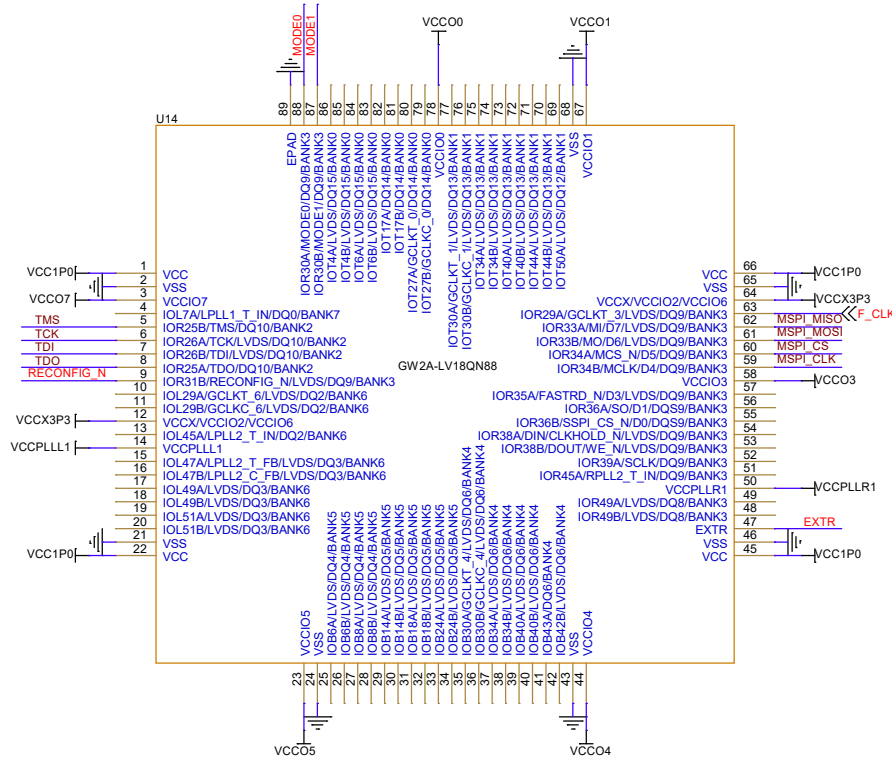
2. External Flash memory is used to store downloaded programs.

For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.

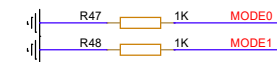
3.It is recommended that add an ESD protection chip to the JTAG download circuit.

4. The MSPI signal levels must match the Flash power supply voltage.

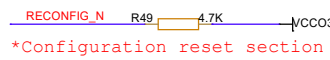
If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation



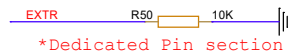
*External Flash, used to store downloaded programs



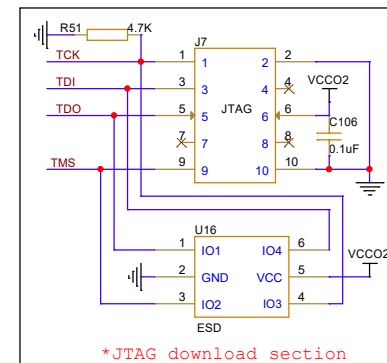
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*Configuration mode signal
  selection
```



*Configuration reset section



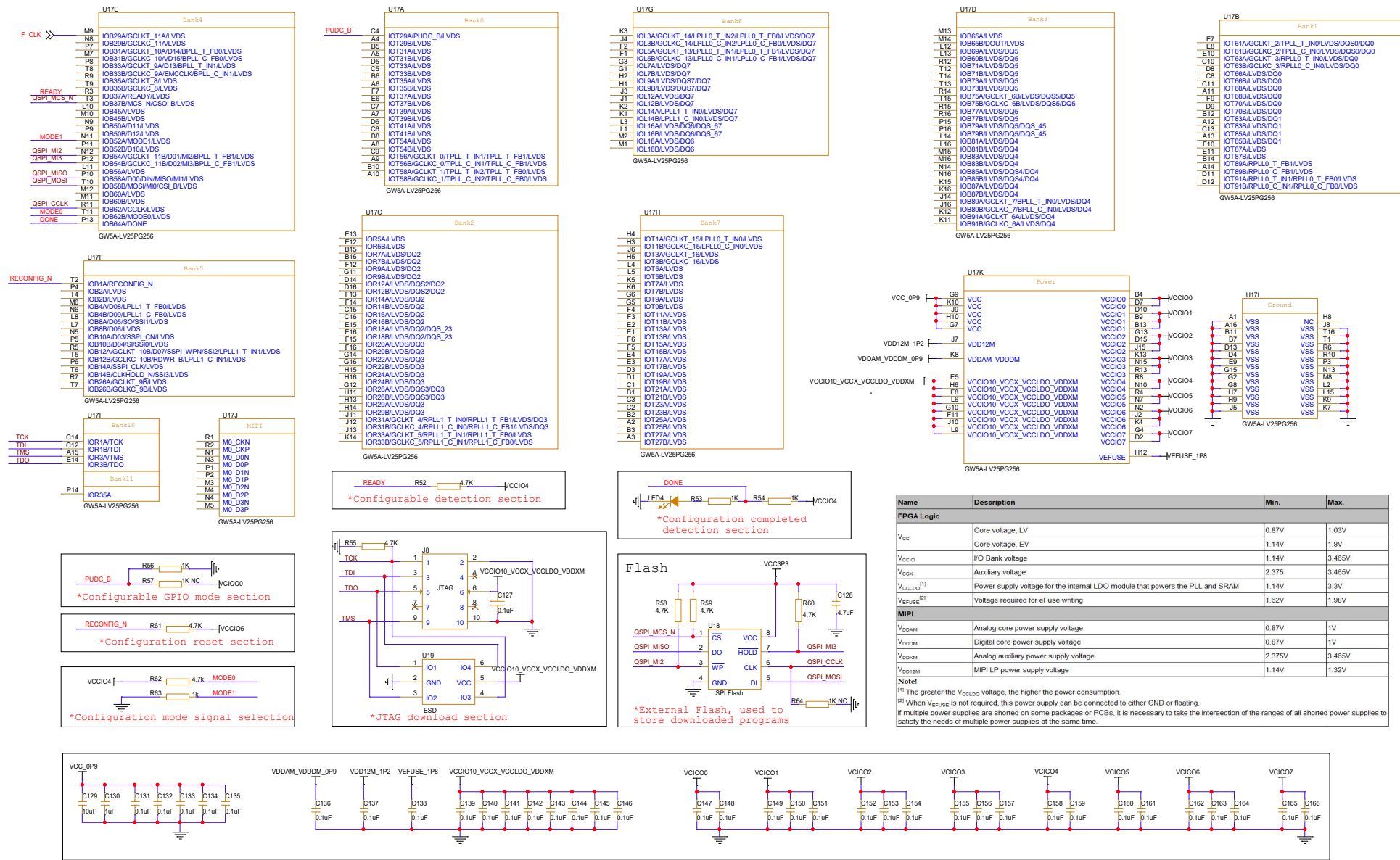
*Dedicated Pin section



*JTAG download section

Title			
Gowin FPGA-AOTOMOTIVE Minimum System Diagram			
Size	Document Number		Rev
A3	GW2A-LV18QN88F		3.5
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GW5A-LV25PG256

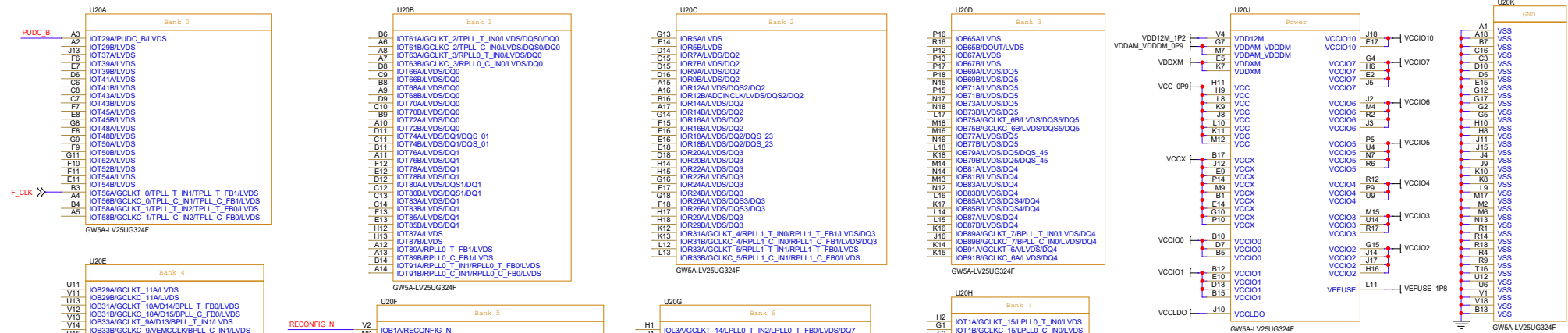


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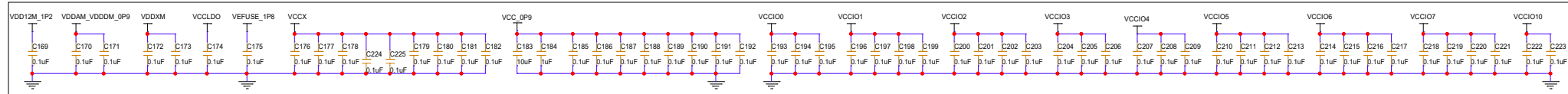
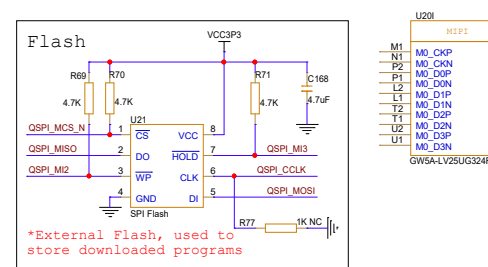
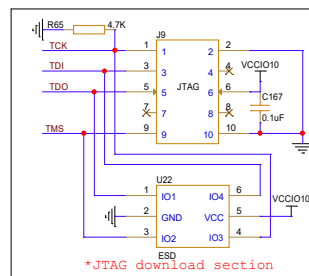
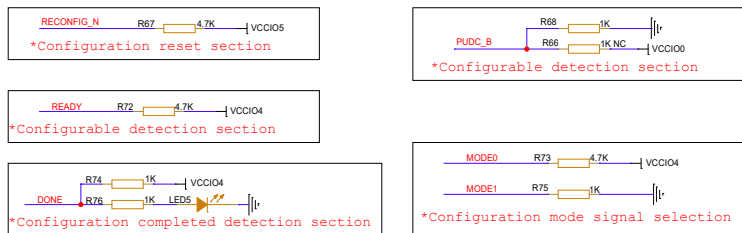
- 1.F. CLK signal is an external input clock signal.
- It is recommended that F. CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.
- If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
V _{CCIO}	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCX}	Auxiliary voltage	2.375	3.465V
V _{CCLOD} ^[1]	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{EFUSE} ^[2]	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V _{DDAM}	Analog core power supply voltage	0.87V	1V
V _{DDDM}	Digital core power supply voltage	0.87V	1V
V _{DDXM}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{DDIM}	MIPI LP power supply voltage	1.14V	1.32V
Note!			
[1] The greater the V _{CCLOD} voltage, the higher the power consumption.			
[2] When V _{EFUSE} is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			

GW5A-LV25UG324F



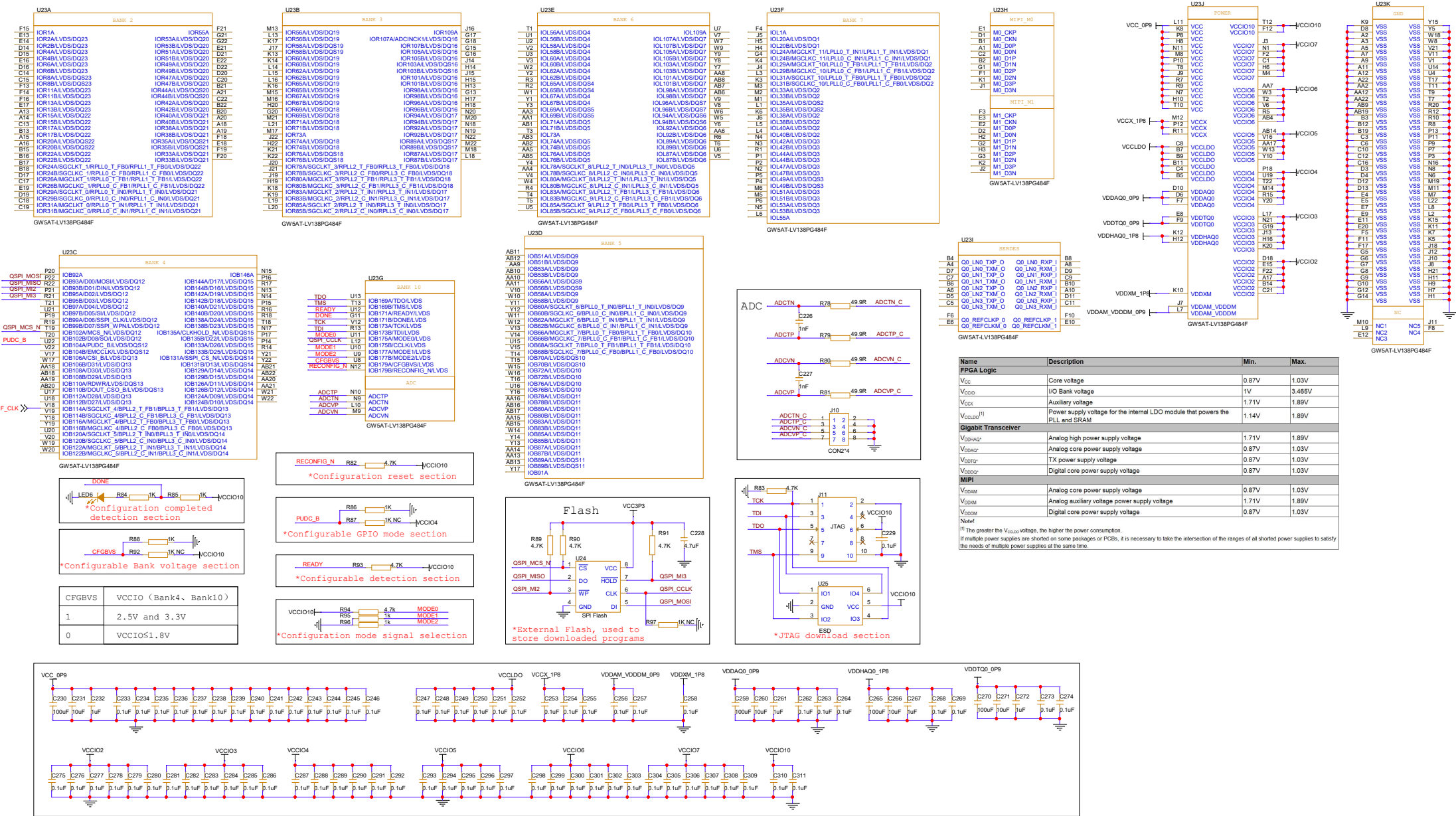
Name	Description	Min.	Max.
FPGA Logic			
V_{CC}	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V_{CCIO}	I/O Bank voltage	1.14V	3.465V
V_{CCA}	Auxiliary voltage	2.37V	3.465V
$V_{CCLO}^{[1]}$	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
$V_{FUSE}^{[2]}$	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V_{DDAM}	Analog core power supply voltage	0.87V	1V
V_{DDDM}	Digital core power supply voltage	0.87V	1V
V_{DDIM}	Analog auxiliary power supply voltage	2.375V	3.465V
V_{DDIM2}	MIPI LP power supply voltage	1.14V	1.32V
Note!			
[1] The greater the V_{CCLO} voltage, the higher the power consumption.			
[2] When V_{FUSE} is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			



Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 6.The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage,
a level shifter is required for voltage translation.

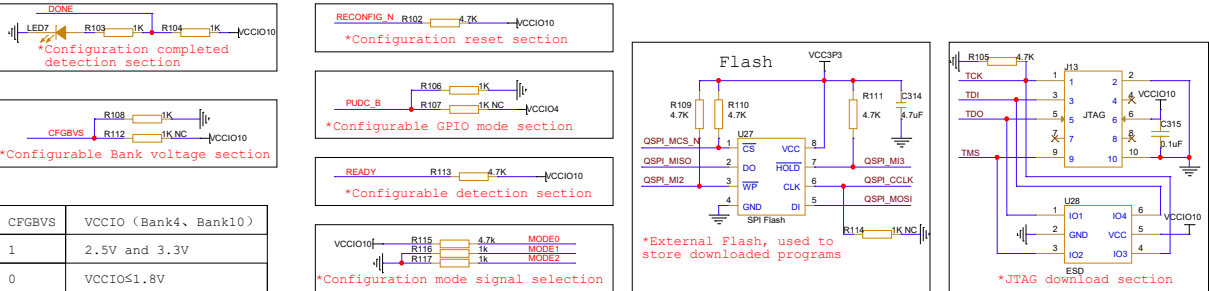
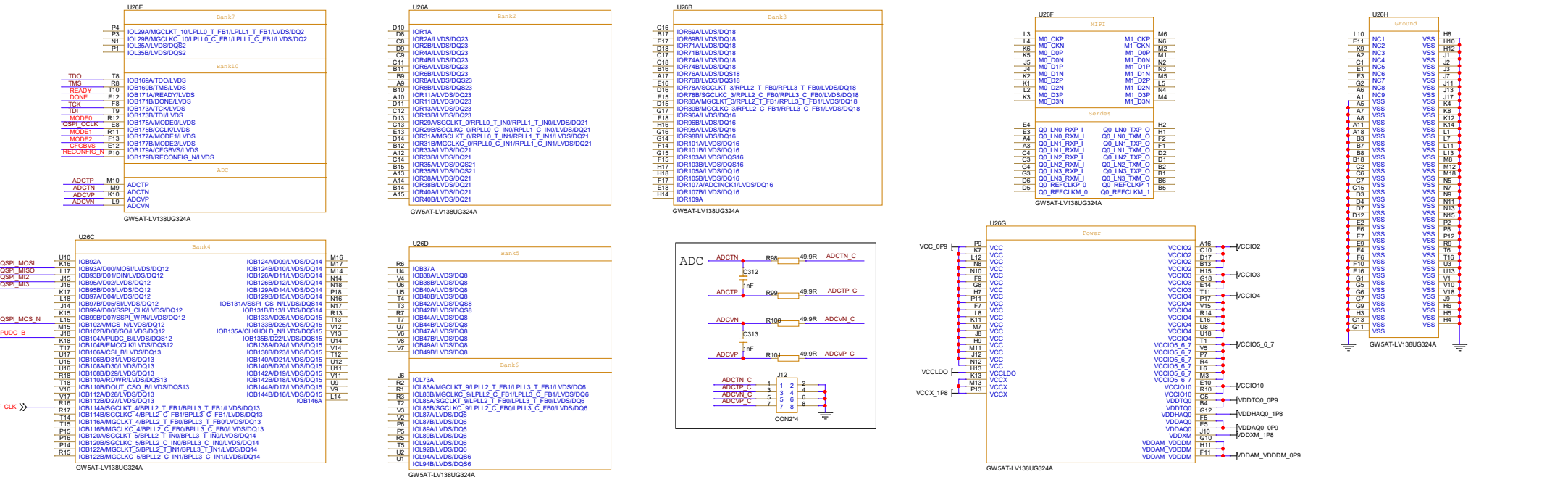
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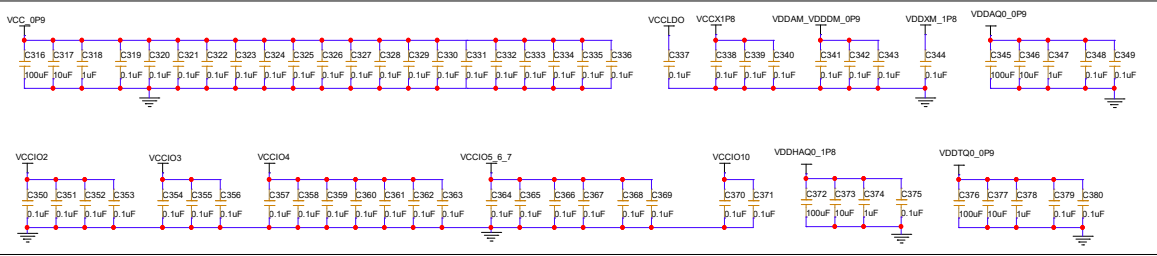
Notes:

1. F.CLK signal is an external input clock signal. It is recommended that F.CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG704, Arora V FPGA Products Programming and Configuration Guide.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. VCC core voltage requires a large current, so it is recommended to supply power separately.
5. The MODE pin is the GowinCONFIG configuration mode selection signal. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, Arora V FPGA Products Programming and Configuration Guide.
6. The MSPI signal levels must match the Flash power supply voltage. If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

GW5AT-LV138UG324A



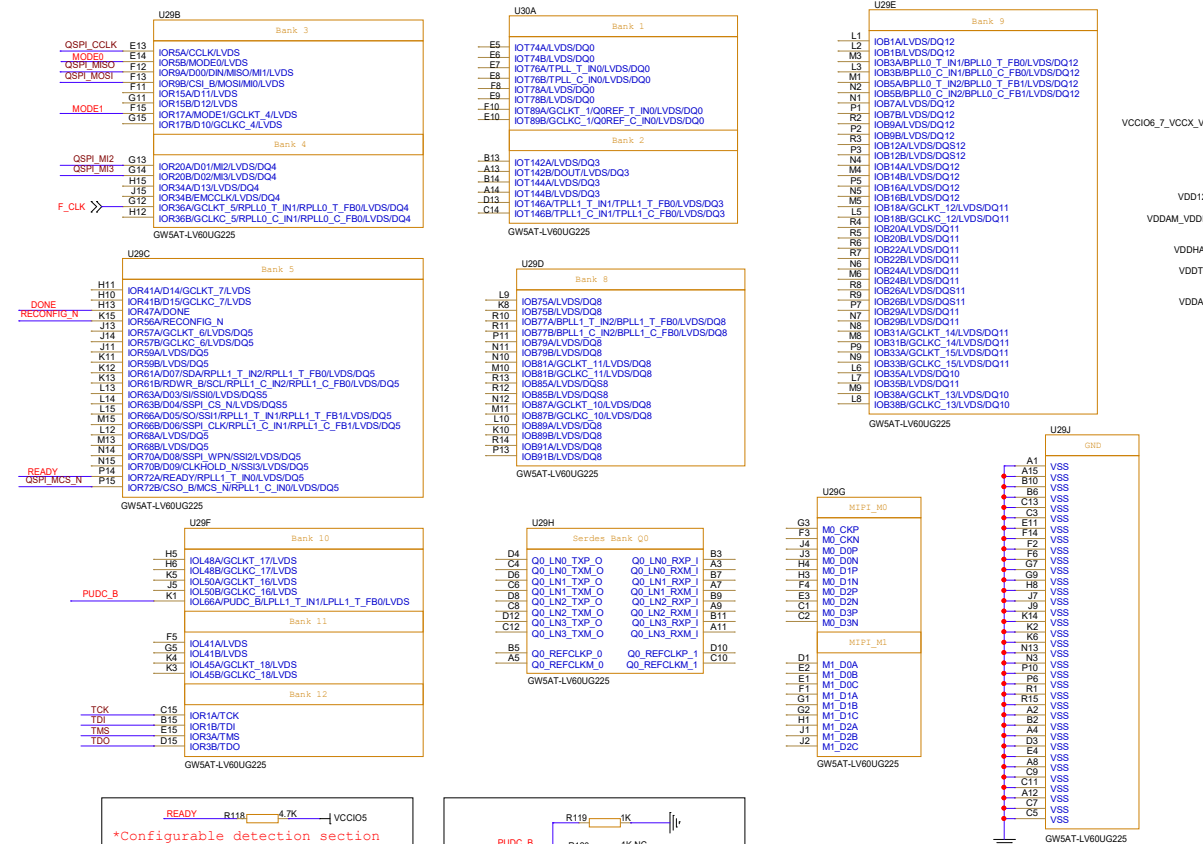
Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage	0.87V	1.03V
V _{CCIO}	I/O Bank voltage	1V	3.465V
V _{CCX}	Auxiliary voltage	1.71V	1.89V
V _{CCIO10} ⁽¹⁾	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	1.89V
Gigabit Transceiver			
V _{DDHAQ2}	Analog high power supply voltage	1.71V	1.89V
V _{DDHAQ2}	Analog core power supply voltage	0.87V	1.03V
V _{DDTQ2}	TX power supply voltage	0.87V	1.03V
V _{DDDO2}	Digital core power supply voltage	0.87V	1.03V
MIPI			
V _{DDAM}	Analog core power supply voltage	0.87V	1.03V
V _{DDAM}	Analog auxiliary voltage power supply voltage	1.71V	1.89V
V _{DDOM}	Digital core power supply voltage	0.87V	1.03V
Note!			
⁽¹⁾ The greater the V _{CCIO10} voltage, the higher the power consumption.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			



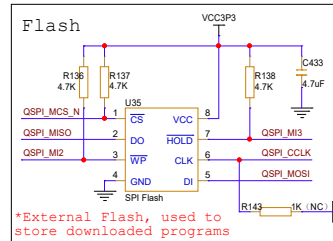
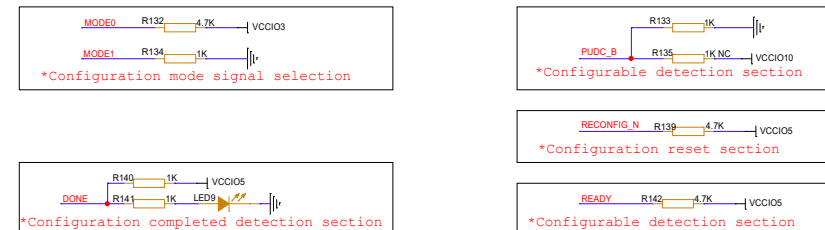
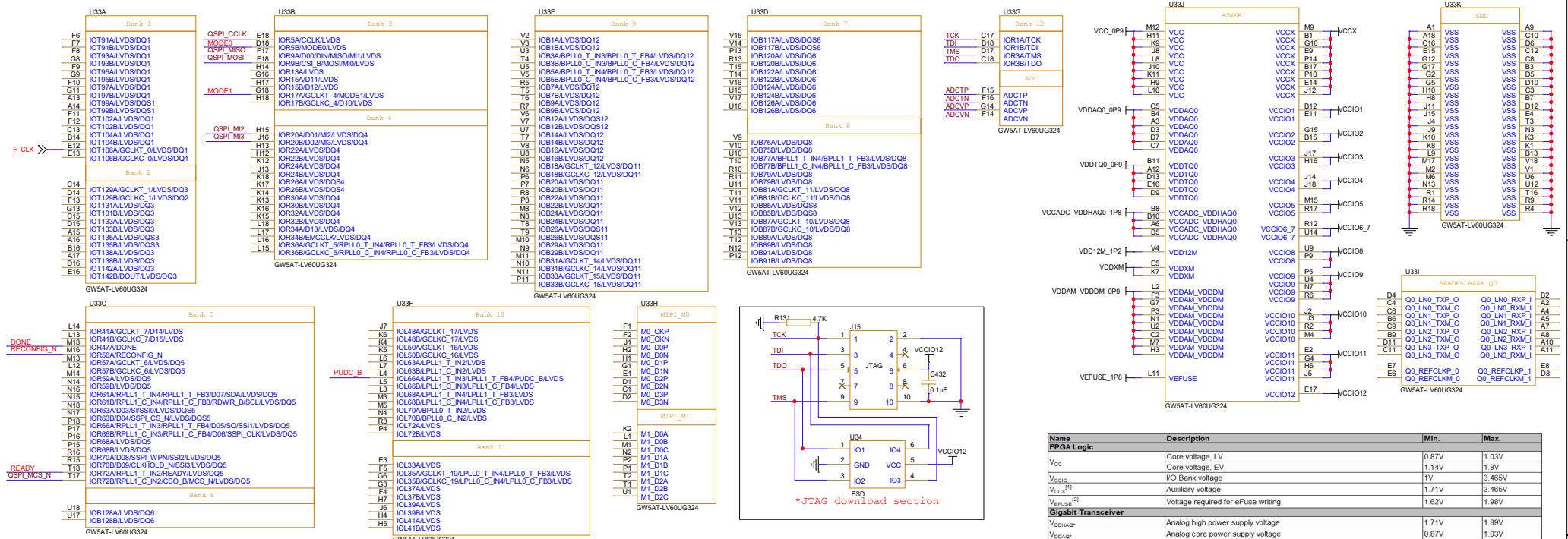
Notes:

- 1.F_CLK signal is an external input clock signal.
- It is recommended that F_CLK signal be provided through an active oscillator crystal.
- External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG704, Arora V FPGA Products Programming and Configuration Guide.
- It is recommended that add an ESD protection chip to the JTAG download circuit.
- VCC core voltage requires a large current, so it is recommended to supply power separately.
- The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, Arora V FPGA Products Programming and Configuration Guide.
- The MSPI signal levels must match the Flash power supply voltage.
- If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

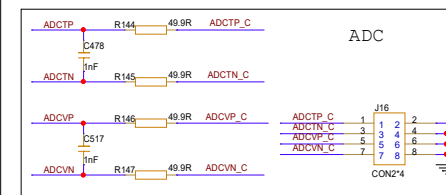
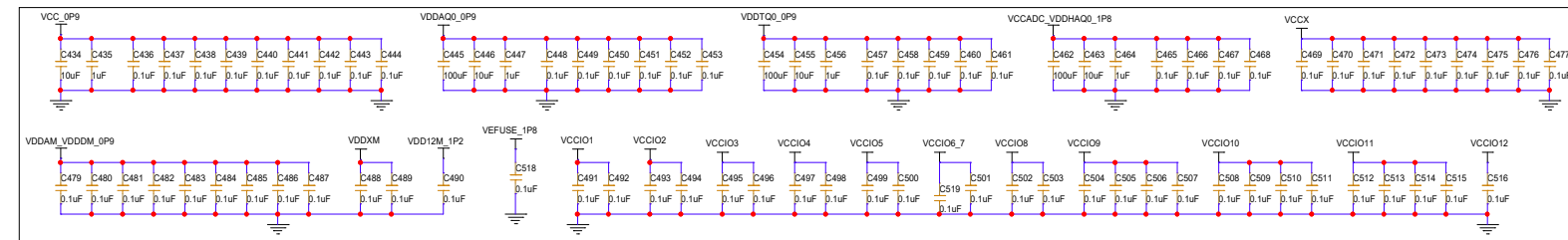
GW5AT-1V60UG225



GW5AT-LV60UG324



Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
V _{CCIO}	Core voltage, ECVs	1.14V	1.8V
V _{CCIO} ^[1]	I/O Bank voltage	1V	3.465V
V _{CCIO} ^[2]	Auxiliary voltage	1.71V	3.465V
V _{EPUSE}	Voltage required for eFuse writing	1.62V	1.98V
Gigabit Transceiver			
V _{DDH24V}	Analog high power supply voltage	1.71V	1.89V
V _{DDIO24V}	Analog core power supply voltage	0.87V	1.03V
V _{DDIO24V}	TX power supply voltage	0.87V	1.03V
V _{DDIO24V}	Digital power supply voltage	0.87V	1.03V
MIPI			
V _{DDH24V}	Analog core power supply voltage	0.87V	1.08V
V _{DDH24V}	Analog auxiliary power supply voltage	1.71V	3.465V
V _{DDH24V}	Digital power supply voltage	0.87V	1.08V
V _{DDH24V}	MIPI LP power supply voltage	1.14V	1.32V
ADC			
V _{CCAGE}	ADC power supply voltage	1.62V	1.98V
V _{REFH}	ADC reference voltage	0V	0V
V _{REFP}	ADC reference voltage	0V	1.25V
Note			
^[1] When internal differential termination resistors are required, V _{CCIO} must be greater than or equal to 3V; the IO input-output F _{max} is limited when V _{CCIO} =1.8V, and V _{CCIO} needs to be greater than or equal to 2.5V for input-output applications with F _{max} greater than 600Mbps. ^[2] When V _{EPUSE} is not required, this power supply can be connected to either GND or floating. If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			



Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F.CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage,
a level shifter is required for voltage translation.

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