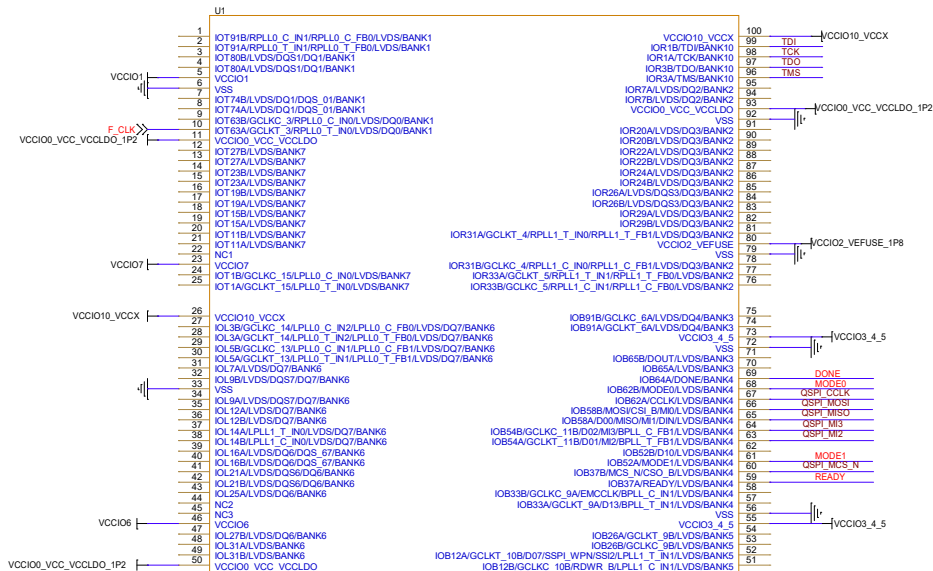
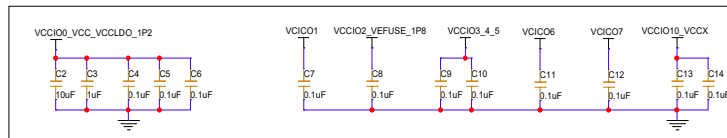


GW5A-EV25LQ100



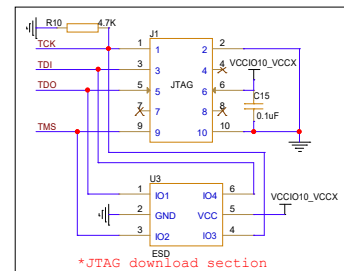
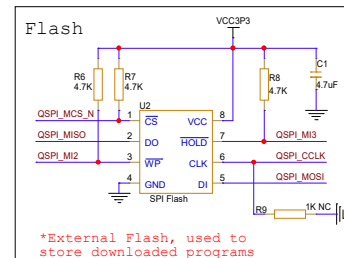
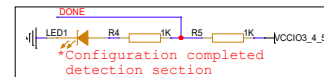
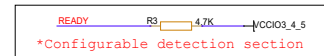
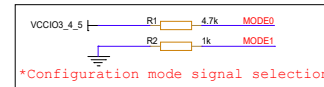
GW5A-EV25LQ100



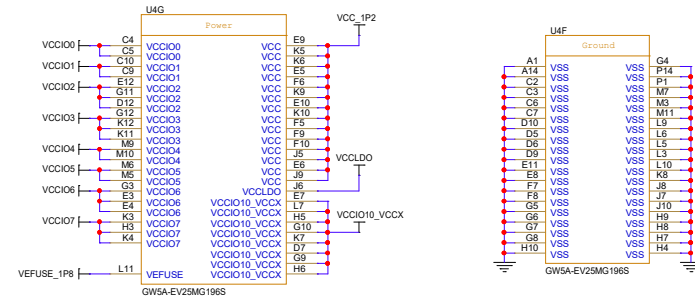
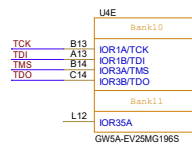
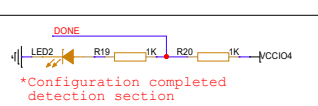
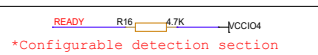
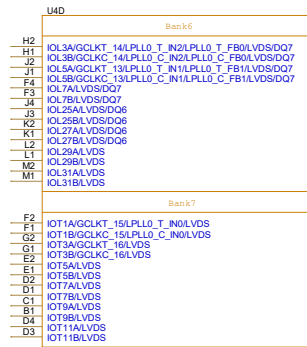
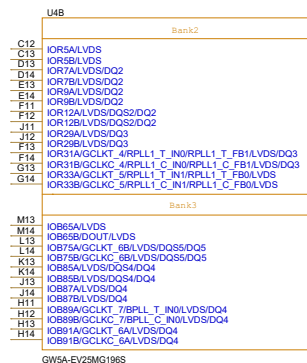
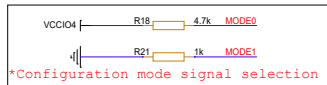
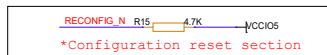
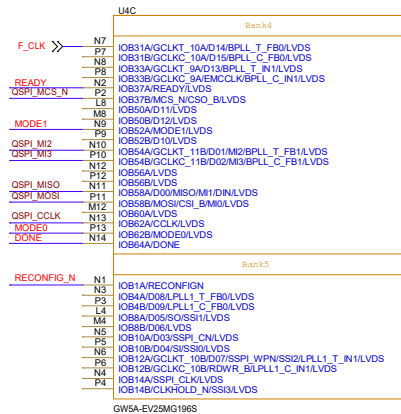
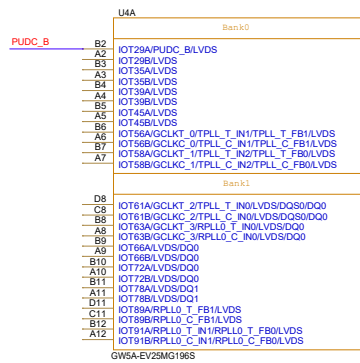
Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCAUX}	Auxiliary voltage	2.375	3.465V
V _{CCIOIO} ⁽¹⁾	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{APURST} ⁽²⁾	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V _{DDAH}	Analog core power supply voltage	0.87V	1V
V _{DDDM}	Digital core power supply voltage	0.87V	1V
V _{DDIHA}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{DDI2M}	MIPI LP power supply voltage	1.14V	1.32V
Note:			
⁽¹⁾ The greater the V _{CCIOIO} voltage, the higher the power consumption.			
⁽²⁾ When V _{CCIOIO} is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of all shorted power supplies as the minimum voltage.			

Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 6.The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage,
a level shifter is required for voltage translation.



GW5A-EV25MG196S

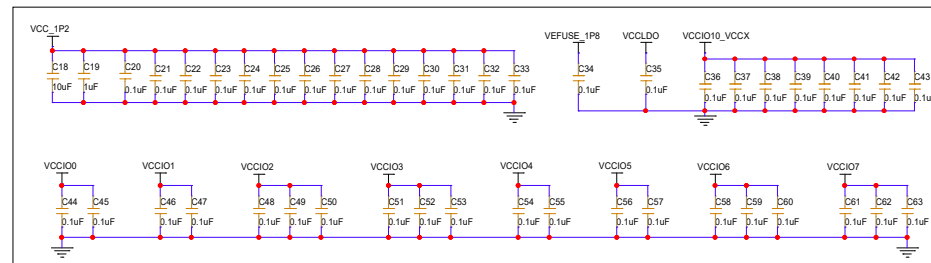
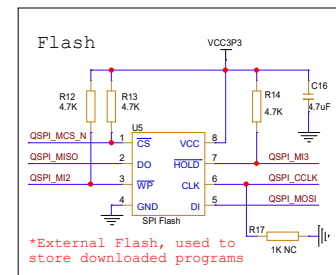
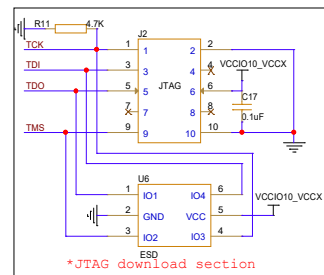


Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.6V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCAUX}	Auxiliary voltage	2.375	3.465V
V _{CEESDIO} ⁽¹⁾	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{FUSEB} ⁽²⁾	Voltage required for eFuse writing	1.62V	1.96V
MIPI			
V _{CCDM}	Analog core power supply voltage	0.87V	1V
V _{DDDM}	Digital core power supply voltage	0.87V	1V
V _{DDIM}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{DD12N}	MIPI LP power supply voltage	1.14V	1.32V

Note!
(1) The greater the V_{CCQDQ} voltage, the higher the power consumption.

^[2] When V_{EFGUE} is not required, this power supply can be connected to either GND or floating.

If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.



Notes:

1.F CLK signal is an external input clock signal.

It is recommended that F CLK signal be provided through an active oscillator crystal.

2. External Flash memory is used to store downloaded programs.

For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .

3. It is recommended that add an ESD protection chip to the JTAG download circuit.

4.VCC core voltage requires a large current, so it is recommended to supply power separately.

5. The MODE pin is the GowinCONFIG configuration mode selection signal.

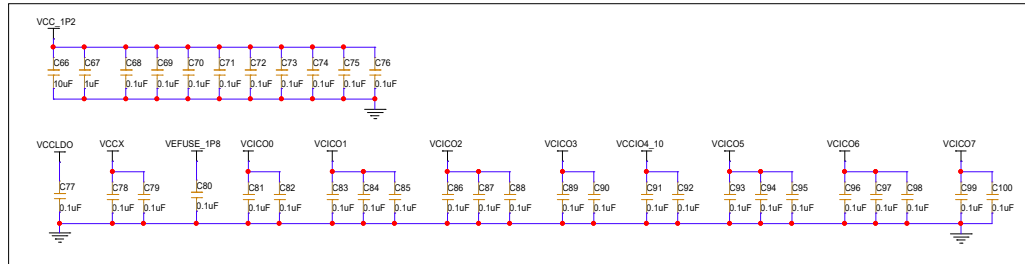
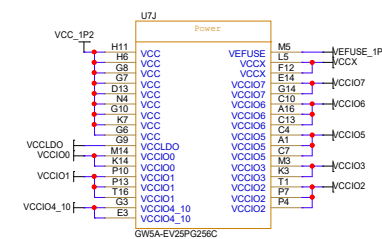
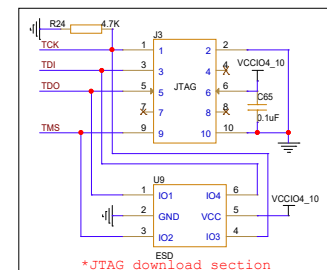
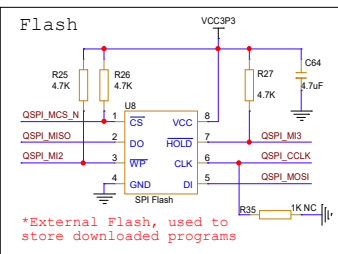
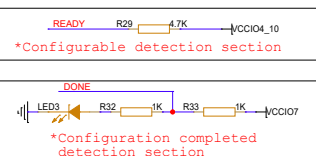
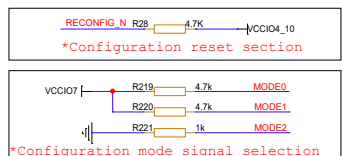
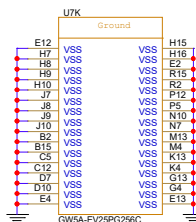
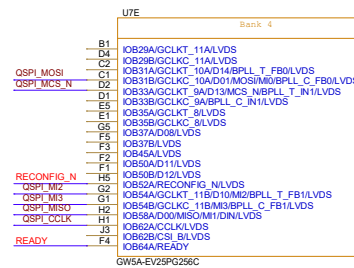
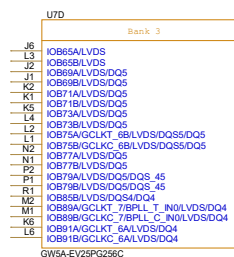
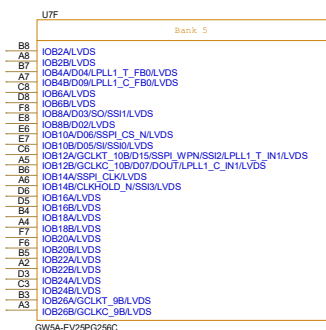
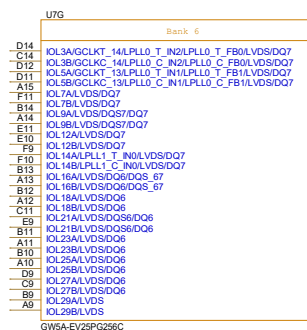
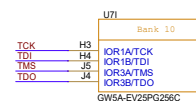
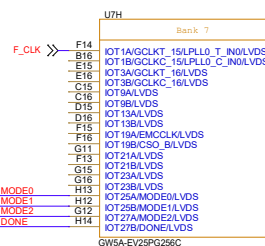
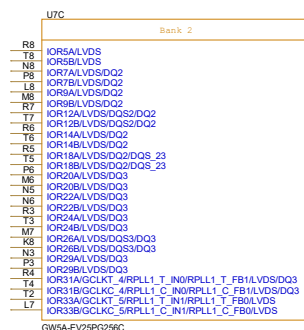
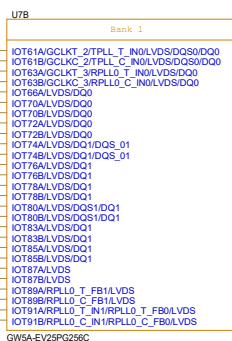
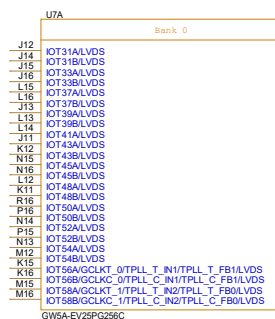
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714,

For details about how to select the Mode signal, see Chapter 3.1 of the Arora V 25K FPGA Products Programming and Configuration Guide.

6. The MSPI signal levels must match the Flash power supply voltage.

6. The MSPI signal levels must match the Flash power. If the voltage of the MSPI BANK does not match the

GW5A-EV25PG256C



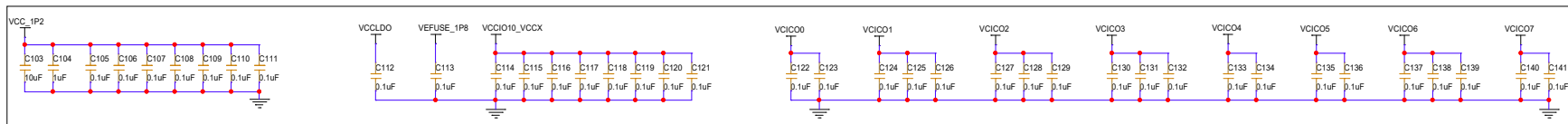
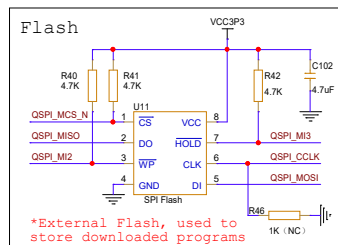
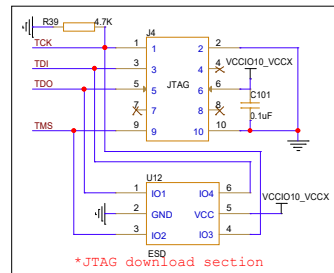
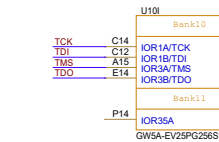
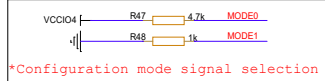
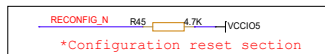
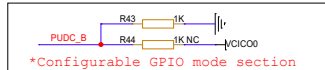
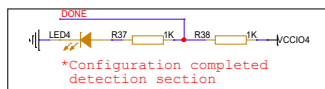
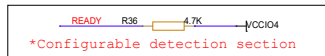
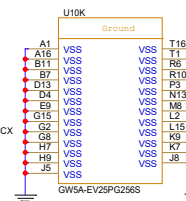
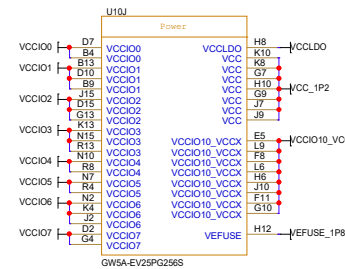
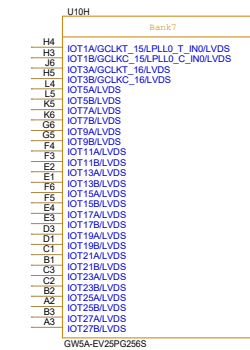
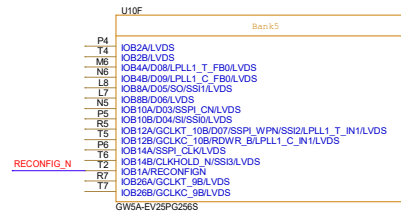
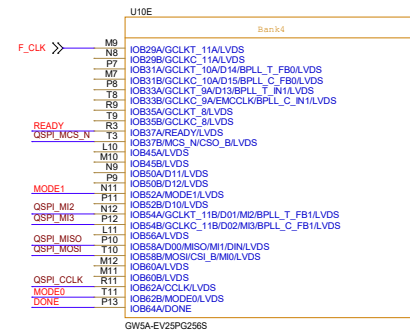
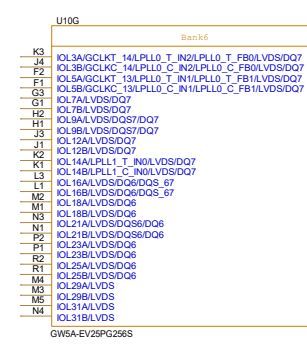
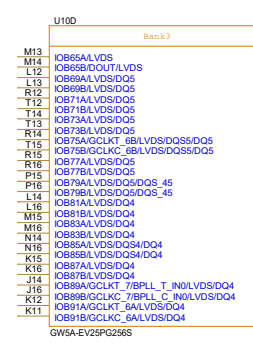
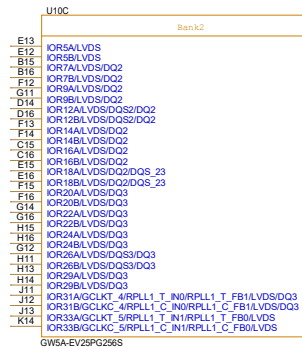
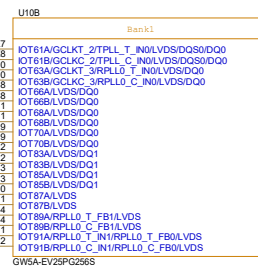
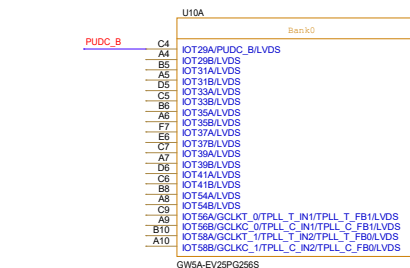
Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash Model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage,
a level shifter is required for voltage translation.

Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
V _{CC}	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCN}	Auxiliary voltage	2.375	3.465V
V _{CCIO2} ⁽¹⁾	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{FUSE} ⁽²⁾	Voltage required for eFuse writing	1.62V	1.99V
MIPI			
V _{DDMI}	Analog core power supply voltage	0.87V	1V
V _{DDM}	Digital core power supply voltage	0.87V	1V
V _{DDMI}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{DD12M}	MIPI LP power supply voltage	1.14V	1.32V
Note:			
⁽¹⁾ The greater the V _{CCIO2} voltage, the higher the power consumption.			
⁽²⁾ When V _{FUSE} is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			

Title			
GOWIN Minimum System Diagram			
Size	Document Number	Rev	
C	GW5A-EV25PG256C	2.7	
Date:	Thursday, April 17, 2025	Sheet	3 of 18

GW5A-EV25PG256S



Notes:

1.F CLK signal is an external input clock signal.

It is recommended that F CLK signal be provided through an ac

2.External Flash memory is used to store downloaded programs.

For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714,

Arora V 25K FPGA Products Programming and Configuration Guide .

3. It is recommended that add an ESD protection chip to the JTAG download circuit.

4.VCC core voltage requires a large current, so it is recommended to s

5.The MODE pin is the GowinCONFIG configuration mode selection signal.

5. The MODE pin is the GowinCONFIG configuration mode selection signal. For details about how to select the Mode signal, see "Chapter 3.1 Configuring the Mode Signal".

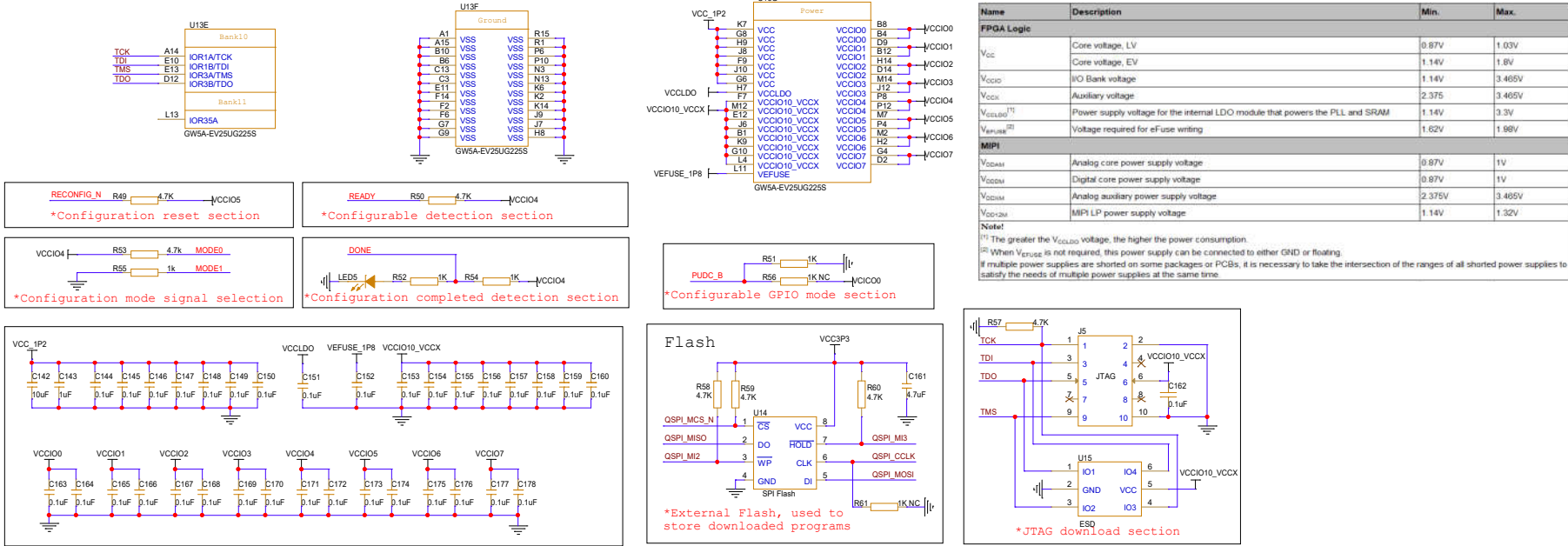
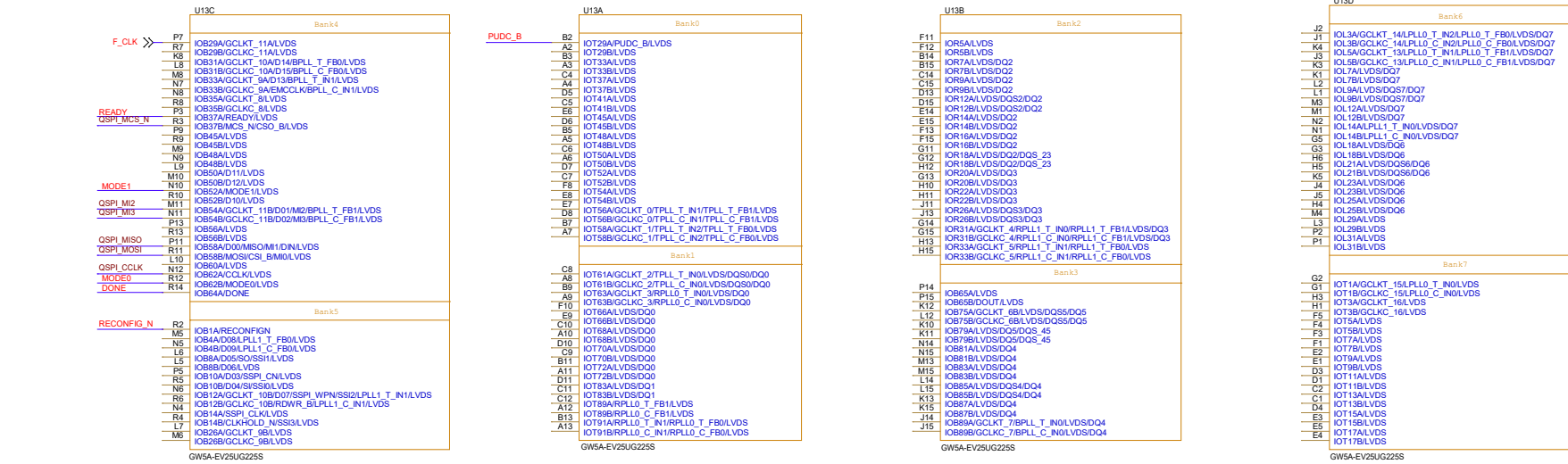
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG-14, Arora V 25K FPGA Products Programming and Configuration Guide.

6. The MSPI signal levels must match the Flash power supply voltage.

6. The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage,

If the voltage of the MSPI BANK does not match the Flash power supply, a level shifter is required for voltage translation.

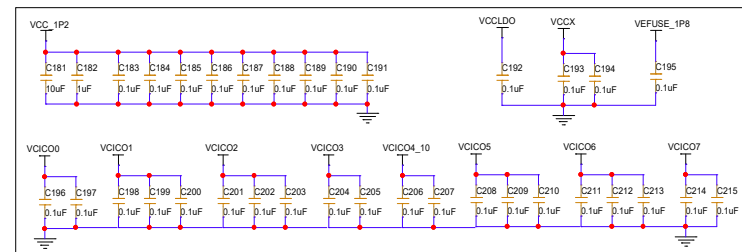
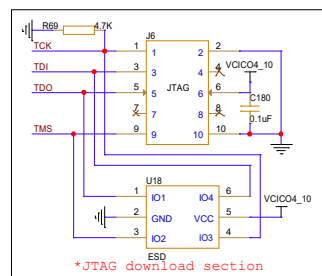
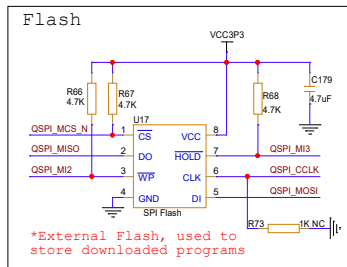
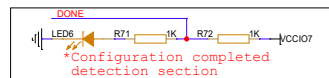
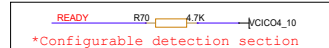
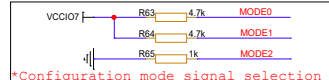
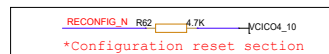
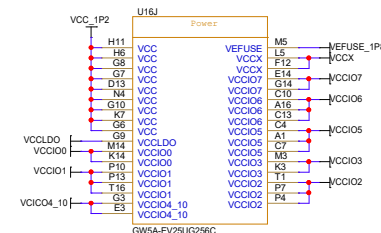
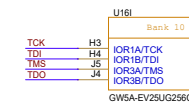
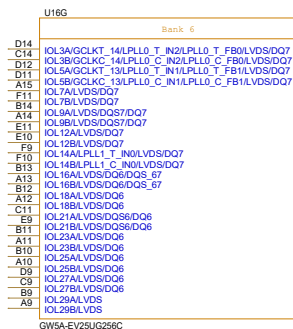
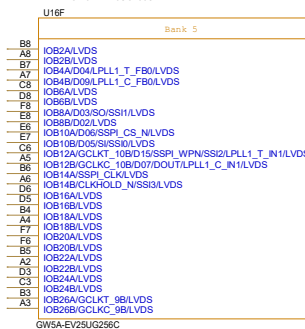
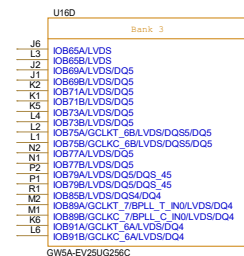
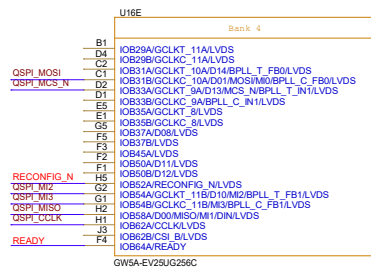
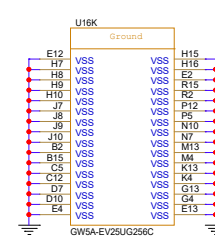
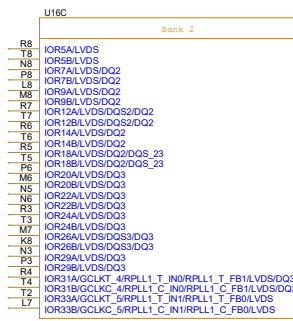
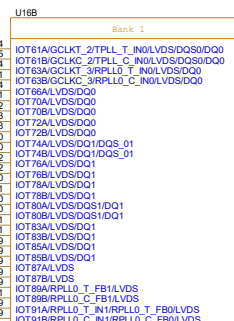
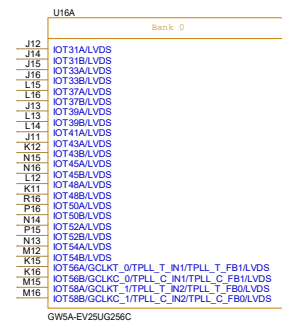
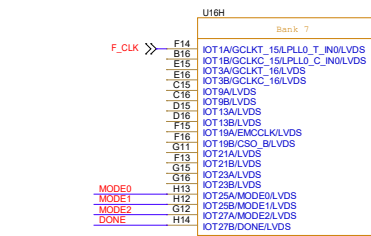
Title			
GOWIN Minimum System Diagram			
Size	Document Number	Rev	
C	GW5A-EV25PG256S	2.7	
Date:	Thursday, April 17, 2025	Sheet	4 of 18



Notes:

- 1.F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage. If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

GW5A-EV25UG256C



Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCAUX}	Auxiliary voltage	2.375	3.465V
V _{CCIO1} ⁽¹⁾	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{APLUS} ⁽²⁾	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V _{CCDM1}	Analog core power supply voltage	0.87V	1V
V _{CCDM}	Digital core power supply voltage	0.87V	1V
V _{CCDMA}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{CCD12M}	MIPI LP power supply voltage	1.14V	1.32V

⁽¹⁾ The greater the V_{CCQDQ} voltage, the higher the power consumption

^[2] When V_{CRSS} is not required, this power supply can be connected to either GND or floating.

If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.

Notes:

1.F CLK signal is an external input clock signal.

It is recommended that F CLK signal be provided through an active oscillator crystal.

2.External Flash memory is used to store downloaded programs

For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714,

Arora V 25K FPGA Products Programming and Configuration Guide .

3. It is recommended that add an ESD protection chip to the JTAG download circuit.

4.VCC core voltage requires a large current, so it is recommended to s

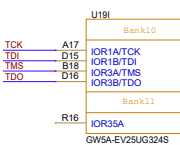
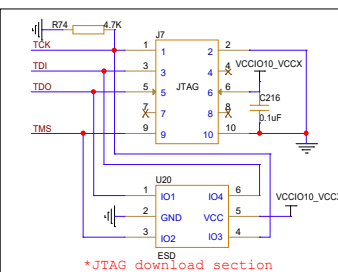
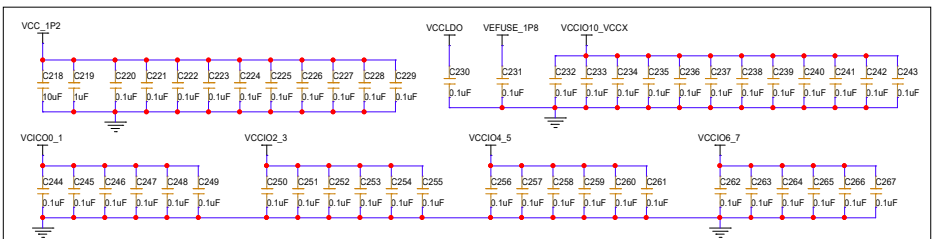
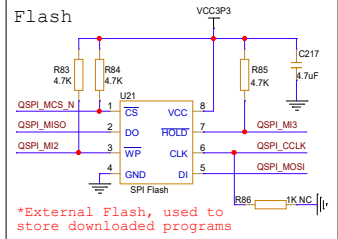
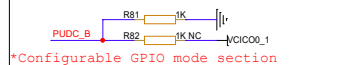
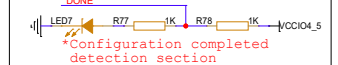
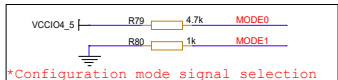
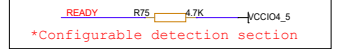
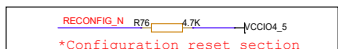
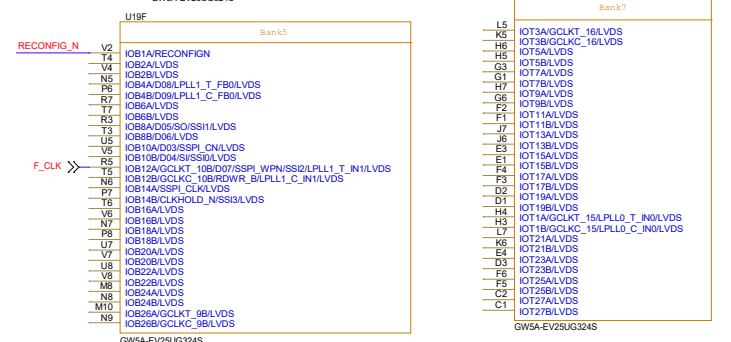
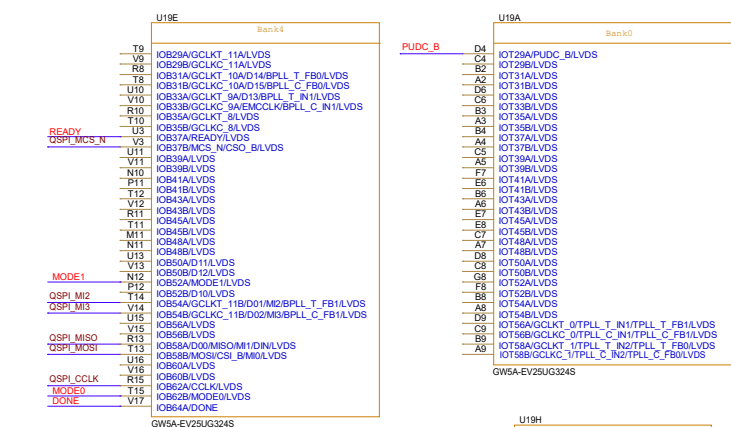
5.The MODE pin is the GowinCONFIG configuration mode selection signal.

For details about how to select the Mode signal, see "Chapter 3.

Arora V 25K FPGA Products Programming and Configuration Guide.

6. The MSPI signal levels must match the Flash power supply voltage. If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

GW5A-EV25UG324S

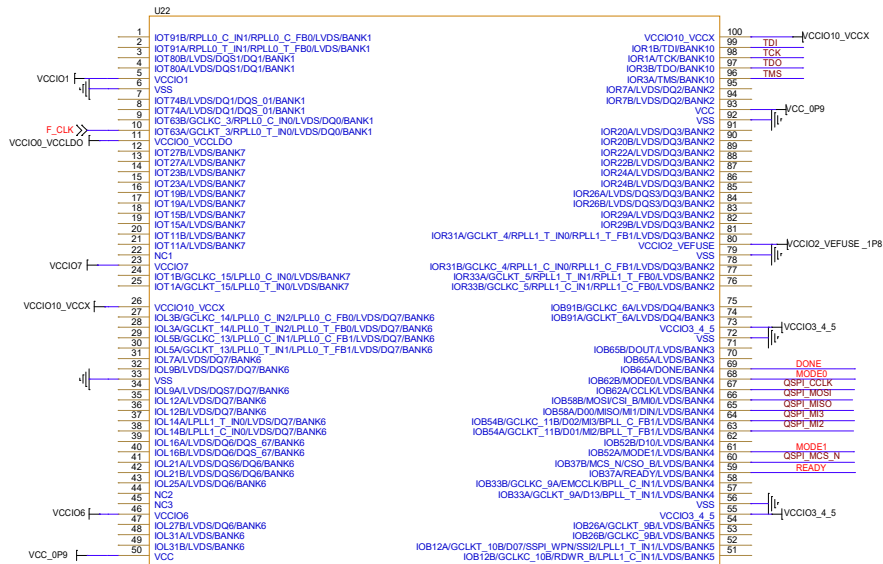


Name	Description	Min.	Max.
PPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCA}	Auxiliary voltage	2.375	3.465V
V _{CELLDO} TM	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{EPUFUSE} TM	Voltage required for eFuse writing	1.02V	1.98V
MIPI			
V _{CCAH}	Analog core power supply voltage	0.87V	1V
V _{CCDM}	Digital core power supply voltage	0.87V	1V
V _{CCIH}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{CC-L2N}	MIPI LP power supply voltage	1.14V	1.32V
Note:			
TM The greater the V _{CELLDO} voltage, the higher the power consumption.			
^{EV} When V _{EVUSE} is required, this power supply can be connected to either GND or floating.			
TM If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			

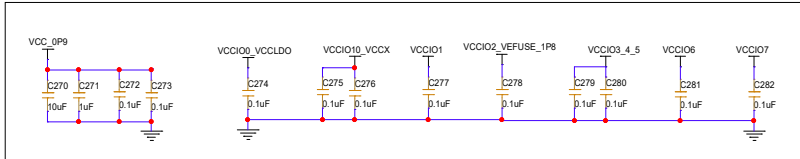
Notes:

- 1.F CLK signal is an external input clock signal. It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage. If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

GW5A-LV25LQ100



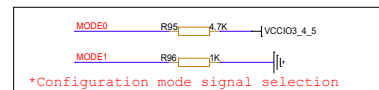
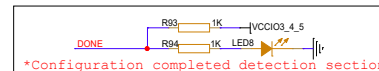
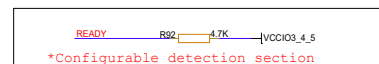
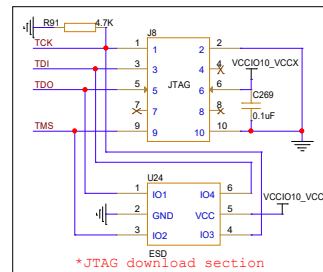
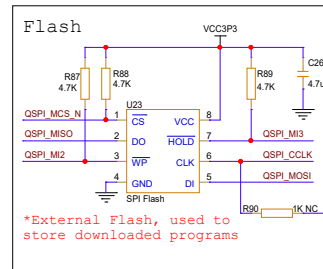
GW5A-LV25LQ100



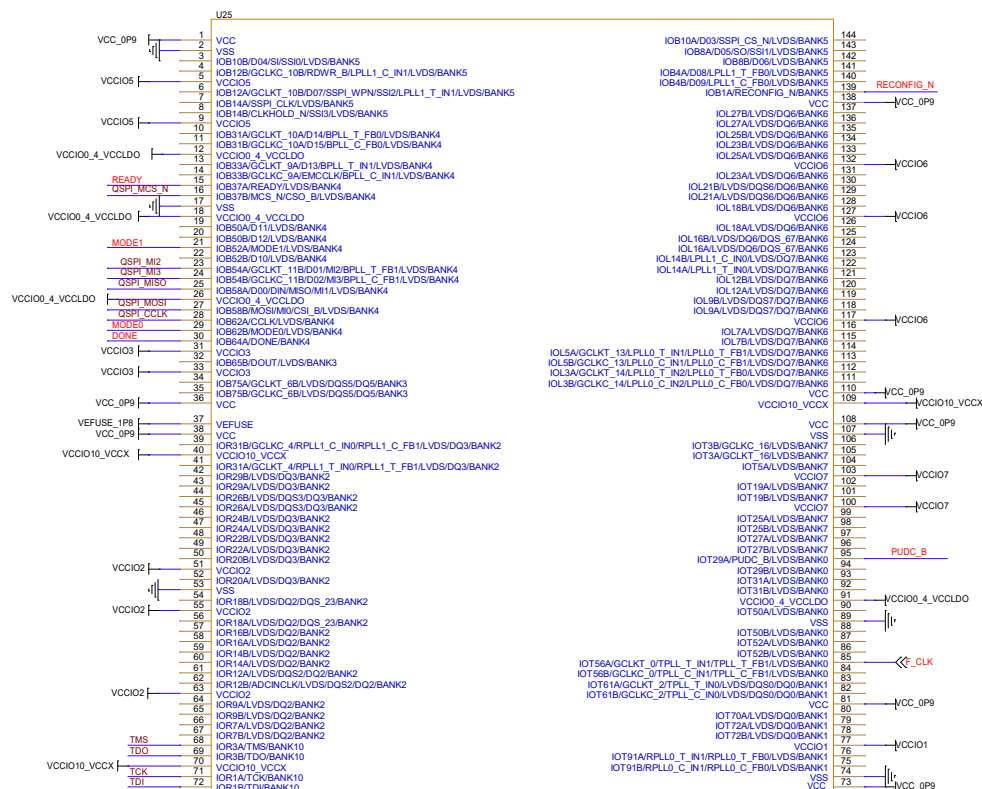
Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V _{DDIO}	I/O Bank voltage	1.14V	3.465V
V _{CCAUX}	Auxiliary voltage	2.375	3.465V
V _{CCDDO} ^[1]	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{APUFUSE} ^[2]	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V _{DDAH}	Analog core power supply voltage	0.87V	1V
V _{DDDM}	Digital core power supply voltage	0.87V	1V
V _{DDIOM}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{DDI2M}	MIPI LP power supply voltage	1.14V	1.32V
Notes!			
^[1] The greater the V _{CCDDO} voltage, the higher the power consumption.			
^[2] When V _{APUFUSE} is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies as the operating range.			

Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage,
a level shifter is required for voltage translation.



GW5A-LV25LQ144



GW5A-LV25LQ144

Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V _{CCD}	I/O Bank voltage	1.14V	3.465V
V _{CCA}	Auxiliary voltage	2.375	3.465V
V _{CELLDO} ^[1]	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{EPUSE} ^[2]	Voltage required for eFuse writing	1.62V	1.98V
MP1			
V _{DDAN}	Analog core power supply voltage	0.87V	1V
V _{DDDM}	Digital core power supply voltage	0.87V	1V
V _{DDHM}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{DD12M}	MP1 LP power supply voltage	1.14V	1.32V
Note:			
^[1] The greater the V _{CELLDO} voltage, the higher the power consumption.			
^[2] When V _{EPUSE} is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of all shorted power supplies as the minimum voltage.			

Notes:

Notes:
1.F CLK signal is an external input clock signal.

It is recommended that F CLK signal be provided through an active oscillator crystal.

2. External Flash memory is used to store downloaded programs.

For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714.

Arora V 25K FPGA Products Programming and Configuration Guide .

3. It is recommended that add an ESD protection chip to the JTAG download circuit.

4.VCC core voltage requires a large current, so it is recommended to supply power separately.

5. The MODE pin is the GowinCONFIG configuration mode selection signal.

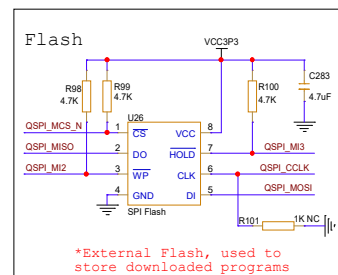
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714.

For details about how to select the Mode signal, see Chapter 3.1 of the Arora V 25K FPGA Products Programming and Configuration Guide.

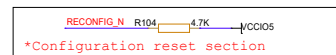
6. The MSPI signal levels must match the Flash power supply voltage.

6. The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage,

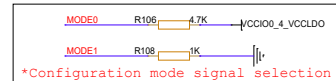
If the voltage of the MSP1 BANK does not match the
a level shifter is required for voltage translation.



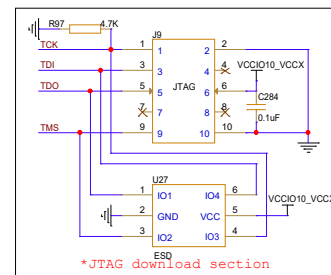
*External Flash, used to store downloaded programs



*Configuration reset section



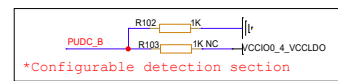
*Configuration mode signal selection



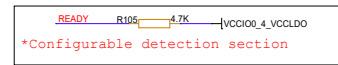
```

ESD
*JTAG download section

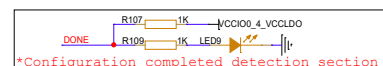
```



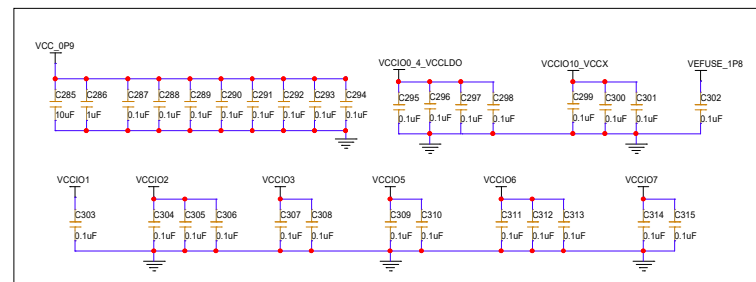
*Configurable detection section



*Configurable detection section

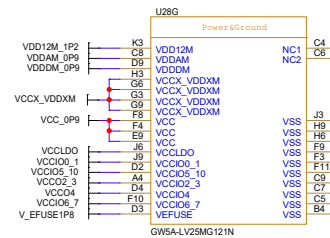
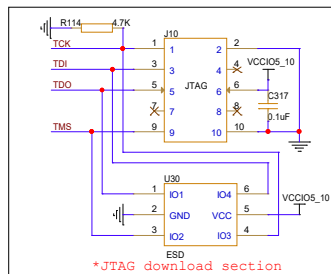
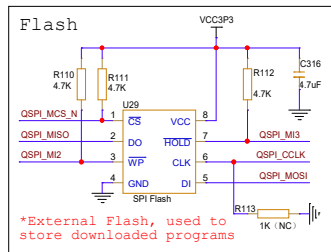
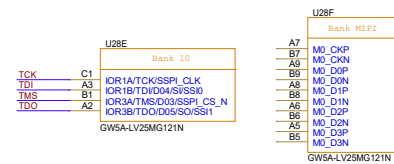
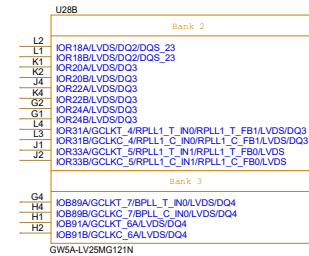
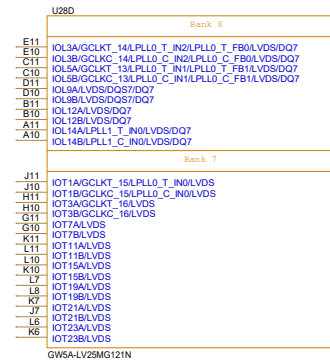
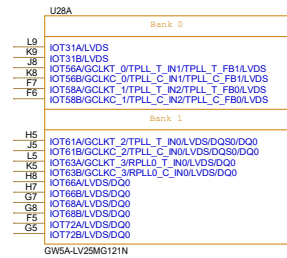
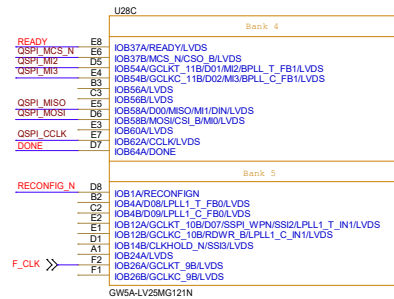


*Configuration completed detection section



Title				
GOWIN Minimum System Diagram				
Size	Document Number			Rev
C	GW5A-LV25LQ144			2.1
Date:	Thursday, April 17, 2025	Sheet	9	of 18

GW5A-LV25MG121N



Name	Description	Min.	Max.
FPQA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
V _{CC}	Core voltage, EV	1.14V	1.6V
V _{CCD}	I/O Bank voltage	1.14V	3.465V
V _{CCA}	Auxiliary voltage	2.375	3.465V
V _{CC_LDO} ⁽¹⁾	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{APU_{SR}} ⁽²⁾	Voltage required for eFuse writing	1.62V	1.96V
MIPI			
V _{CCDM}	Analog core power supply voltage	0.87V	1V
V _{CCDM}	Digital core power supply voltage	0.87V	1V
V _{CCDM}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{CCD2M}	MIPI LP power supply voltage	1.14V	1.32V

⁽¹⁾ The greater the V_{COLDO} voltage, the higher the power consumption

⁽²⁾ When V_{FUSE} is not required, this power supply can be connected to either GND or floating.

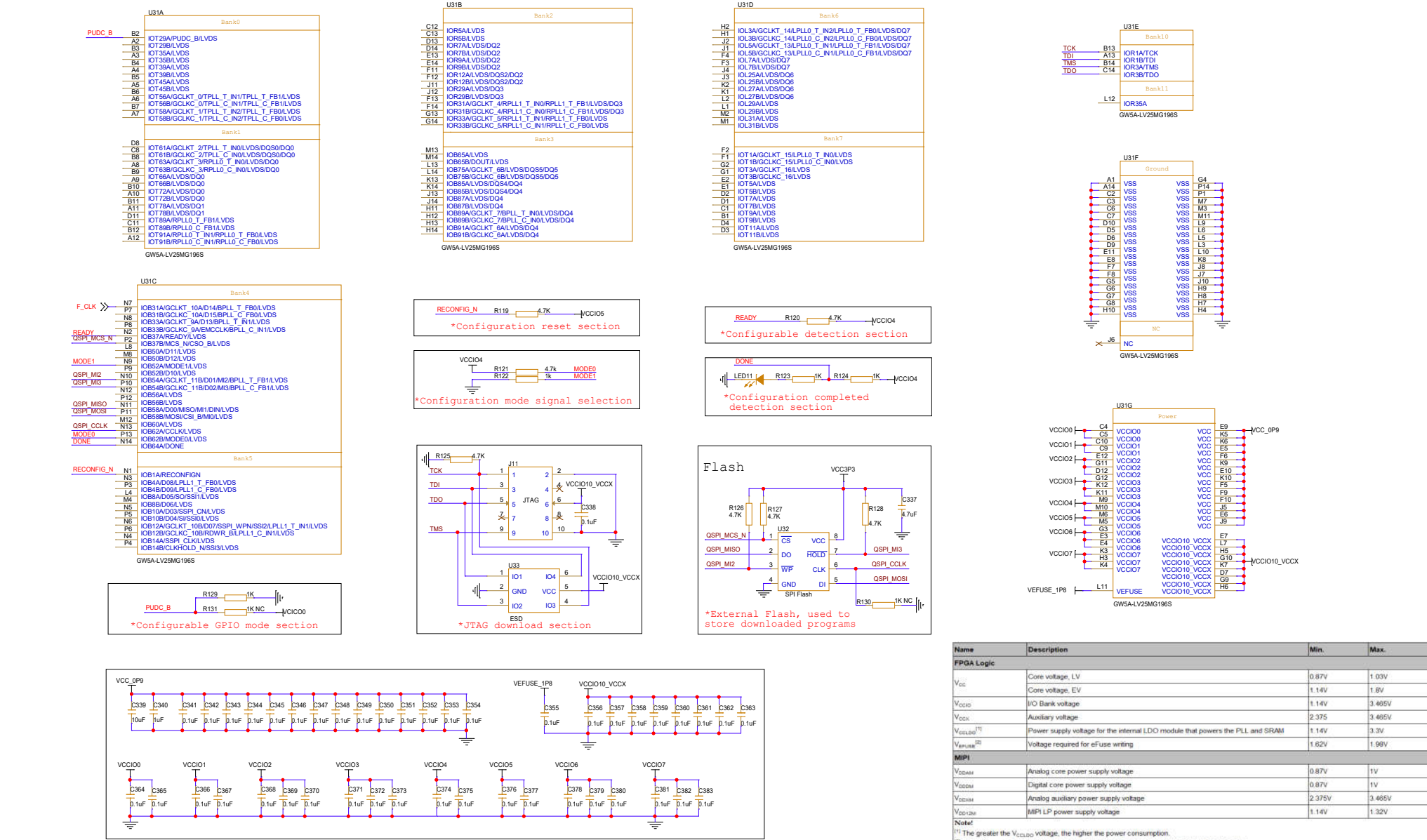
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.

Notes:

- Notes:
- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
 - 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
 - 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
 - 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
 - 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
 - 6.The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

Title			
GOWIN Minimum System Diagram			
Size	Document Number	Rev	
C	GW5A-LV25MG121N	2.7	
Date:	Thursday, April 17, 2025	Sheet	10 of 18

GW5A-LV25MG196S

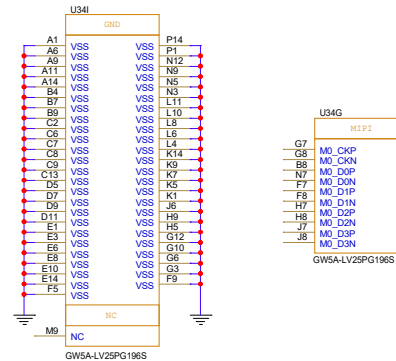
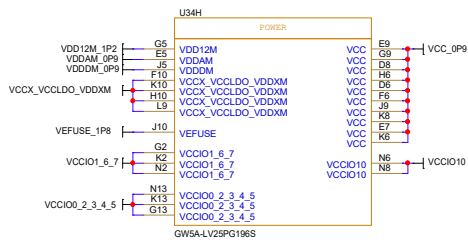
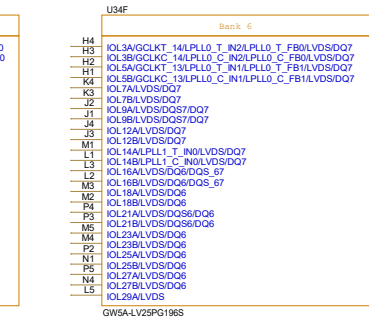
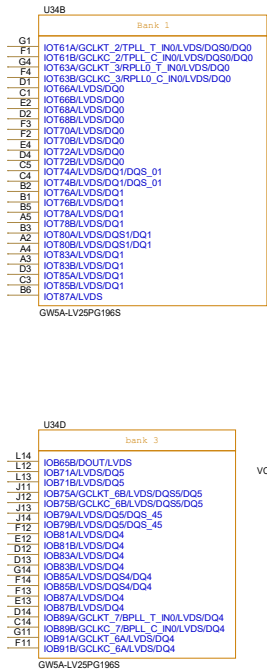
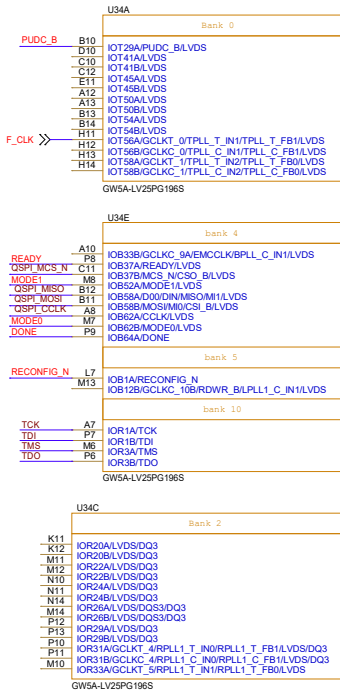


Notes:

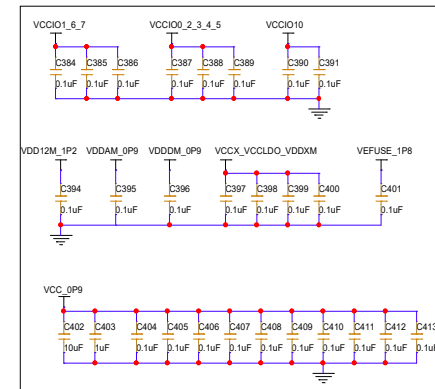
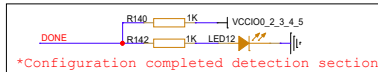
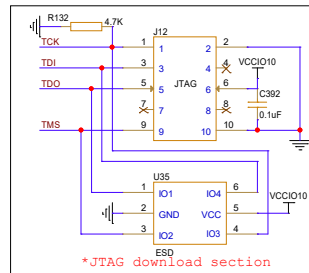
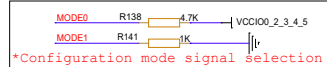
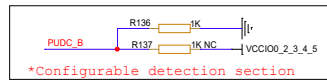
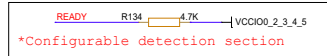
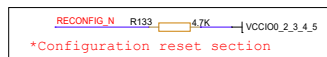
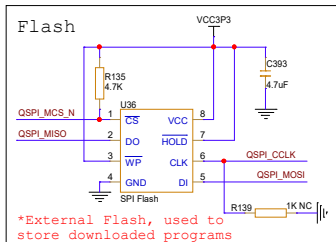
- 1.F CLK signal is an external input clock signal.
- It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.
- If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
V _{CC}	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCX}	Auxiliary voltage	2.375	3.465V
V _{CCIO0} ⁽¹⁾	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{FWRITE} ⁽²⁾	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V _{DDAN}	Analog core power supply voltage	0.87V	1V
V _{DDDM}	Digital core power supply voltage	0.87V	1V
V _{DDHM}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{DD12M}	MIPI LP power supply voltage	1.14V	1.32V
Note!			
⁽¹⁾ The greater the V _{CCIO0} voltage, the higher the power consumption.			
⁽²⁾ When V _{FWRITE} is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shared on some packages or PCBs, it is necessary to take the intersection of the ranges of all shared power supplies to satisfy the needs of multiple power supplies at the same time.			

GW5A-LV25PG196S



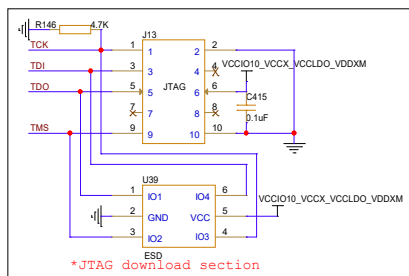
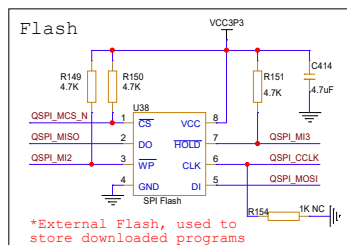
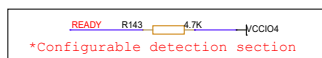
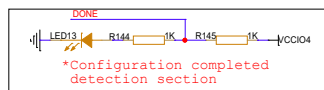
Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCAUX}	Auxiliary voltage	2.375	3.465V
V _{CCDDIO} ⁽¹⁾	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{FUSEB} ⁽²⁾	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V _{CCDM}	Analog core power supply voltage	0.87V	1V
V _{CCDM}	Digital core power supply voltage	0.87V	1V
V _{CCDM}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{CCDLM}	MIPI LP power supply voltage	1.14V	1.32V
Notes:			
⁽¹⁾ The greater the V _{CCDDIO} voltage, the higher the power consumption.			
⁽²⁾ When V _{FUSEB} is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shared on some packages or PCBs, it is necessary to take the intersection of the ranges of all shared power supplies to satisfy the needs of multiple power supplies at the same time.			



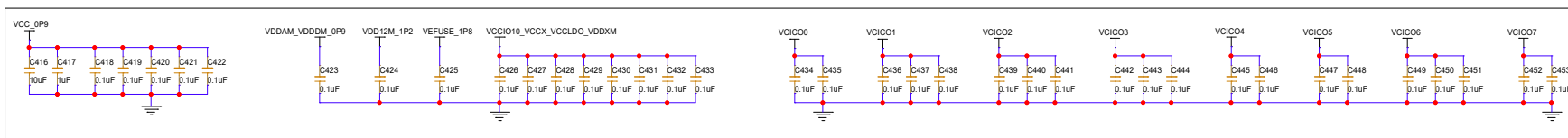
Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash Model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage,
a level shifter is required for voltage translation.

GW5A-LV25PG256



Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
V _{CCM}	Core voltage, EV	1.14V	1.6V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCAUX}	Auxiliary voltage	2.375	3.465V
V _{CCIOE} ^[1]	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{APURST} ^[2]	Voltage required for eFuse writing	1.02V	1.96V
MIPI			
V _{DDAH}	Analog core power supply voltage	0.87V	1V
V _{DDDM}	Digital core power supply voltage	0.87V	1V
V _{DDAHM}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{DD12M}	MIPI LP power supply voltage	1.14V	1.32V
Note:			
^[1] The greater the V _{CCIOE} voltage, the higher the power consumption.			
^[2] When V _{EFUSE} is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shared on some packages or PCBs, it is necessary to take the intersection of the ranges of all shared power supplies satisfy the needs of multiple power supplies at the same time.			

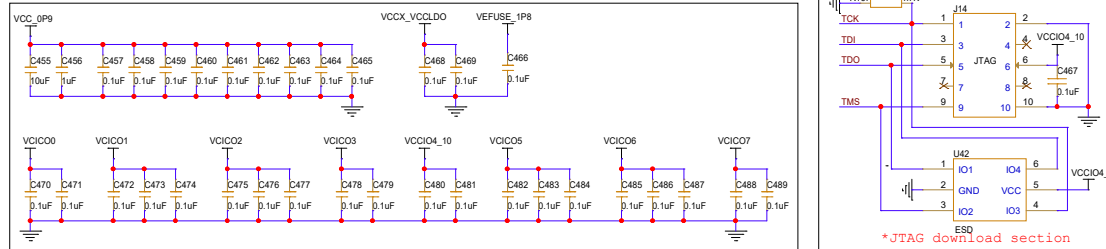
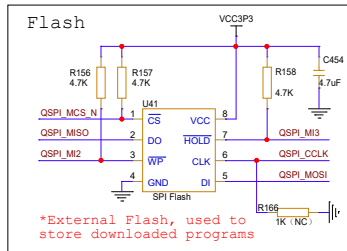
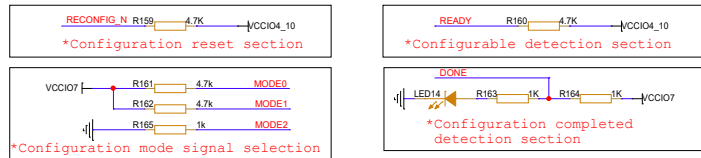
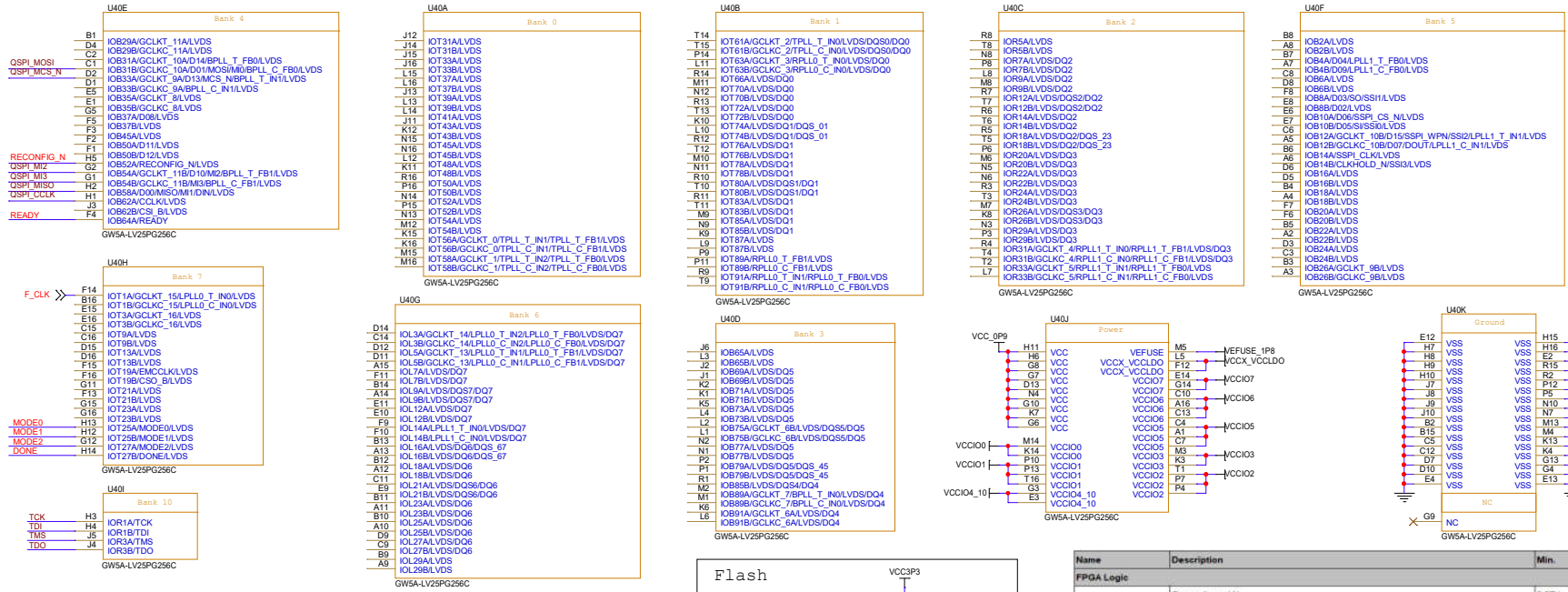


Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash Model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage,
a level shifter is required for voltage translation.

Title				
GOWIN Minimum System Diagram				
Size C	Document Number GW5A-LV2SPG256			Rev 2.1
Date:	Thursday, April 17, 2025	Sheet	13 of 18	

GW5A-LV25PG256C

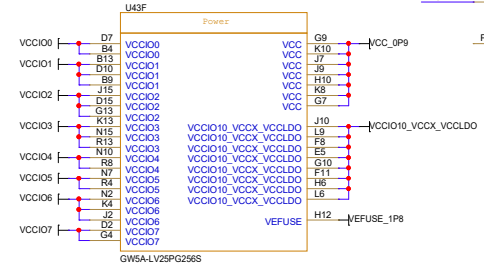
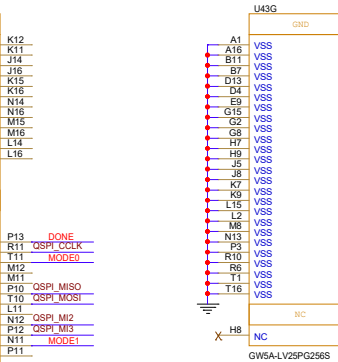
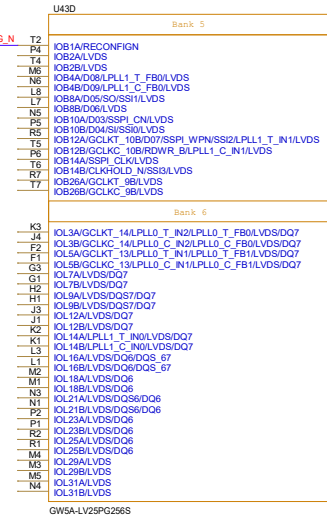
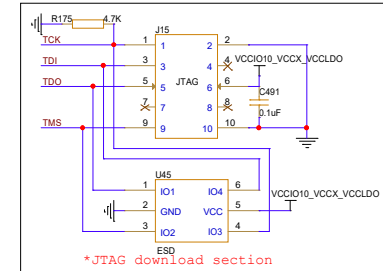
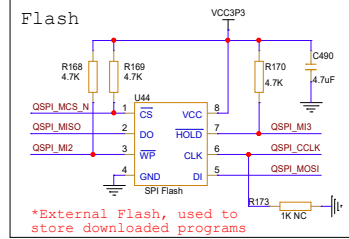
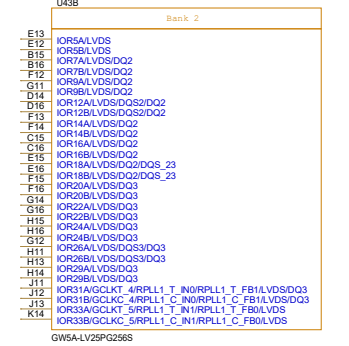
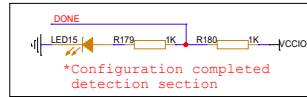
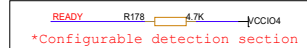
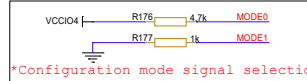
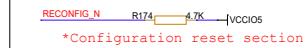
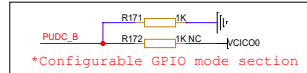


Notes:

- 1.F CLK signal is an external input clock signal.
- It is recommended that F CLK signal be provided through an active oscillator crystal.
- External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- It is recommended that add an ESD protection chip to the JTAG download circuit.
- VCC core voltage requires a large current, so it is recommended to supply power separately.
- The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- The MSPI signal levels must match the Flash power supply voltage.
- If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

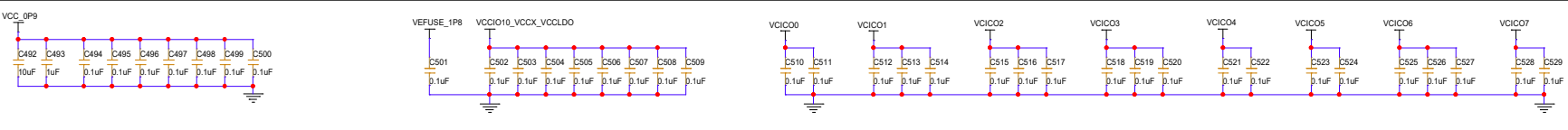
Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
V _{CC}	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CC}	Auxiliary voltage	2.375	3.465V
V _{CCIO0} ⁽¹⁾	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{EFUSE} ⁽²⁾	Voltage required for eFuse writing	1.62V	1.96V
MSPI			
V _{DDAH}	Analog core power supply voltage	0.87V	1V
V _{DDDM}	Digital core power supply voltage	0.87V	1V
V _{DDAH}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{DDI2M}	MSPI LP power supply voltage	1.14V	1.32V
Note:			
⁽¹⁾ The greater the V _{CCIO0} voltage, the higher the power consumption.			
⁽²⁾ When V _{EFUSE} is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			

GW5A-LV25PG256S



Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.6V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCA}	Auxiliary voltage	2.375	3.465V
V _{CELLIO} ⁽¹⁾	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{APURS} ⁽²⁾	Voltage required for eFUSE writing	1.62V	1.98V
MIPI			
V _{DDAH}	Analog core power supply voltage	0.87V	1V
V _{DDDM}	Digital core power supply voltage	0.87V	1V
V _{DDIM}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{DDL2M}	MIPI LP power supply voltage	1.14V	1.32V

^[2] When V_{EUSE} is not required, this power supply can be connected to either GND or floating.
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.

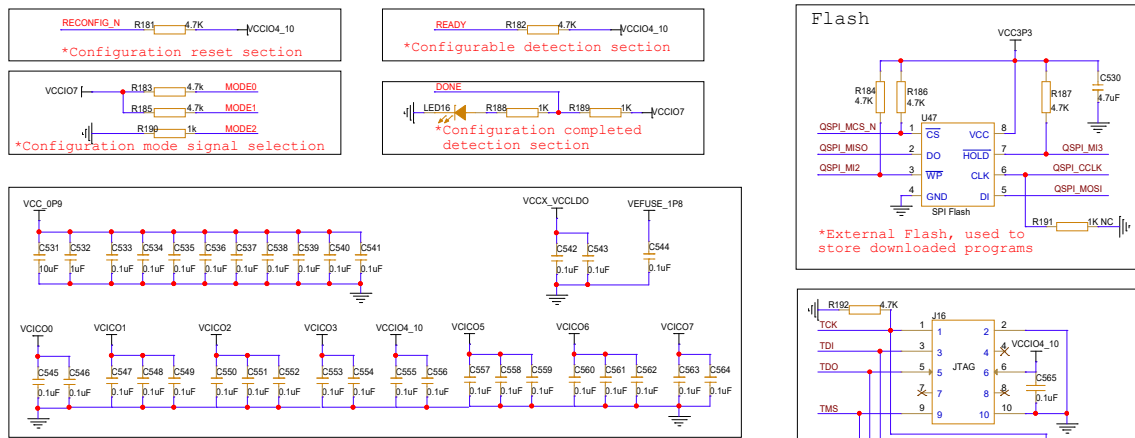


Notes:

- 1.F CLK signal is an external input clock signal.
- It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arara V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arara V 25K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.

If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

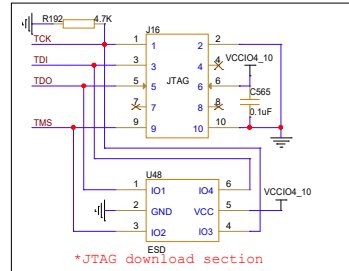
GW5A-LV25UG256C



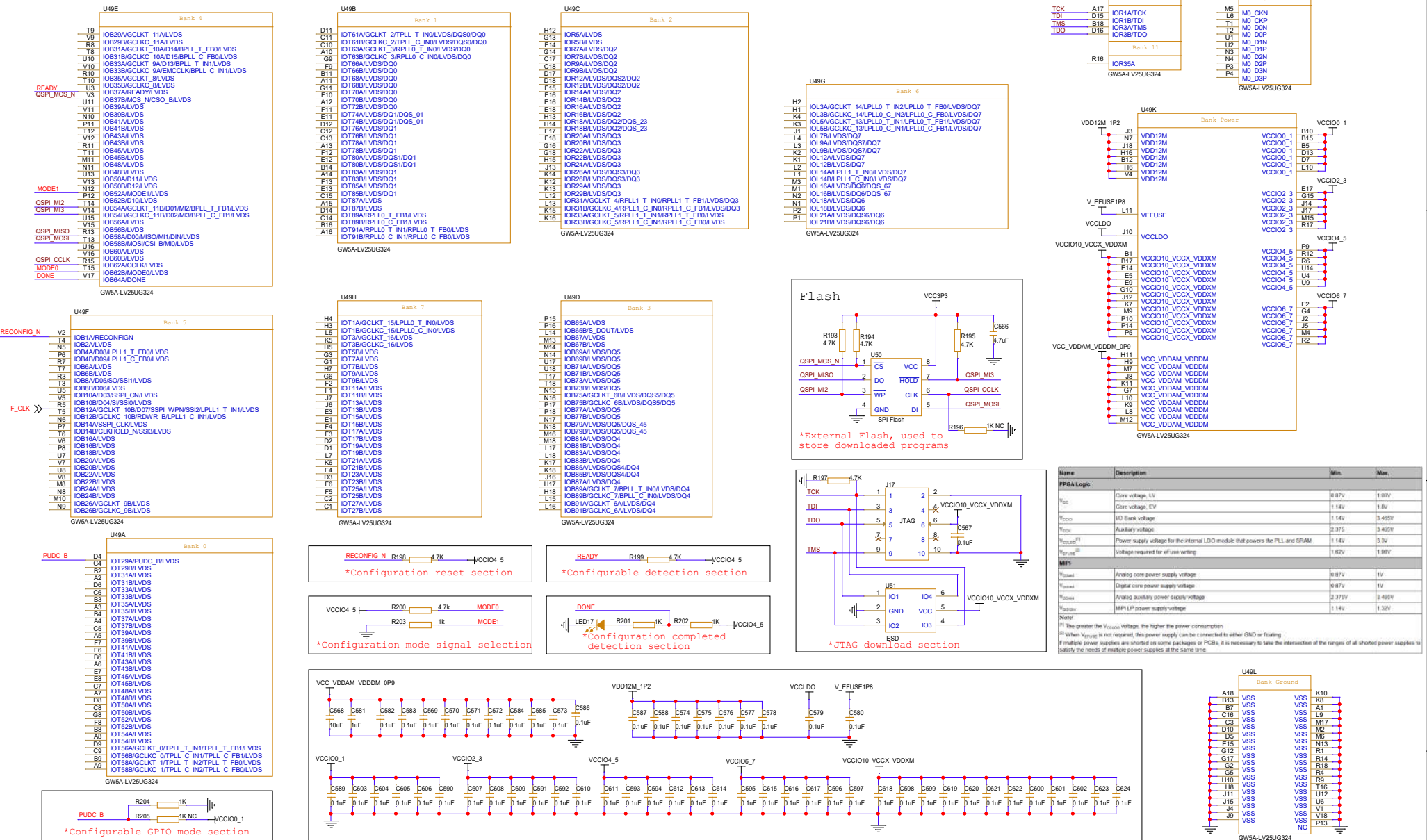
Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCK}	Auxiliary voltage	2.375	3.465V
V _{CCLDO} ⁽¹⁾	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{FUSE} ⁽²⁾	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V _{CCDM}	Analog core power supply voltage	0.87V	1V
V _{CCDM}	Digital core power supply voltage	0.87V	1V
V _{CCDM}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{CC12M}	MIPI LP power supply voltage	1.14V	1.32V
Note:			
⁽¹⁾ The greater the V _{CCLDO} voltage, the higher the power consumption.			
⁽²⁾ When V _{FUSE} is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shared on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			

Notes:

1. F_CLK signal is an external input clock signal. It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. VCC core voltage requires a large current, so it is recommended to supply power separately.
5. The MODE pin is the GowinCONFIG configuration mode selection signal. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
6. The MSPI signal levels must match the Flash power supply voltage. If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.



GW5A-LV25UG324



Notes:

1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
For details about SPI Flash mode selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. VCC core voltage requires a large current, so it is recommended to supply power separately.
5. The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
6. The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

Name	Description	Min.	Max.
PGGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
V _{CC}	Core voltage, EV	1.14V	1.8V
V _{DDIO}	IO Bank voltage	1.14V	3.45V
V _{DDIO}	Auxiliary voltage	2.37V	3.45V
V _{DDIO} ⁽¹⁾	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{PUDEF}	Voltage required for eFuse setting	1.62V	1.98V
MP1			
V _{DDANAL}	Analog core power supply voltage	0.87V	1V
V _{DDDIG}	Digital core power supply voltage	0.87V	1V
V _{DDIOH}	Auxiliary power supply voltage	2.37V	3.45V
V _{DDIOH}	MP1 LP power supply voltage	1.14V	1.52V

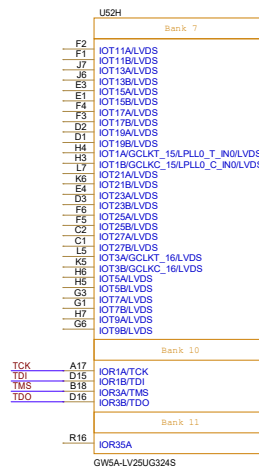
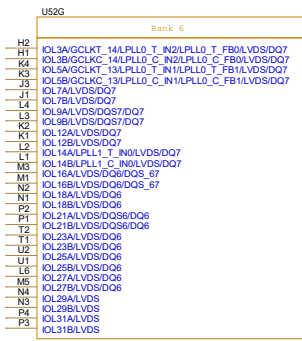
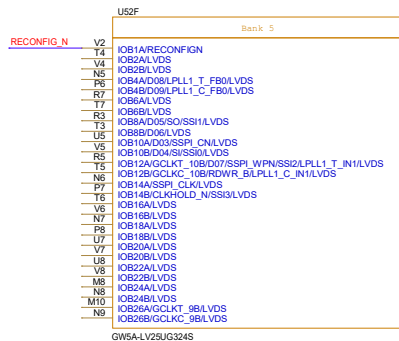
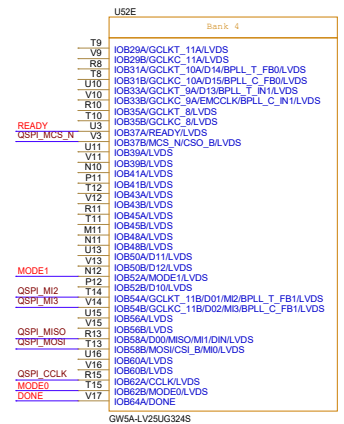
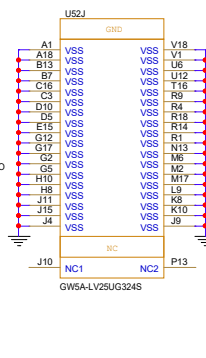
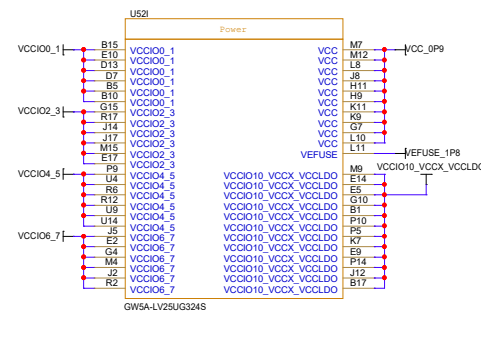
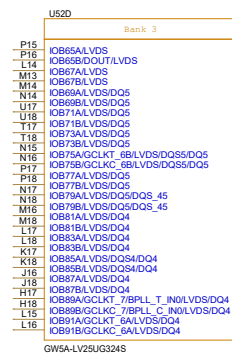
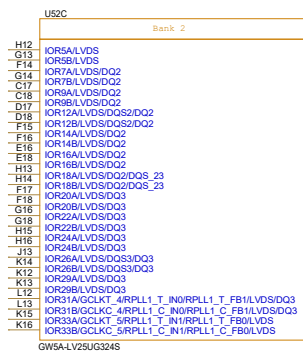
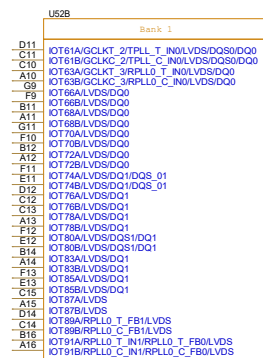
⁽¹⁾ The greater the V_{DDIOH} voltage, the higher the power consumption.

⁽²⁾ When V_{DDIOH} is not required, this power supply can be connected to either GND or floating.

⁽³⁾ Multiple power supplies are shared on some packages or PCBs, it is necessary to take the interaction of all shared power supplies to satisfy the needs of multiple power supplies at the same time.

Title			
GOWIN Minimum System Diagram			
Size	Document Number	Rev	
C	GW5A-LV25UG324	2.7	
Date:	Thursday, April 17, 2025	Sheet	17 of 18

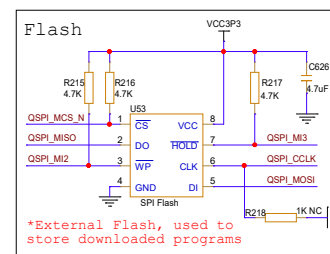
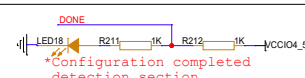
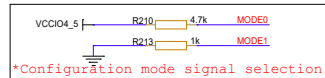
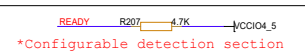
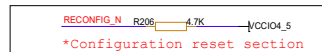
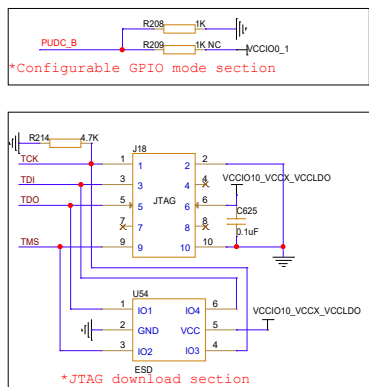
GW5A-LV25UG324S



Name	Description	Min.	Max.
PPGA Logic			
V_{CC}	Core voltage, LV	0.87V	1.03V
V_{CC}	Core voltage, EV	1.14V	1.8V
V_{DDI}	I/O Bank voltage	1.14V	3.405V
V_{DDI}	Auxiliary voltage	2.375	3.405V
$V_{COLDO}^{(1)}$	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
$V_{ANALOG}^{(2)}$	Voltage required for eFuse writing	1.62V	1.88V
MPU			
V_{DDM}	Analog core power supply voltage	0.87V	1V
V_{DDM}	Digital core power supply voltage	0.87V	1V
V_{DDM}	Analog auxiliary power supply voltage	2.375V	3.405V
V_{DDM}	MPU LP power supply voltage	1.14V	1.32V
Note:			
⁽¹⁾ The greater the V_{COLDO} voltage, the higher the power consumption. ⁽²⁾ When V_{ANALOG} is not required, the power supply can be connected to either GND or floating. If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			

[2] When V_{GFLSS} is not required, this power supply can be connected to either GND or floating.

Multiple power supplies are used in some packages (e.g., Core, it is necessary to take the interconnection of the heights of all installed power supplies to satisfy the needs of multiple power supplies at the same time.



*External Flash, used to store downloaded programs

Notes:

- 1.F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.

For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in Arora V 25K FPGA Products Programming and Configuration Guide .

- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.

For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in Arora V 25K FPGA Products Programming and Configuration Guide .

- 6.The MSPi signal levels must match the Flash power supply voltage.

If the voltage of the MSPi BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.