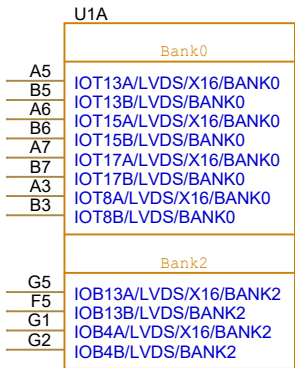
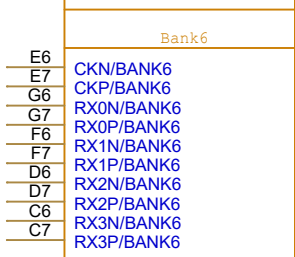
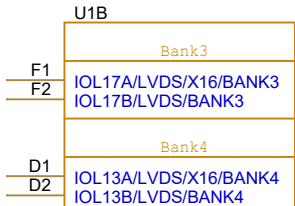


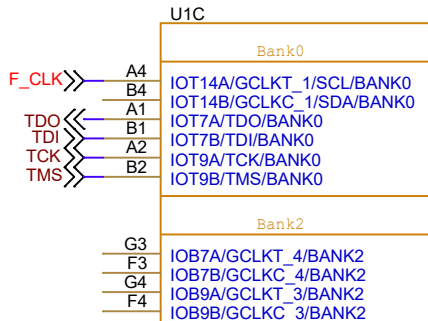
# GW1NR-LV2MG49G



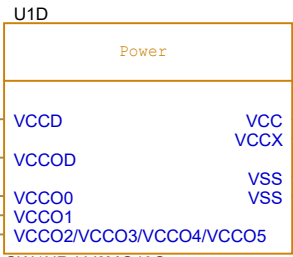
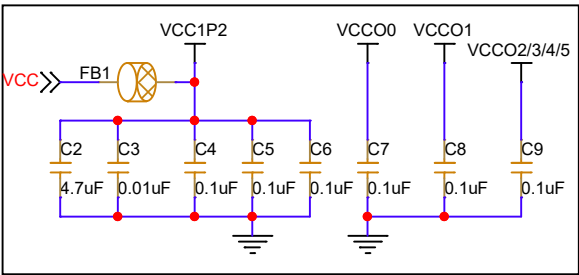
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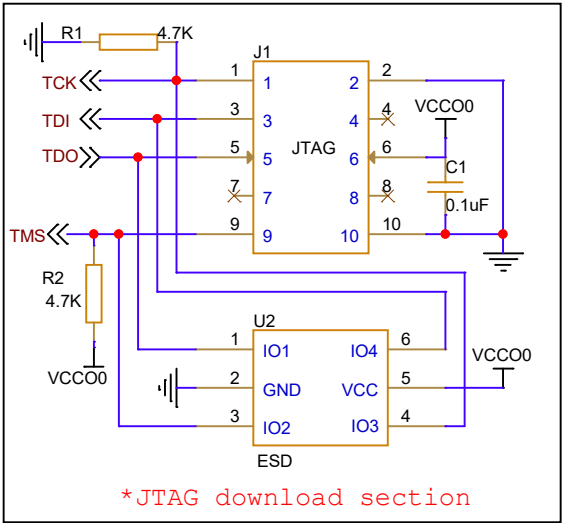
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GW1NR-LV2MG49G



\*JTAG download section

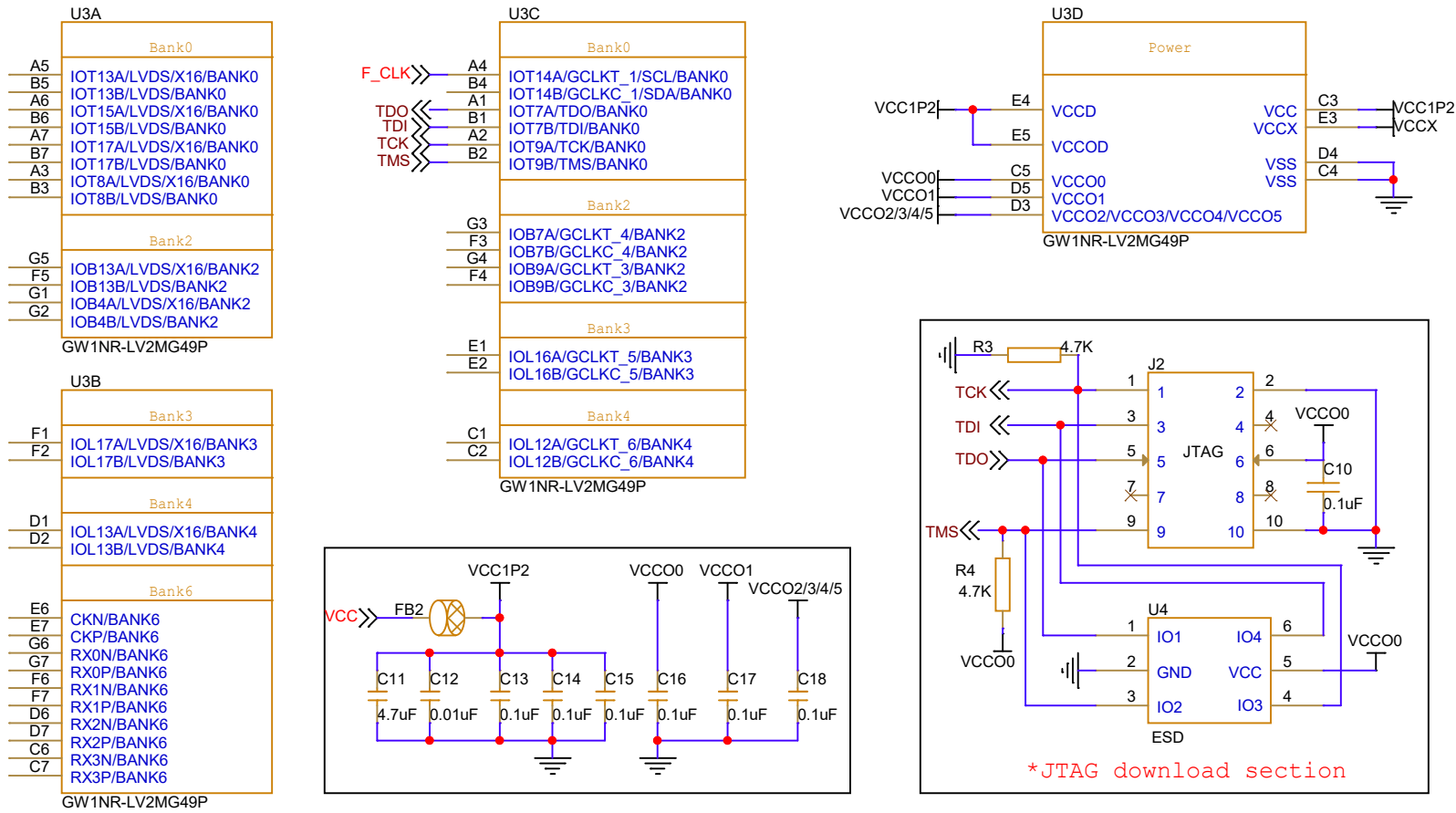
Notes:

1.F\_CLK signal is an external input clock signal.

It is recommended that F\_CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.

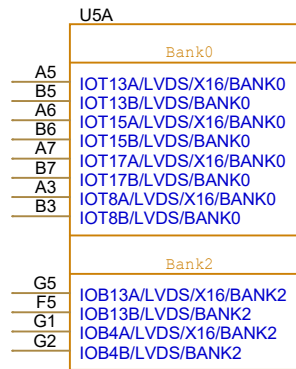
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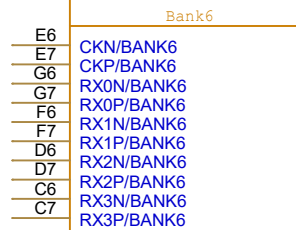
Notes:

- 1.F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

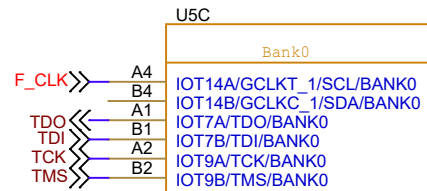
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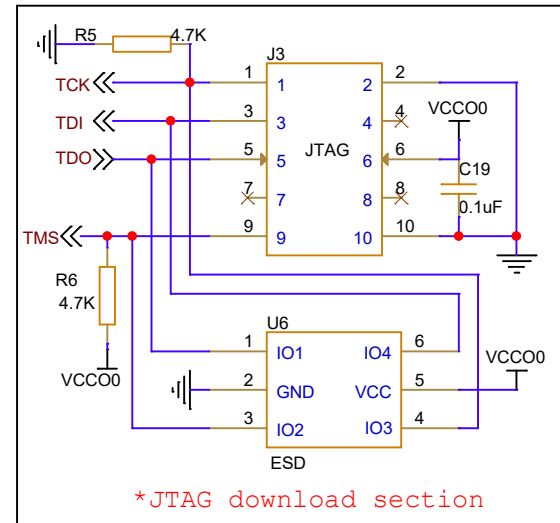
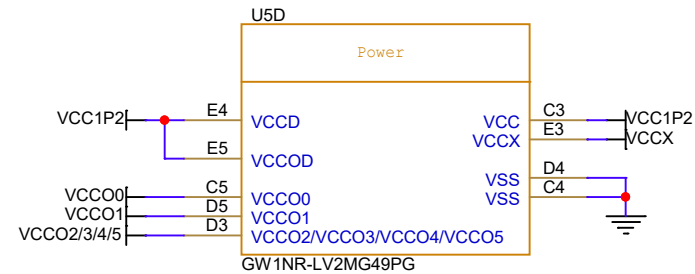
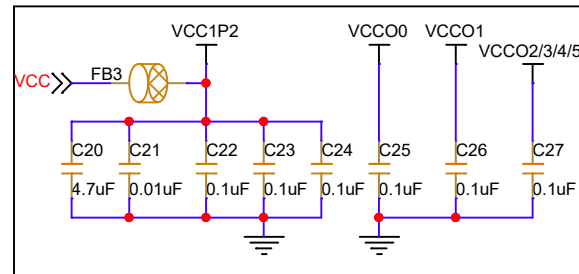
GW1NR-LV2MG49PG



GW1NR-LV2MG49PG



GW1NR-LV2MG49PG



## Notes:

1.F\_CLK signal is an external input clock signal.

It is recommended that F\_CLK signal be provided through an active oscillator crystal.

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Title  
GOWIN Minimum System Diagram

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A4

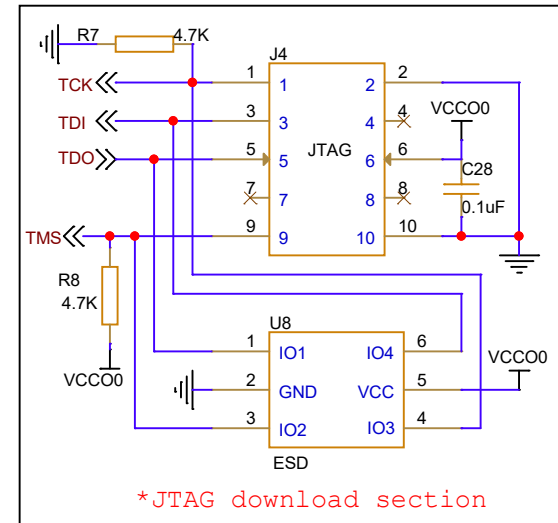
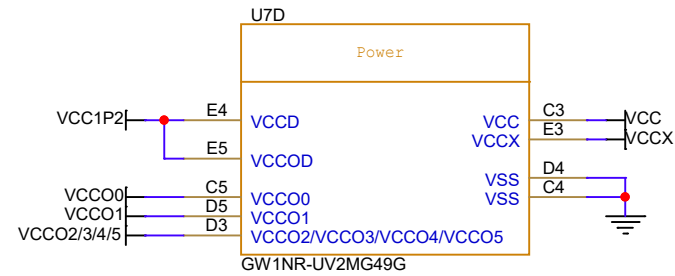
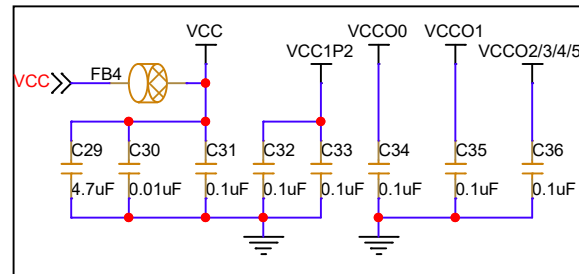
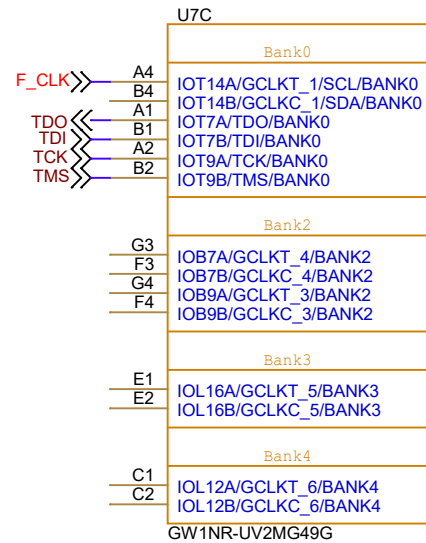
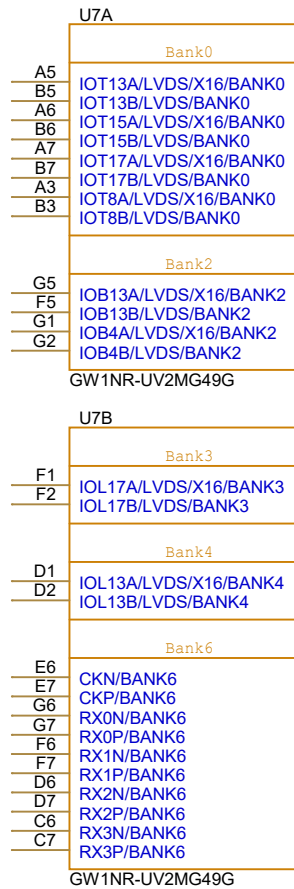
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GW1NR-LV2MG49PG

Rev  
2.1

Date: Wednesday, April 10, 2024

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# GW1NR-UV2MG49G



Notes:

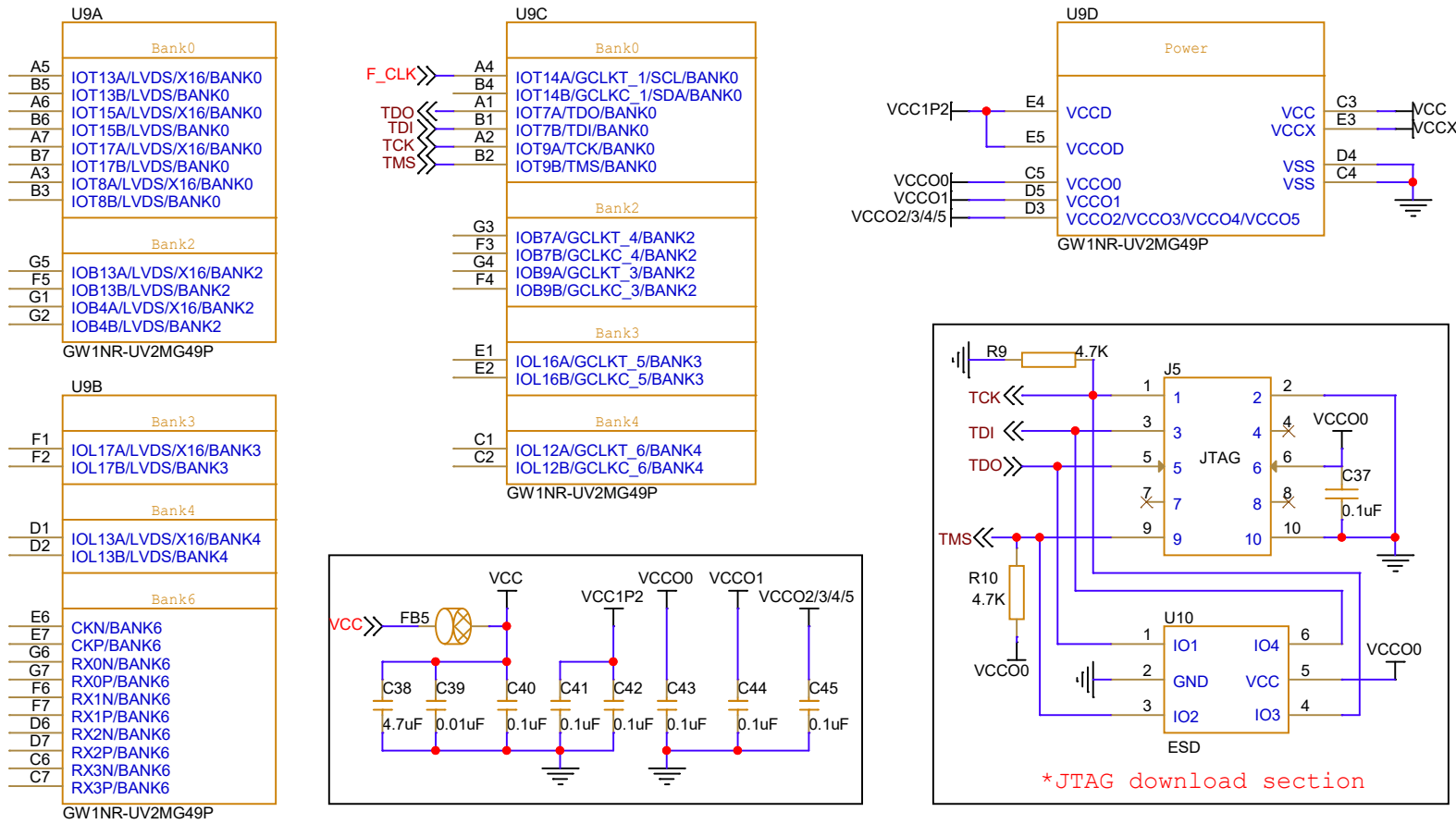
1.F\_CLK signal is an external input clock signal.

It is recommended that F\_CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
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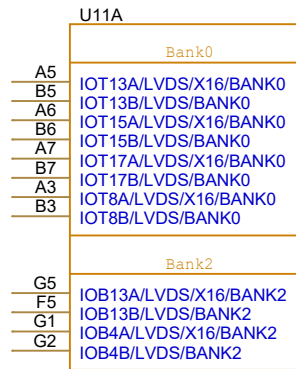
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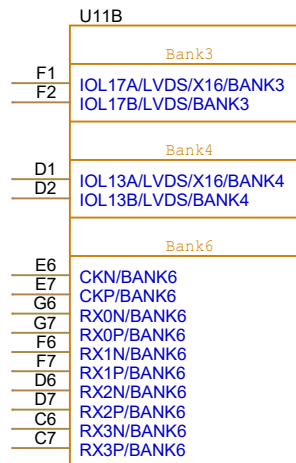
Notes:

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- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

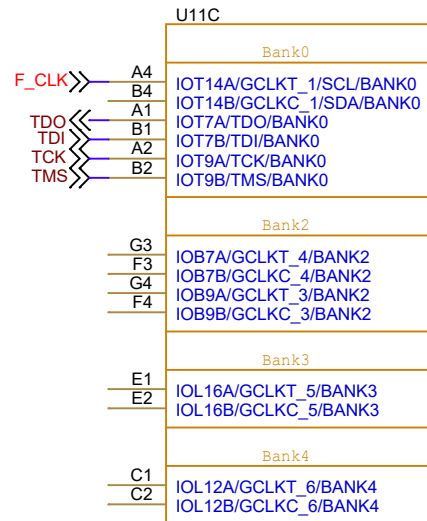
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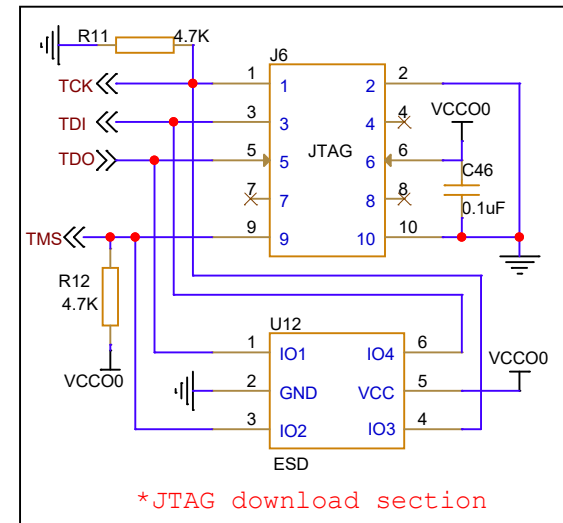
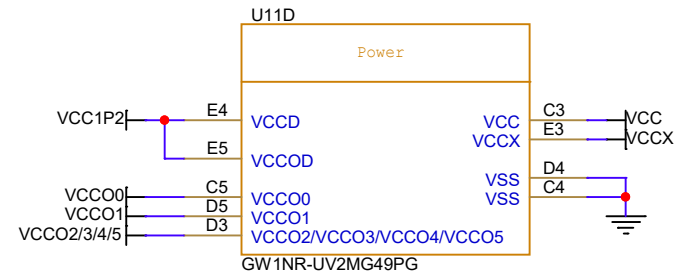
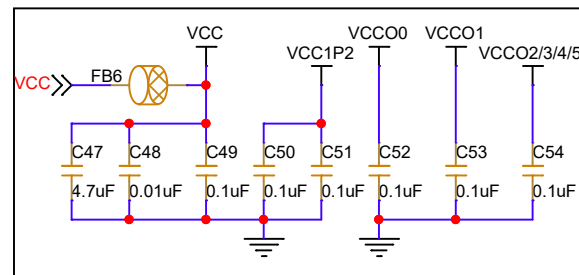
GW1NR-UV2MG49PG



GW1NR-UV2MG49PG



GW1NR-UV2MG49PG



## Notes:

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