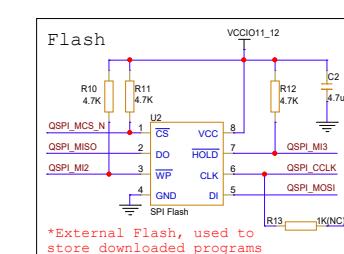
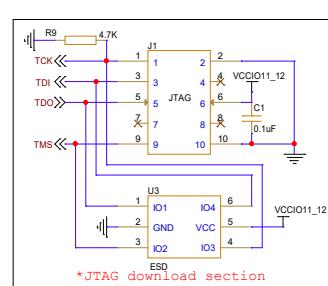
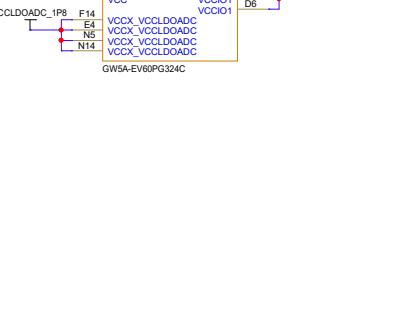
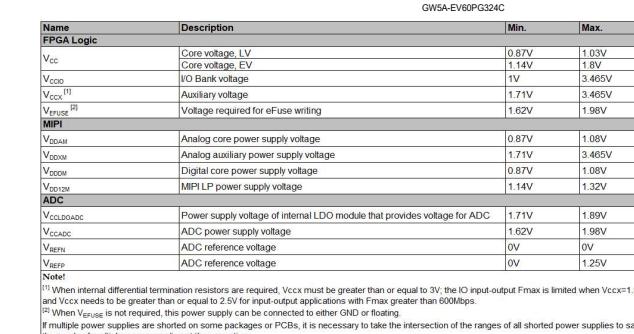
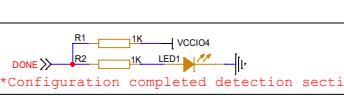
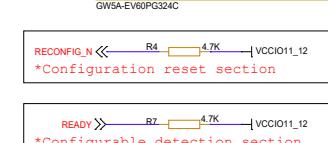
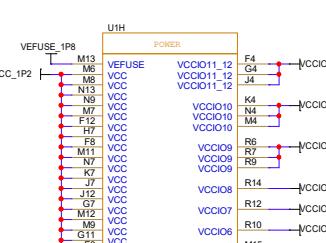
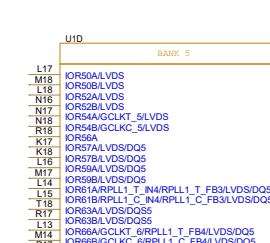
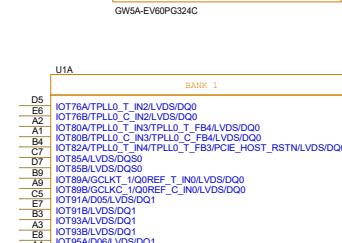
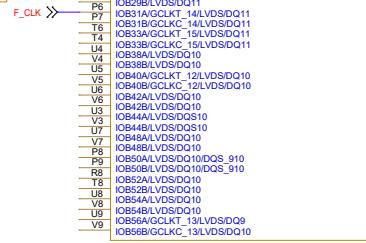
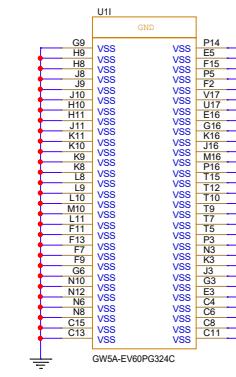
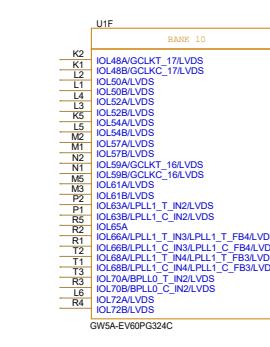
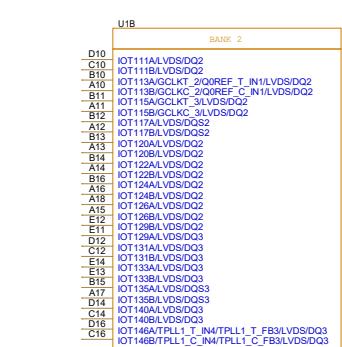
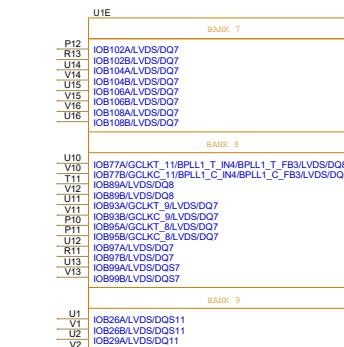
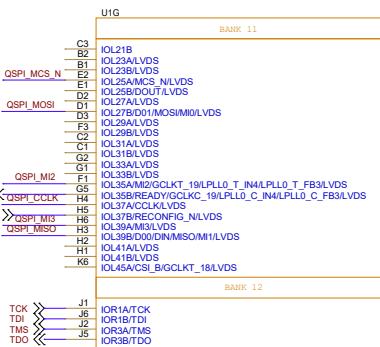


GW5A-EV60PG324C



Notes: ~~for six signals in one channel, one signal~~

It is recommended that F_CLK signal be provided through an active oscillator crystal.

For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718.

Arora V 60K FPGA Products Programming and Configuration Guide .
3. It is recommended that add an ESD protection chip to the JTAG download circuit.

4.VCC core voltage requires a large current, so it is recommended

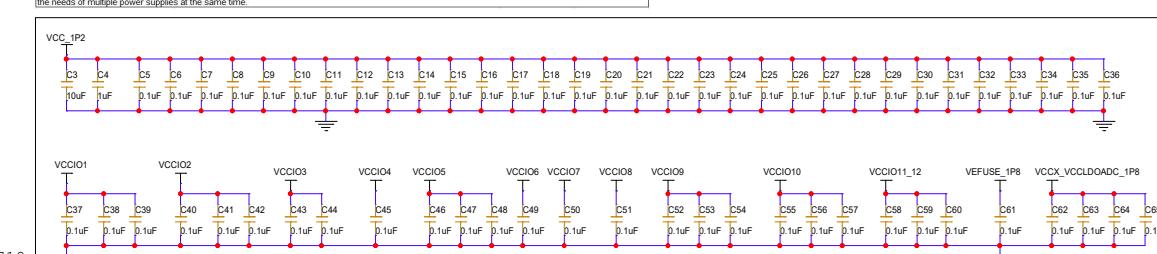
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG711.

For details about how to select the Mode signal, see Chapter 3.1 Configuration Modes.

6. This package does not support the use of internal differential termination resistor

This package does not support the use of internal differential termination resistor.

Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V _{CIO}	I/O Bank voltage	1V	3.465V
V _{CIOX} [1]	Auxiliary voltage	1.71V	3.465V
V _{FBUS} [2]	Voltage required for eFuse writing	1.62V	1.98V
MPI			
V _{DCAH}	Analog core power supply voltage	0.87V	1.08V
V _{DCAW}	Analog auxiliary power supply voltage	1.71V	3.465V
V _{DDM}	Digital core power supply voltage	0.87V	1.08V
V _{DDDM}	MPI/LP power supply voltage	1.14V	1.32V
ADC			
V _{COLDDAC}	Power supply voltage of internal LDO module that provides voltage for ADC	1.71V	1.89V
V _{CCADC}	ADC power supply voltage	1.62V	1.98V
V _{REFIN}	ADC reference voltage	0V	0V
V _{REFP}	ADC reference voltage	0V	1.25V
Note!			
[1]	When internal differential termination resistors are required, V _{CIOX} must be greater than or equal to 3V, the IO input-output Fmax is limited when V _{CIOX} =1, and V _{CIOX} needs to be greater than or equal to 2.5V for input-output applications with Fmax greater than 600Mbps.		
[2]	When V _{FBUS} is not required, this power supply can be connected to either GND or floating.		
If multiple power supplies are shorted on same packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the requirements.			

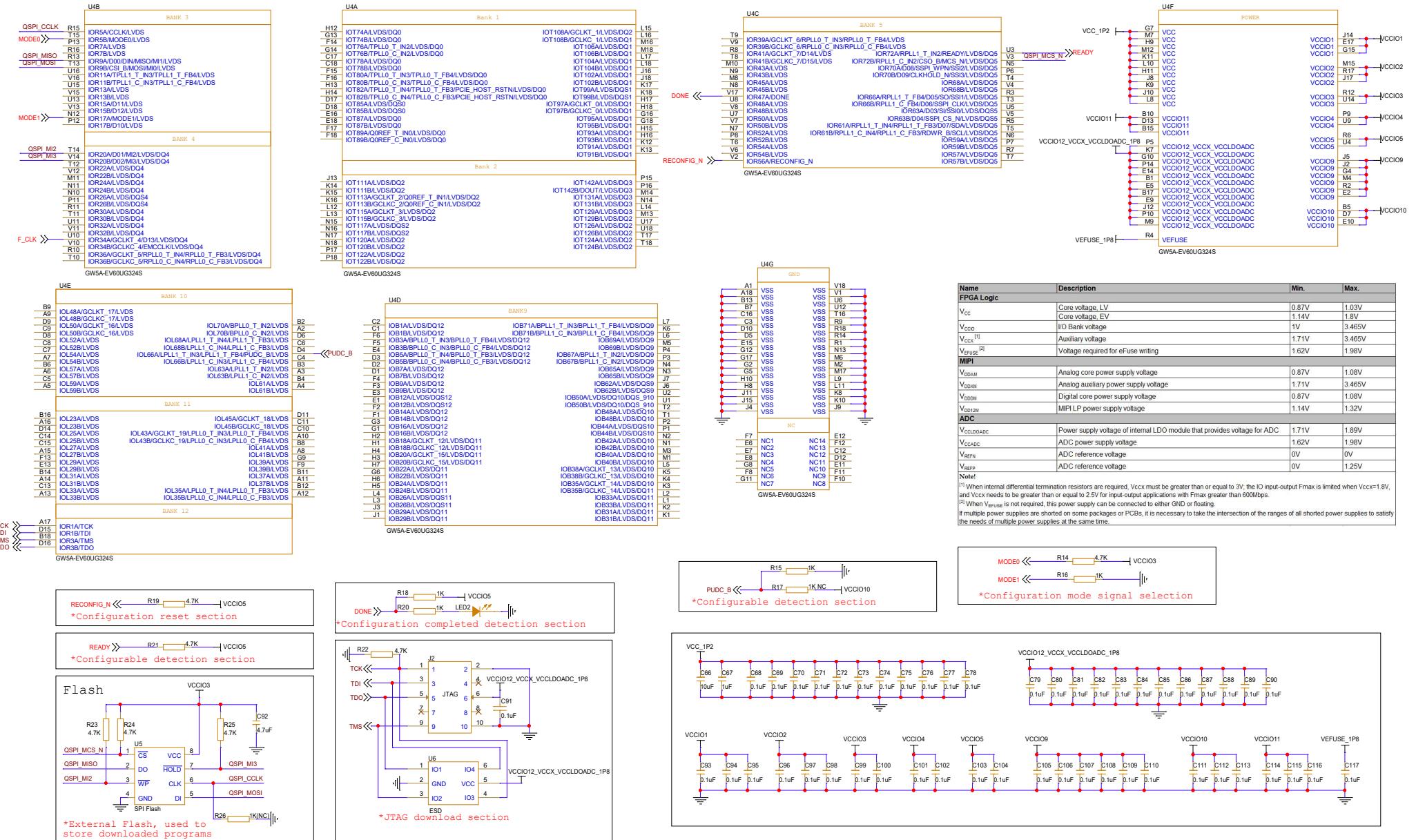


Title COWIN Minimum System Diagram

GOWIN Minimum System Diagram

C GW5A-EV60PG324C

GW5A-EV60UG324S



Notes:

1.F_CLK signal is an external input clock signal.

It is recommended that F_CLK signal be provided through an active driver.

2.External Flash memory is used to store downloaded programs.

For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Model Selection" in the Arora V 60K FRGA Products Programming and Configuration Guide.

3. It is recommended that add an ESD protection chip to the JTAG download circuit.

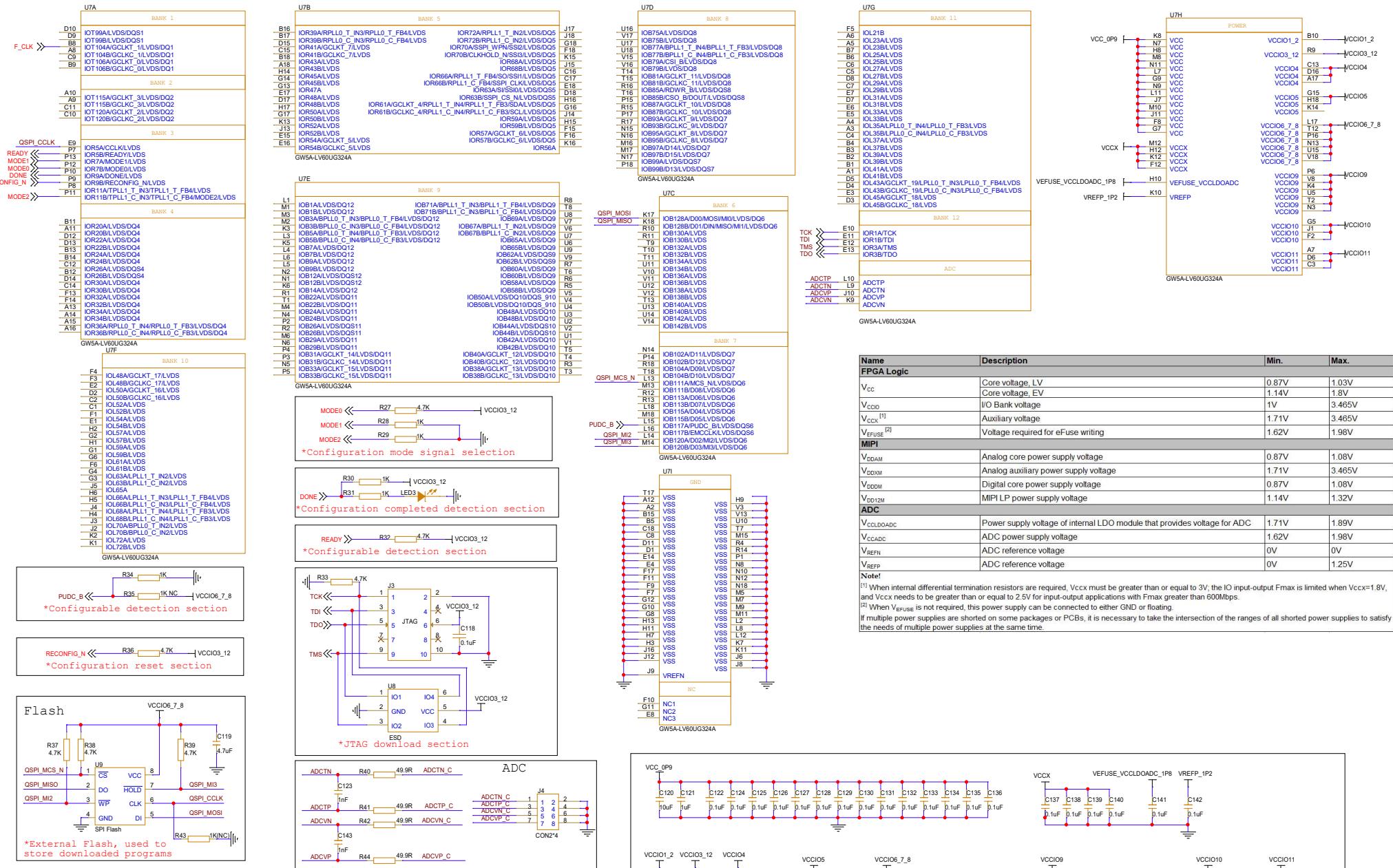
It is recommended that add an ESD protection chip to the STAG current, so it is recommended.

5.The MODE pin is the GowinCONFIG configuration mode selection s

For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718.

Title		
GOWIN Minimum System Diagram		
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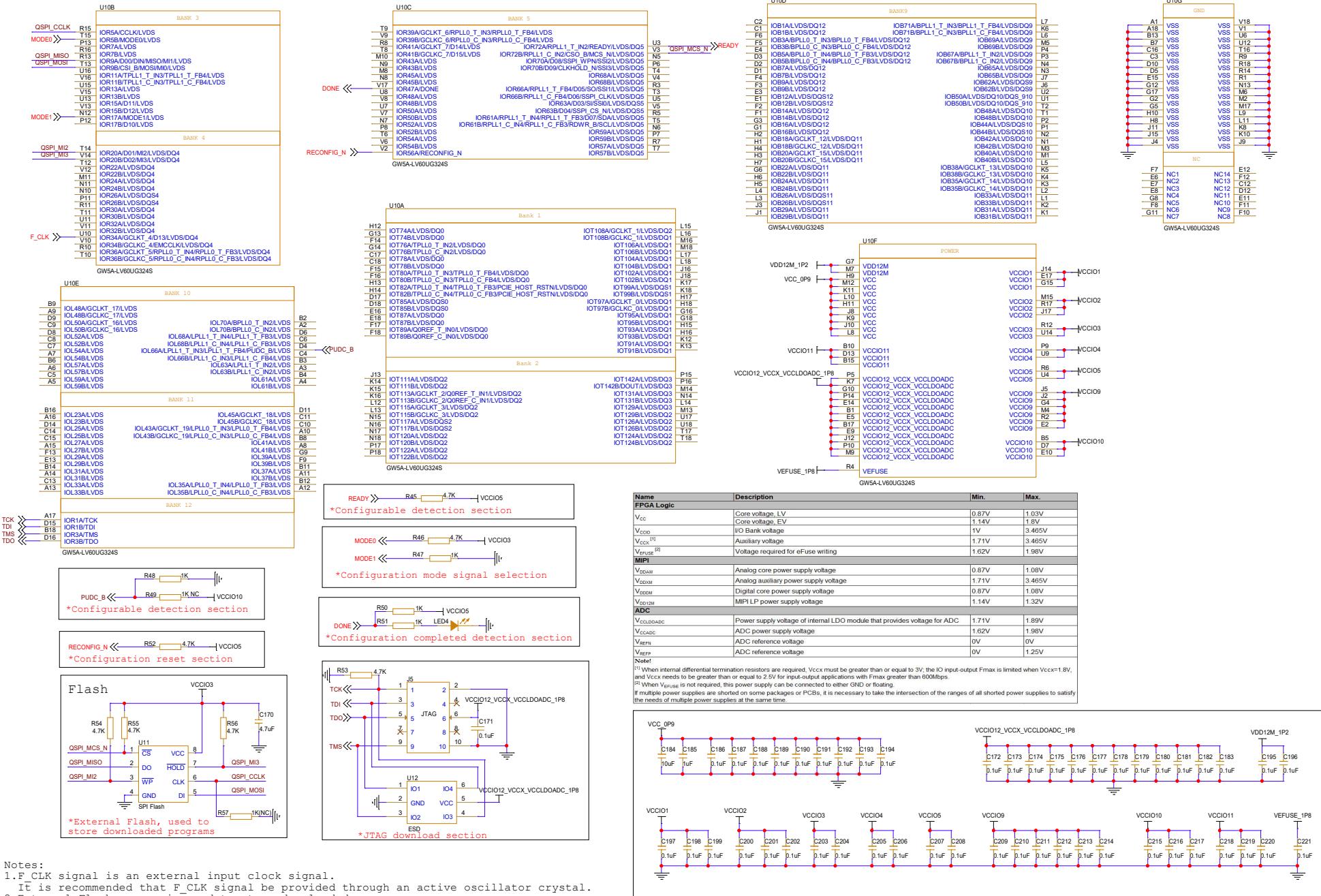


Notes:

1. F CLK signal is an external input clock signal.
- It is recommended that F CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide .
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. VCC core voltage requires a large current, so it is recommended to supply power separately.
5. The MODE pin is the Gowin CONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide .

Title		GOWIN Minimum System Diagram	
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Notes:

- F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Aurora V 60K FPGA Products Programming and Configuration Guide.
- It is recommended that add an ESD protection chip to the JTAG download circuit.
- VCC core voltage requires a large current, so it is recommended to supply power separately.
- The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Aurora V 60K FPGA Products Programming and Configuration Guide.

Name	Description	Min.	Max.
FPGA Logic			
V _{cc}	Core voltage, LV	0.67V	1.03V
V _{cc00}	I/O Bank voltage	1V	1.9V
V _{ccx} ⁽¹⁾	Auxiliary voltage	1.71V	3.465V
V _{EFUSE} ⁽²⁾	Voltage required for eFuse writing	1.62V	1.98V
MPI			
V _{DQAM}	Analog core power supply voltage	0.67V	1.08V
V _{DQAM}	Analog auxiliary power supply voltage	1.71V	3.465V
V _{DQDM}	Digital core power supply voltage	0.67V	1.08V
V _{DQDM}	MPII LP power supply voltage	1.4V	1.32V
ADC			
V _{COLDADC}	Power supply voltage of internal LDO module that provides voltage for ADC	1.71V	1.89V
V _{CADC}	ADC power supply voltage	1.62V	1.98V
V _{REFN}	ADC reference voltage	0V	0V
V _{REFP}	ADC reference voltage	0V	1.25V
Note!			
(1) When internal differential termination resistors are required, V _{ccx} must be greater than or equal to 3V; the IO input-output Fmax is limited when V _{ccx} =1.8V, and V _{ccx} needs to be greater than or equal to 2.5V for most applications with Fmax greater than 600Mbps.			
(2) Power V _{EFUSE} is not recommended for power supply, it should be connected to either GND or floating.			
If multiple power supplies are shared on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			

