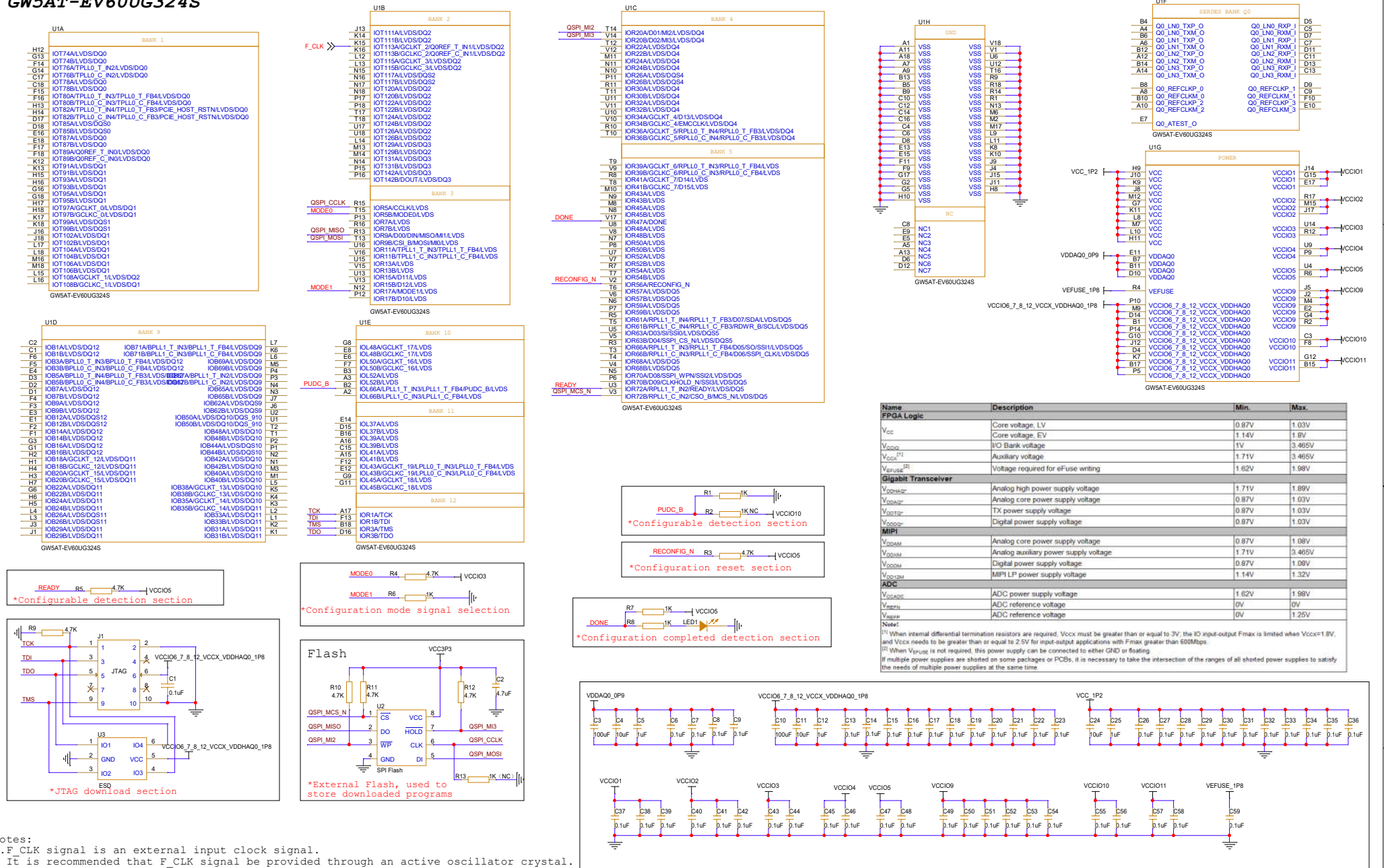


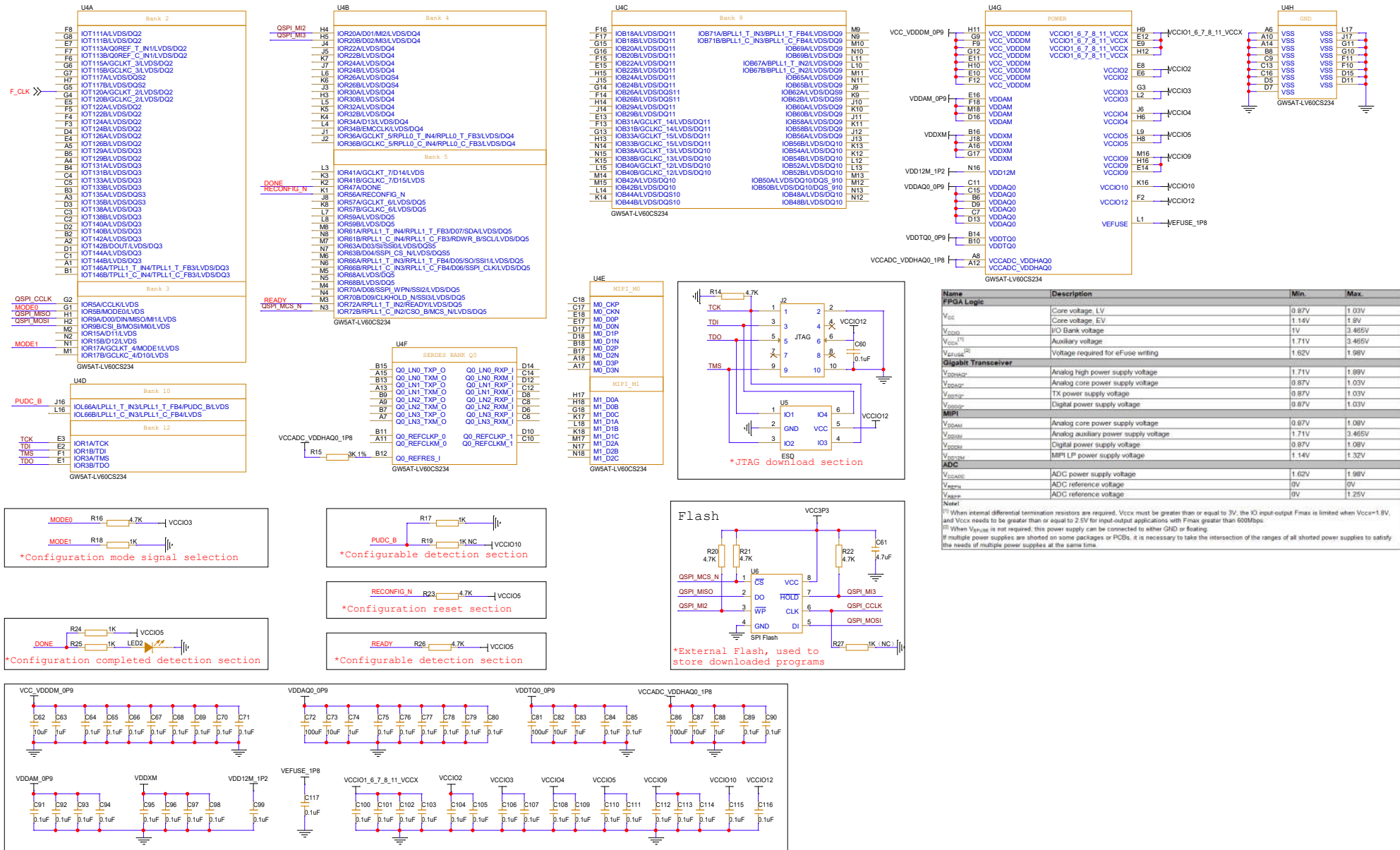
GW5AT-EV60UG324S



- The CLK signal is an external input clock signal.
- It is recommended that the CLK signal be provided through an active oscillator crystal.
- External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in the *U-200 V 60K FPGA Products Programming and Configuration Guide*.
- It is recommended that add an ESD protection chip to the JTAG download circuit.
- The VCC core voltage requires a large current, so it is recommended to supply power separately.
- The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in the *U-200 V 60K FPGA Products Programming and Configuration Guide*.
- This package does not support the use of internal differential termination resistors.
- The MSPI signal levels must match the Flash power supply voltage.
- If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

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GOWIN Minimum System Diagram			
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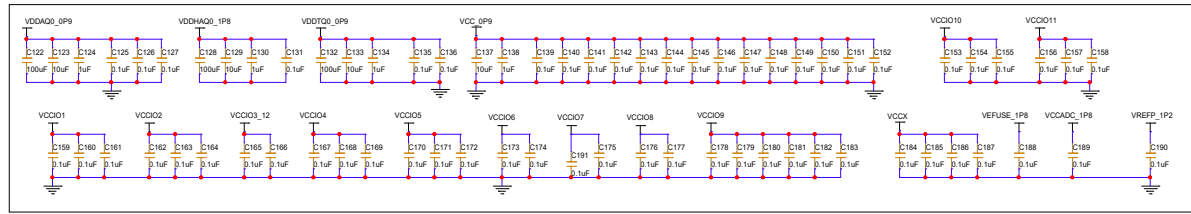
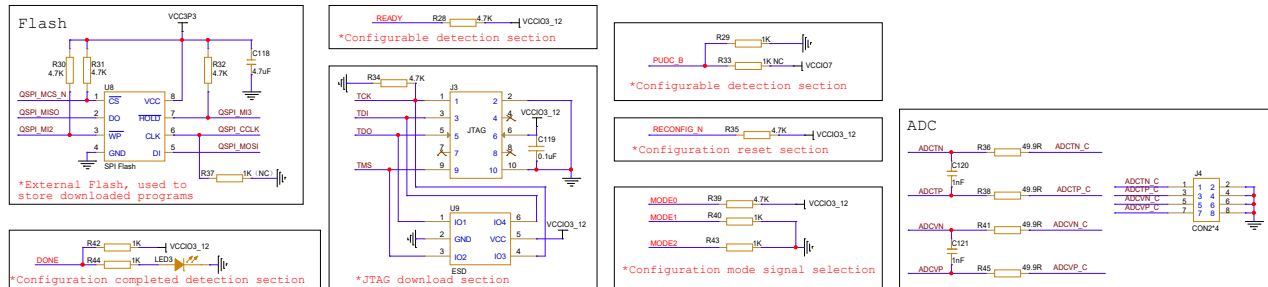
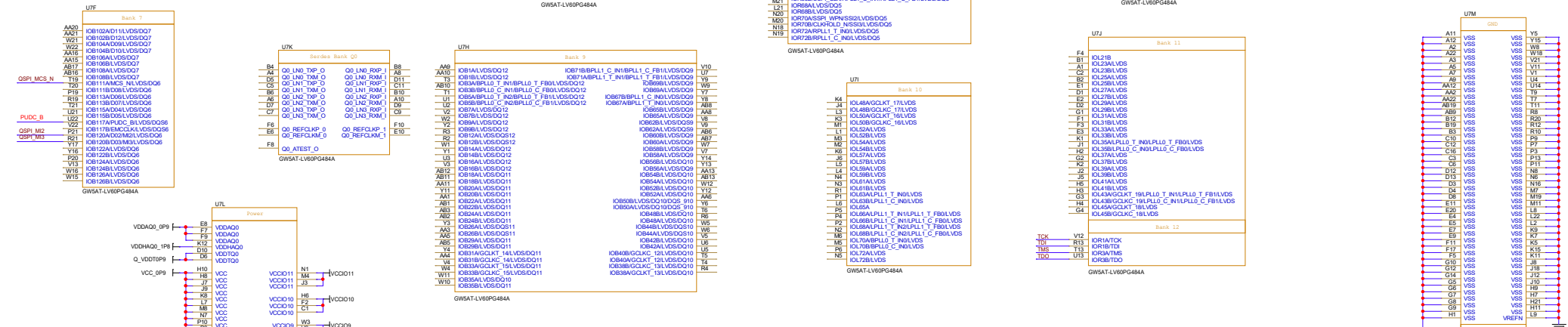
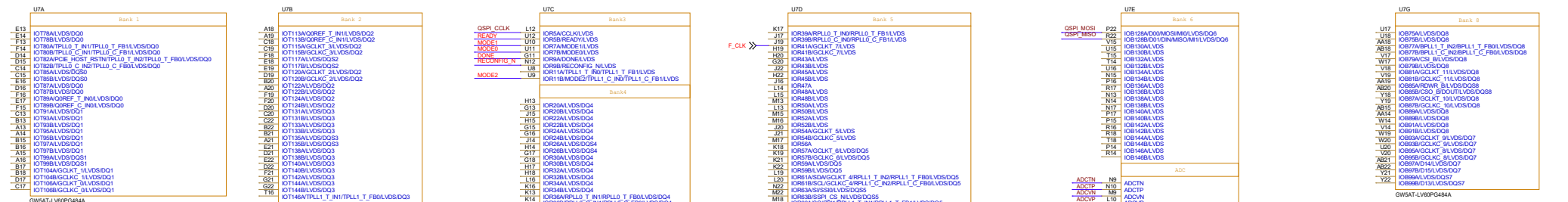
GW5AT-LV60CS234



- Notes:
- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.
 - 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
 - 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
 - 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.
 - 6.The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

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GW5AT-LV60PG484A



Pin	Description	Min.	Max.
GPIO Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
V _{CC}	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1V	3.405V
V _{CCIOH}	Auxiliary voltage	1.71V	3.465V
V _{CCIOH2}	Voltage required for eFuse writing	1.62V	1.98V
Signal Transceiver			
V _{ASUPP}	Analog high power supply voltage	1.71V	1.89V
V _{ASUPP2}	Analog core power supply voltage	0.87V	1.03V
V _{ASUPP3}	TX power supply voltage	0.87V	1.03V
V _{ASUPP4}	Digital power supply voltage	0.87V	0.87V
MPU			
V _{ASUPP}	Analog core power supply voltage	0.87V	1.06V
V _{ASUPP2}	Analog auxiliary power supply voltage	1.71V	2.465V
V _{ASUPP3}	Digital power supply voltage	0.87V	0.86V
V _{ASUPP4}	MPU LP power supply voltage	1.14V	1.32V
ADC			
V _{ASUPP0}	ADC power supply voltage	1.62V	1.98V
V _{ASUPP1}	ADC reference voltage	0V	0V
V _{ASUPP2}	ADC reference voltage	0V	1.25V
None			

Notes:

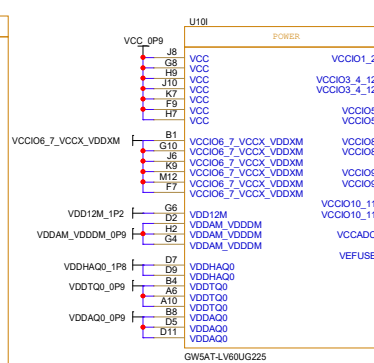
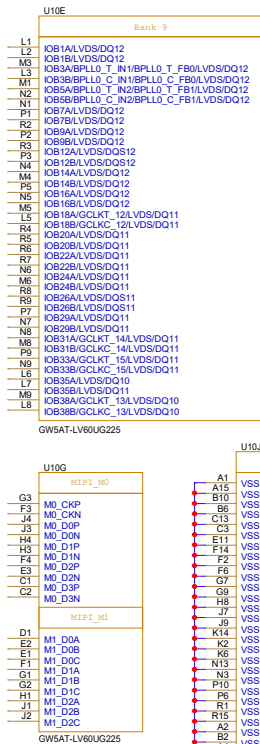
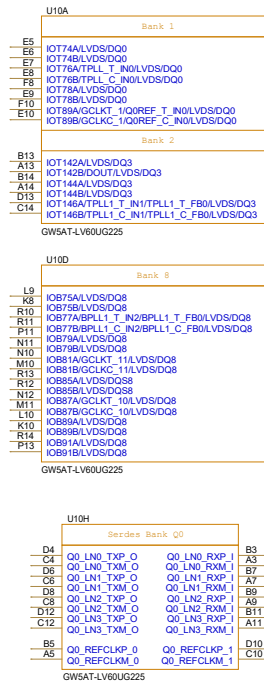
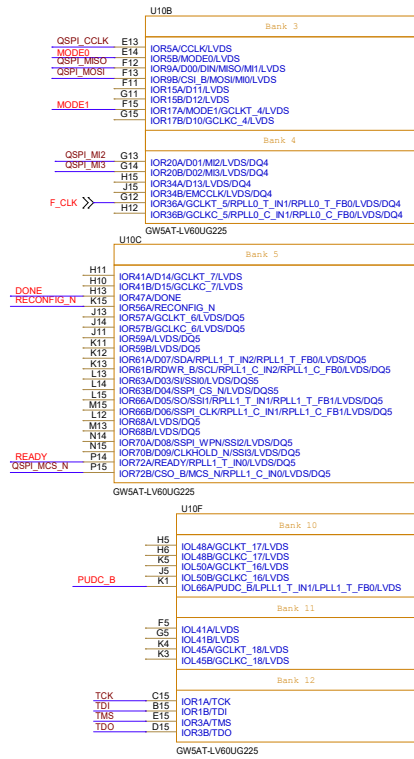
- 1.F.CLK signal is an external input clock signal.
 - It is recommended that F.CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
 - For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Arara V 60K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.

For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arara V 60K FPGA Products Programming and Configuration Guide .

The MSPI signal levels must match the Flash power supply voltage.

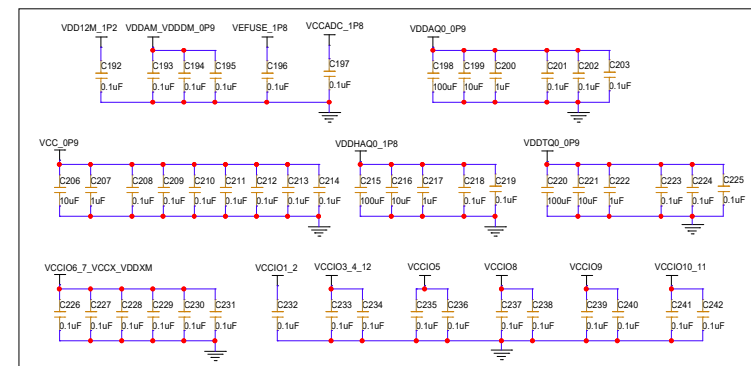
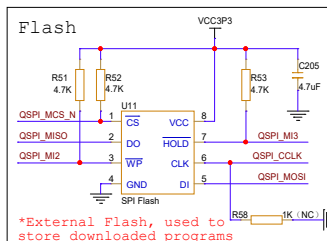
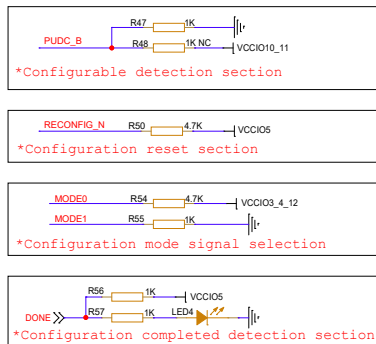
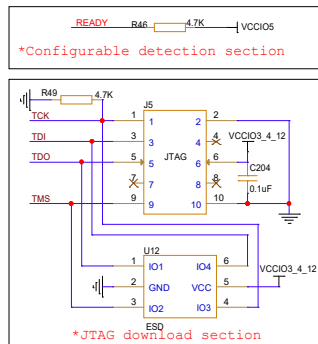
If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

GW5AT-LV60UG225



Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
V _{CCIO}	Core voltage, EV	1.14V	1.8V
V _{CCIO1}	I/O Bank voltage	1V	3.465V
V _{CCIO11}	Auxiliary voltage	1.71V	3.465V
V _{EFUSE} ¹⁰	Voltage required for eFuse writing	1.62V	1.98V
Gigabit Transceiver			
V _{SDHNA2}	Analog high power supply voltage	1.71V	1.89V
V _{SDHNA2P}	Analog core power supply voltage	0.87V	1.03V
V _{SDHNA2T}	TX power supply voltage	0.87V	1.03V
V _{SDHNA2D}	Digital power supply voltage	0.87V	1.03V
MIPI			
V _{SDHNA1}	Analog core power supply voltage	0.87V	1.08V
V _{SDHNA1P}	Analog auxiliary power supply voltage	1.71V	3.465V
V _{SDHNA1D}	Digital power supply voltage	0.87V	1.08V
V _{SDHNA1M}	MIPI LP power supply voltage	1.14V	1.32V
ADC			
V _{CCADC}	ADC power supply voltage	1.62V	1.98V
V _{AREF1}	ADC reference voltage	0V	0V
V _{AREF2}	ADC reference voltage	0V	1.25V

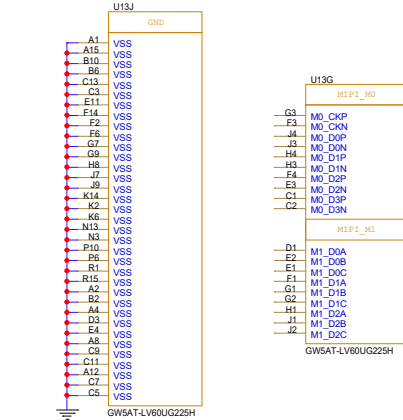
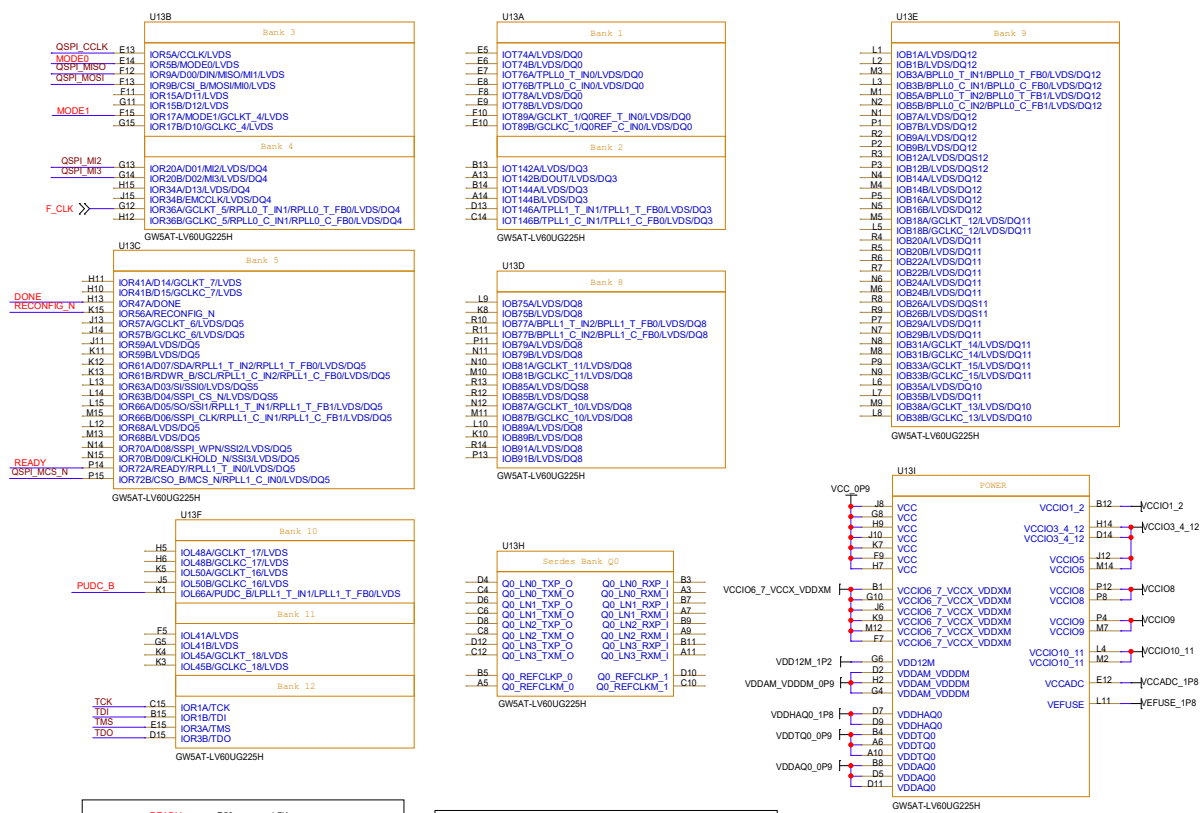
[2] When $V_{DD,REG}$ is not required, this power supply can be connected to either GND or floating.



Notes:

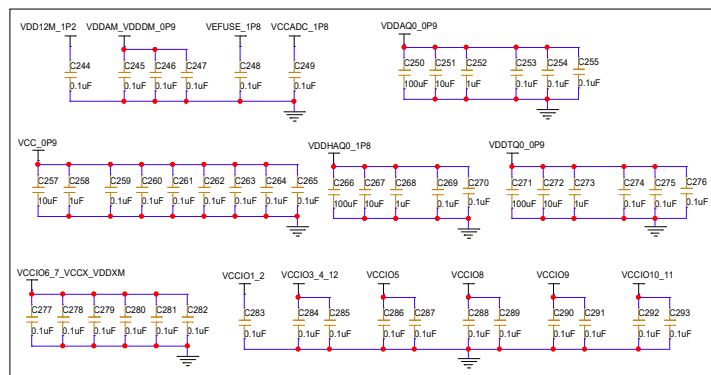
- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

GW5AT-LV60UG225H



Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1V	3.465V
V _{CCM} ⁽¹⁾	Auxiliary voltage	1.71V	3.465V
V _{EFUSE} ⁽²⁾	Voltage required for eFUSE writing	1.62V	1.98V
Gigabit Transceiver			
V _{DDAAG} ⁽³⁾	Analog high power supply voltage	1.71V	1.89V
V _{DDA2P} ⁽³⁾	Analog core power supply voltage	0.87V	1.03V
V _{DDT2P} ⁽³⁾	TX power supply voltage	0.87V	1.03V
V _{DDODD} ⁽³⁾	Digital power supply voltage	0.87V	1.03V
MIPI			
V _{DDMI}	Analog core power supply voltage	0.87V	1.08V
V _{DDMI2}	Analog auxiliary power supply voltage	1.71V	3.465V
V _{DDMI3}	Digital power supply voltage	0.87V	1.08V
V _{DDMI2M}	MIPI LP power supply voltage	1.14V	1.32V
ADC			
V _{LOGADC}	ADC power supply voltage	1.62V	1.98V
V _{AREF1}	ADC reference voltage	0V	0V
V _{AREF2}	ADC reference voltage	0V	1.25V

[2] When $V_{DS,REG}$ is not required, this power supply can be connected to either GND or floating.

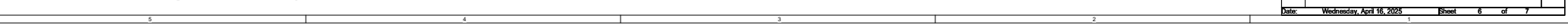
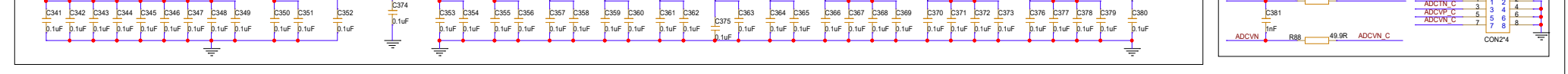
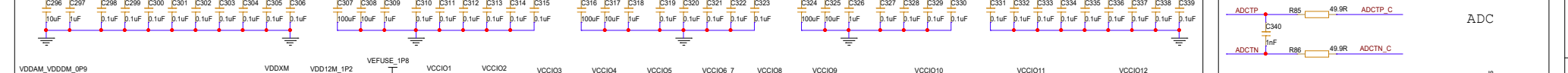
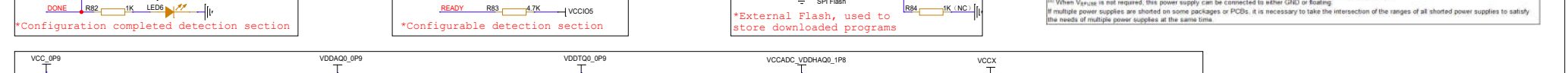
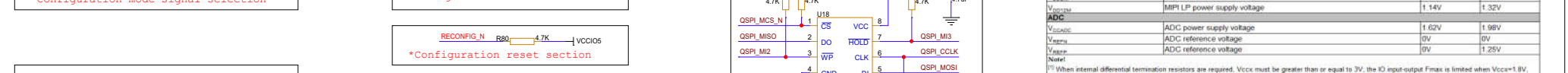
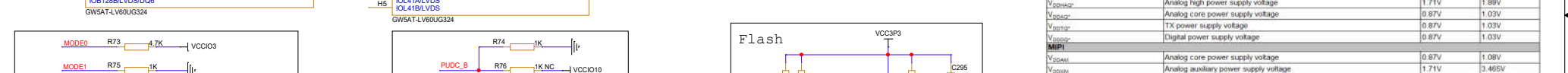
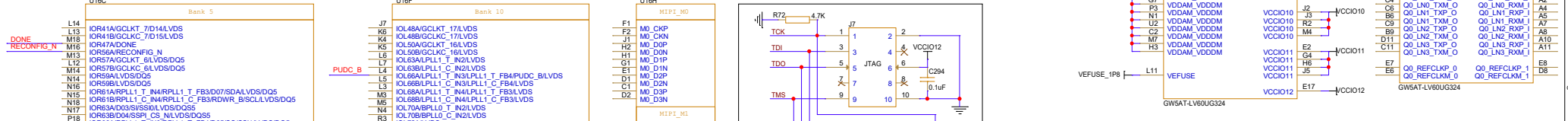


Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage,
a level shifter is required for voltage translation.

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GOWIN Minimum System Diagram			
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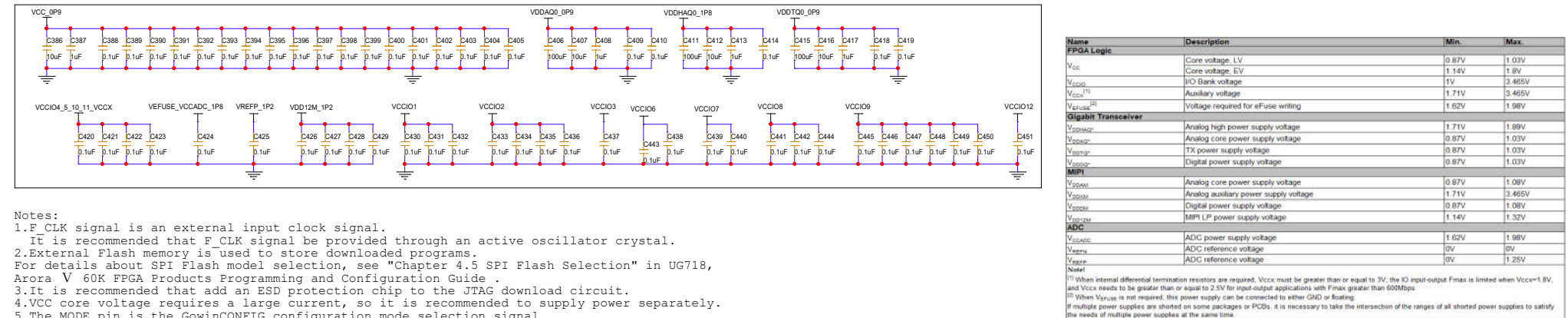
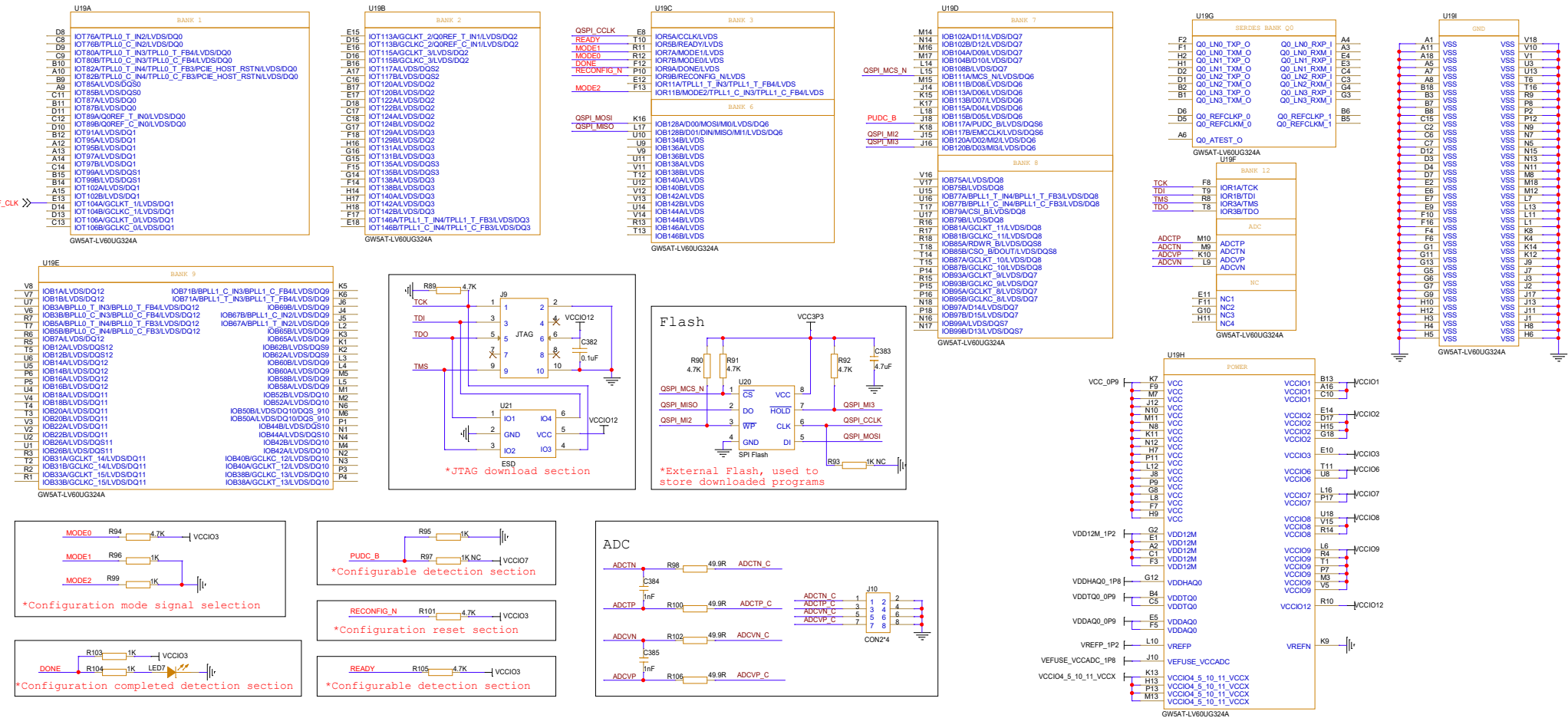


Notes:

- 1.F CLK signal is an external input clock signal.
- 1.F is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
- For details about SPI Flash selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.
- If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

File		
GOWIN Minimum System Diagram		
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GW5AT-LV60UG324A



Notes:

- 1.F CLK signal is an external input clock signal.
- It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.
- If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
V _{CC}	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1V	3.465V
V _{CCIO1}	Auxiliary voltage	1.71V	3.465V
V _{CCIO2}	Voltage required for eFuse writing	1.62V	1.98V
Gigabit Transceiver			
V _{CCIO3}	Analog high power supply voltage	1.71V	1.89V
V _{CCIO4}	Analog core power supply voltage	0.87V	1.03V
V _{CCIO5}	TX power supply voltage	0.87V	1.03V
V _{CCIO6}	Digital power supply voltage	0.87V	1.03V
MIPI			
V _{CCIO7}	Analog core power supply voltage	0.87V	1.08V
V _{CCIO8}	Analog auxiliary power supply voltage	1.71V	3.465V
V _{CCIO9}	Digital power supply voltage	0.87V	1.08V
V _{CCIO10}	MIPI LP power supply voltage	1.14V	1.32V
ADC			
V _{CCIO11}	ADC power supply voltage	1.62V	1.98V
V _{CCIO12}	ADC reference voltage	0V	0V
V _{CCIO13}	ADC reference voltage	0V	1.25V