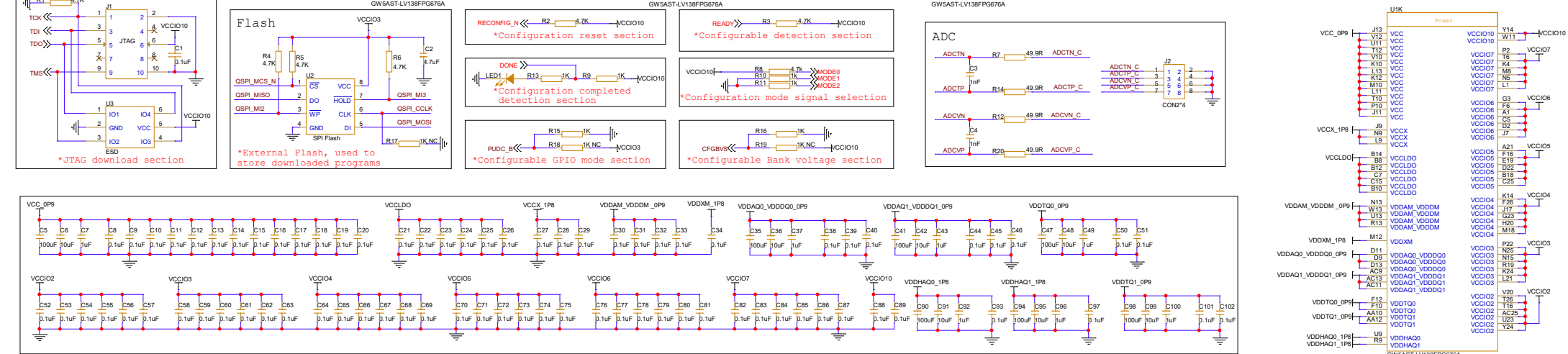


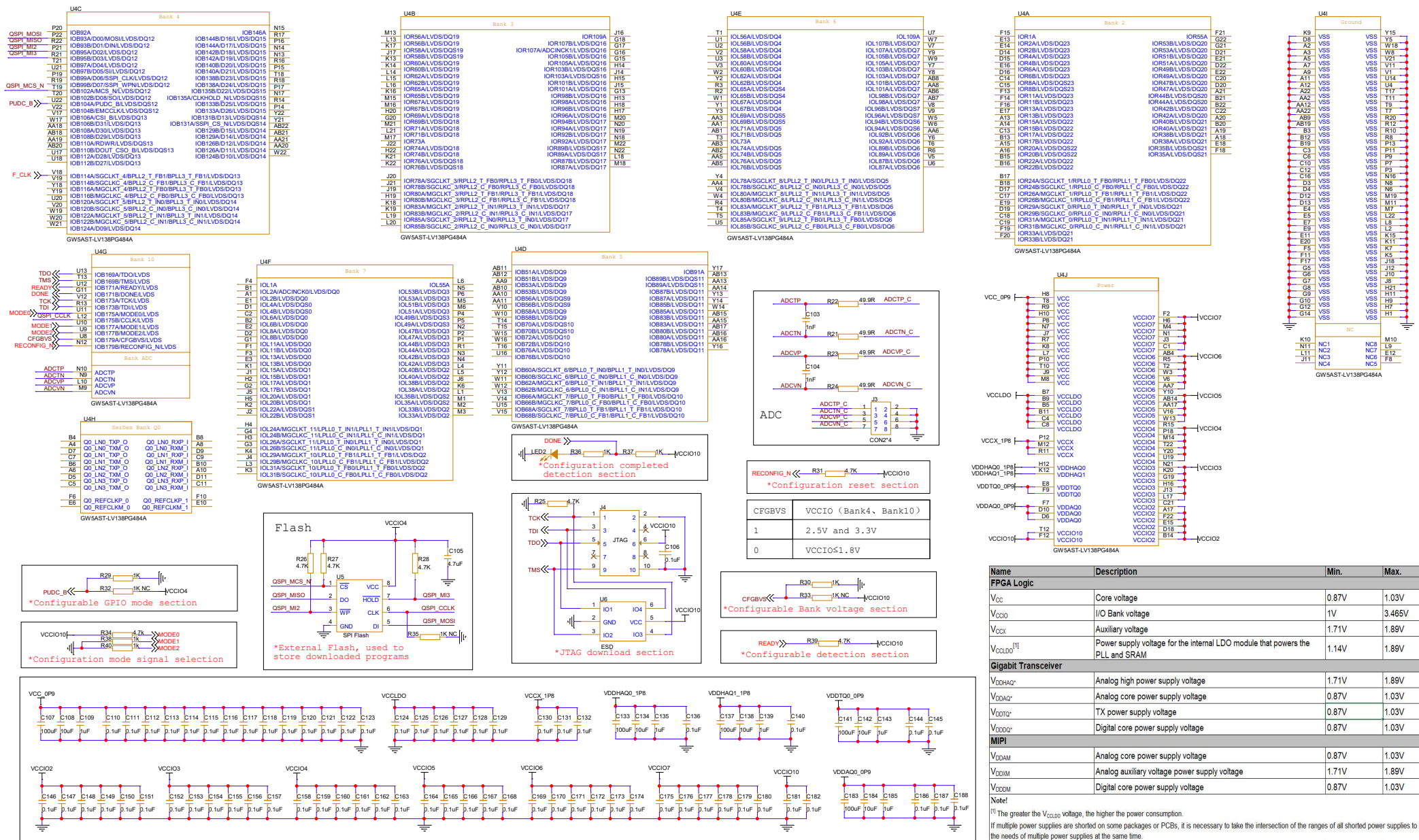
U0		Rank 0	
TDO	J10	IOB169A/TDO/LVDS	
TMS	V11	IOB169B/TMS/VLDS	
READY	H11	IOB171A/READY/LVDS	
DONE	W10	IOB171B/DONE/LVDS	
TDK	H10	IOB173A/TCK/LVDS	
	H10	IOB173B/TCK/LVDS	
DE0	AB7	IOB175A/MODE0/LVDS	
OSPI_CLK	VB9	IOB175B/OSPI_CLK/LVDS	
	W6	IOB177A/MODE1/LVDS	
MODE	AB15	IOB177B/MODE2/LVDS	
CFG0	AE18	IOB178B/CFG0/LVDS	
RECONFIG_N		IOB178B/RECONF_N/LVDS	
		Rank ADC	
ADCTP	R12	ADCTP	
ADCTN	R11	ADCTN	
ADCP	N12	ADCP	
ADCVN	P11	ADCVN	



^[1] The greater the V_{CCDO} voltage, the higher the power consumption.

Title				
GOWIN Minimum System Diagram				
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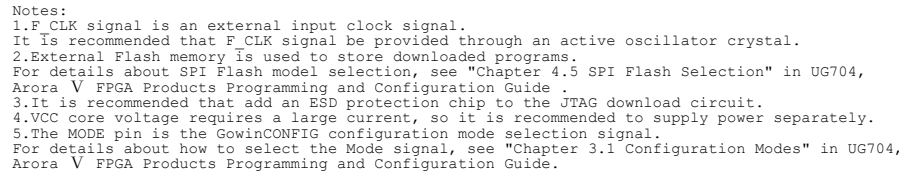
Notes:

1. F_CLK signal is an external input clock signal.
- It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG704, Arora V FPGA Products Programming and Configuration Guide .
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. VCC core voltage requires a large current, so it is recommended to supply power separately.
5. The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, Arora V FPGA Products Programming and Configuration Guide.

¹⁷⁾ The greater the V_{CCLOD} voltage, the higher the power consumption.

Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage	0.87V	1.03V
V _{CCIO}	I/O Bank voltage	1V	3.465V
V _{CCX}	Auxiliary voltage	1.71V	1.89V
V _{COLDO} ⁽¹⁾	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	1.89V
Gigabit Transceiver			
V _{DDHAQ*}	Analog high power supply voltage	1.71V	1.89V
V _{DDAQ*}	Analog core power supply voltage	0.87V	1.03V
V _{DDTQ*}	TX power supply voltage	0.87V	1.03V
V _{DDDG*}	Digital core power supply voltage	0.87V	1.03V
MIPI			
V _{DDAM}	Analog core power supply voltage	0.87V	1.03V
V _{DDIM}	Analog auxiliary voltage power supply voltage	1.71V	1.89V
V _{DDDM}	Digital core power supply voltage	0.87V	1.03V

¹⁷⁾ The greater the V_{CCLOD} voltage, the higher the power consumption.



CFGVBS	VCCIO (Bank4、Bank10)
1	2.5V and 3.3V
0	VCCIO≤1.8V