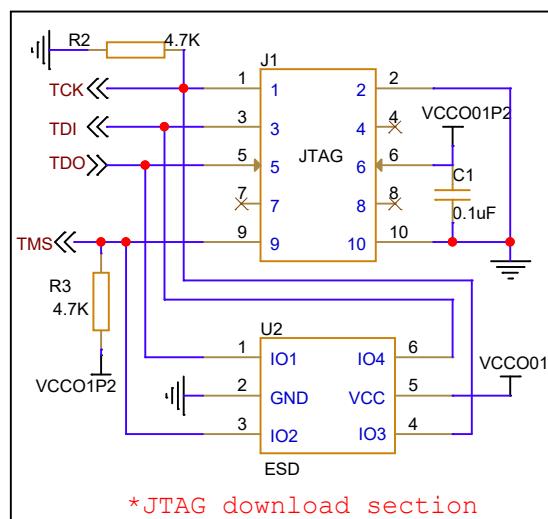
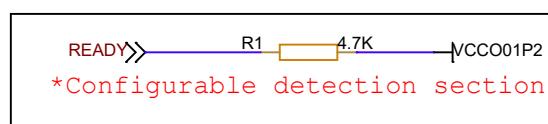
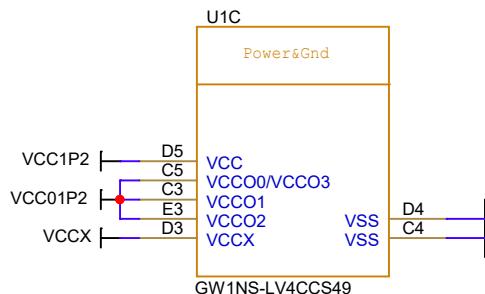
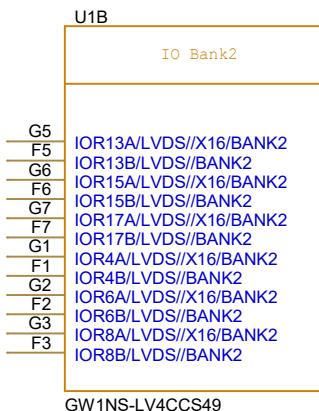
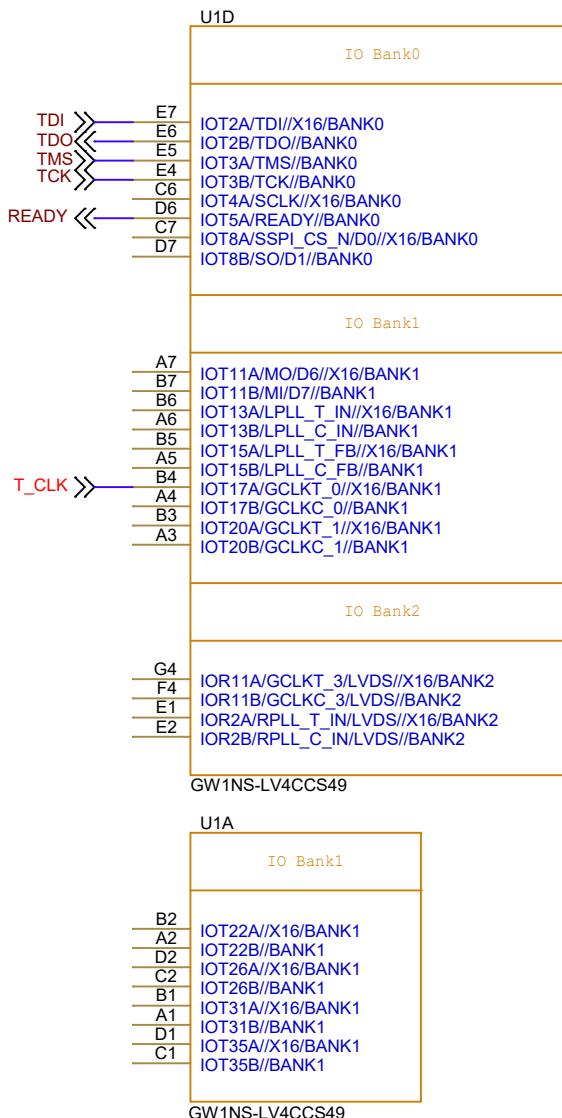
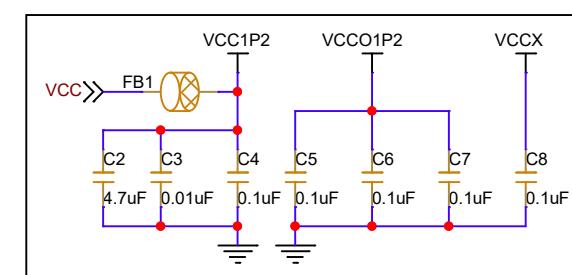


GW1NS-LV4CCS49



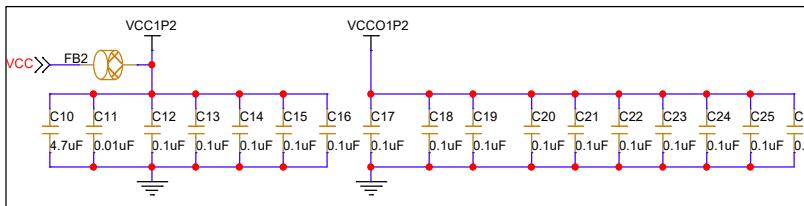
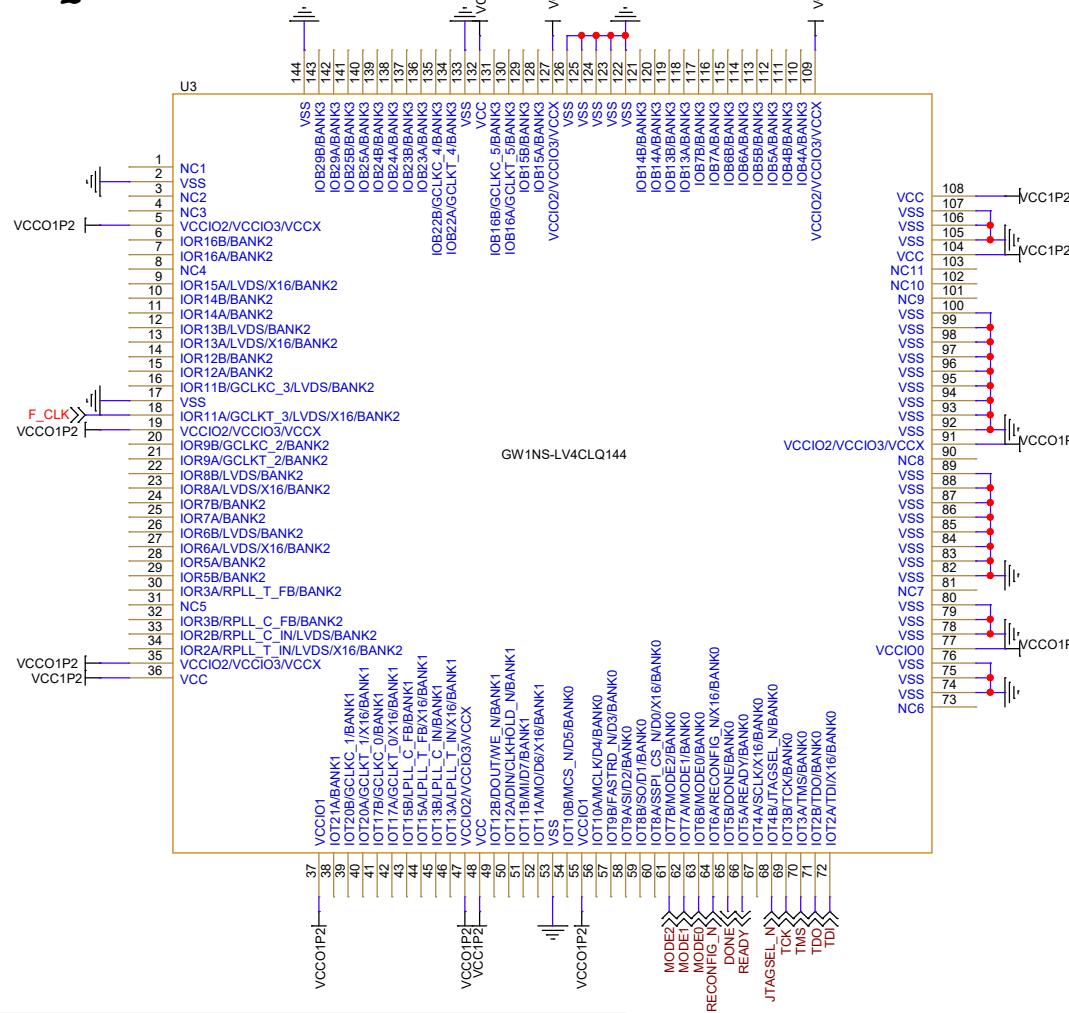
Name	Description	Min.	Max.
VCC	Core voltage	1.14V	1.26V
VCCIO1, VCCIO2	I/O Bank voltage When MiPi input is used in BANK1, VCCIO1 should provide 1.2V voltage. When MiPi output is used in BANK2, VCCIO2 should provide 1.2V voltage.	1.14V	3.6V
VCCIO0/VCCIO3	I/O Bank voltage, VCCIO0/VCCIO3 are internally connected. When MiPi input is used in BANK0, VCCIO0 should provide 1.2V voltage.	1.14V	3.6V
VCCX	Auxiliary voltage	1.71V	3.6V

VCCX should be greater than or equal to VCCIO.



Notes:

1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.
3. The CS49 package supports GW1NS-4 & GW1NS-4C.



Recommended Operating Conditions of LQ144 Package in GW1NS-4C

Name	Description	Min.	Max.
VCC	Core voltage	1.14V	1.26V
VCCIO0, VCCIO1	I/O Bank voltage When MIPI input is used in BANK0 and BANK1, VCCIO0 and VCCIO1 should provide 1.2V voltage.	1.14V	3.6V
VCCIO2/VCCIO3/VCCX	I/O Bank voltage VCCIO2/VCCIO3 and auxiliary voltage VCCX are internally connected. When MIPI output is used in BANK2, VCCIO2 should provide 1.2V voltage.	1.71V	3.6V

VCCX should be greater than or equal to VCCIO.

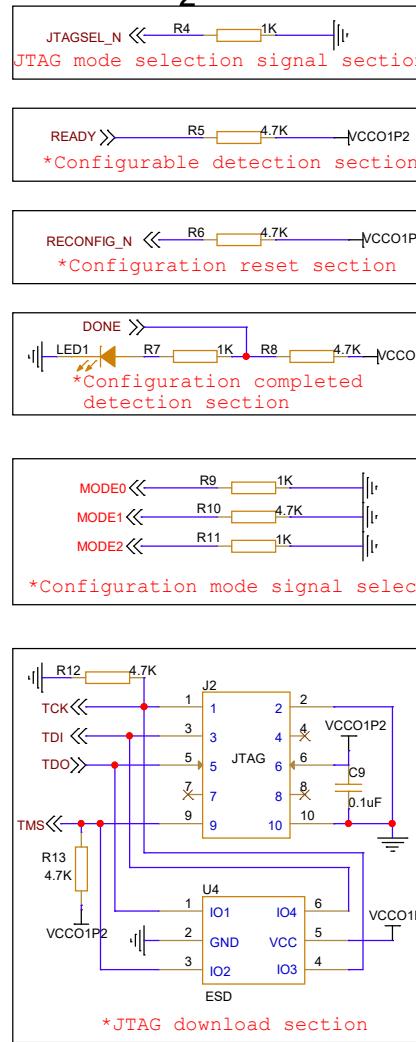
Notes:

1. F_CLK signal is an external input clock signal.

It is recommended that F_CLK signal be provided through an active oscillator crystal.

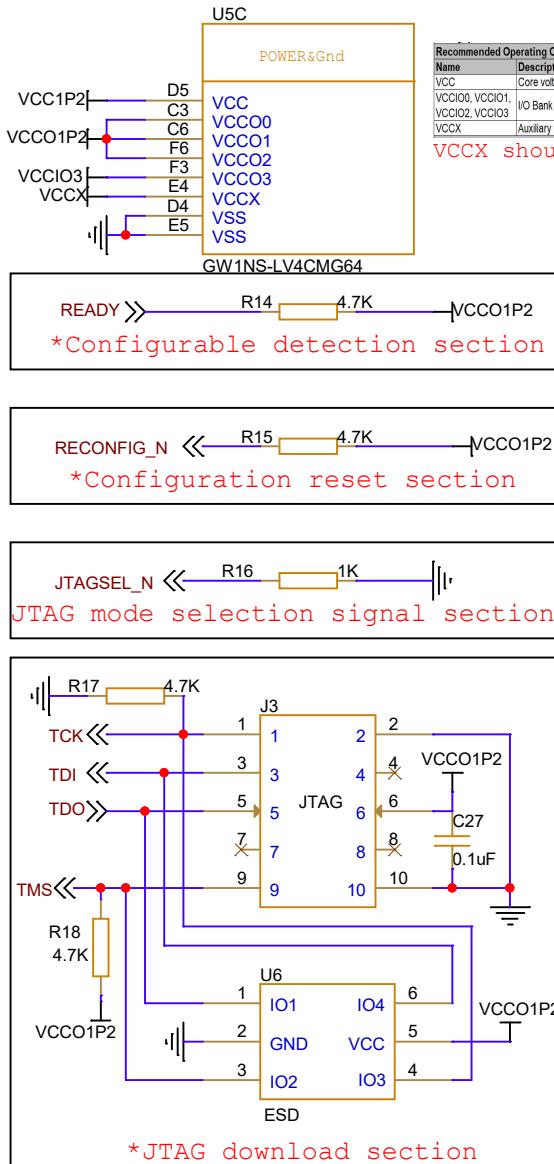
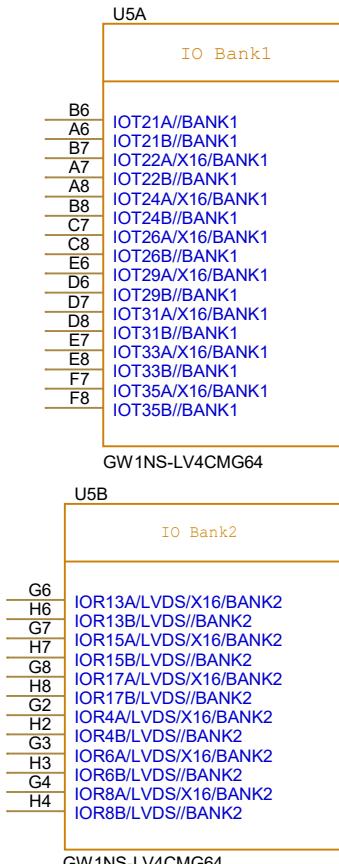
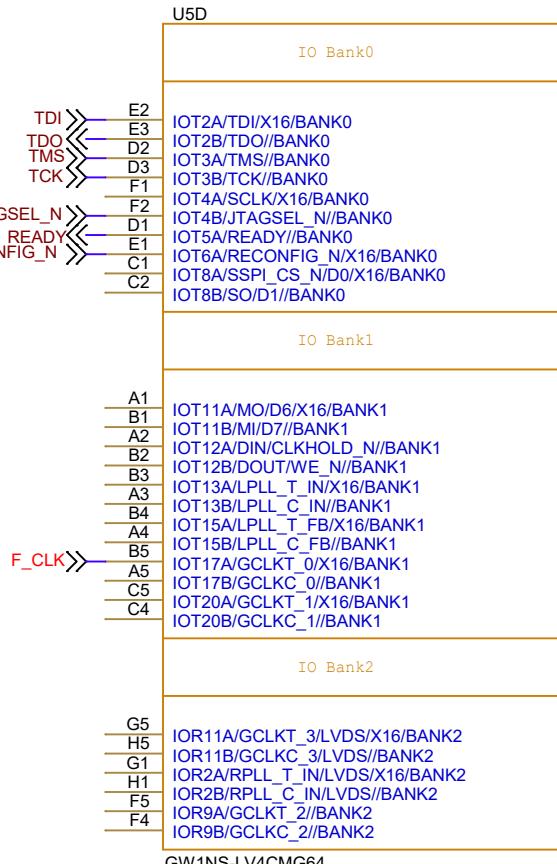
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

3. The MG64 package supports GW1NS-4 & GW1NS-4C.



Title	
GOWIN Minimum System Diagram	
Size	Document Number GW1NS-LV4CLQ144
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GW1NS-LV4CMG64

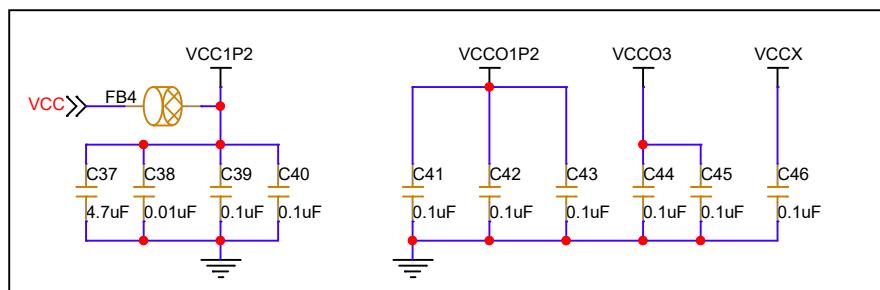
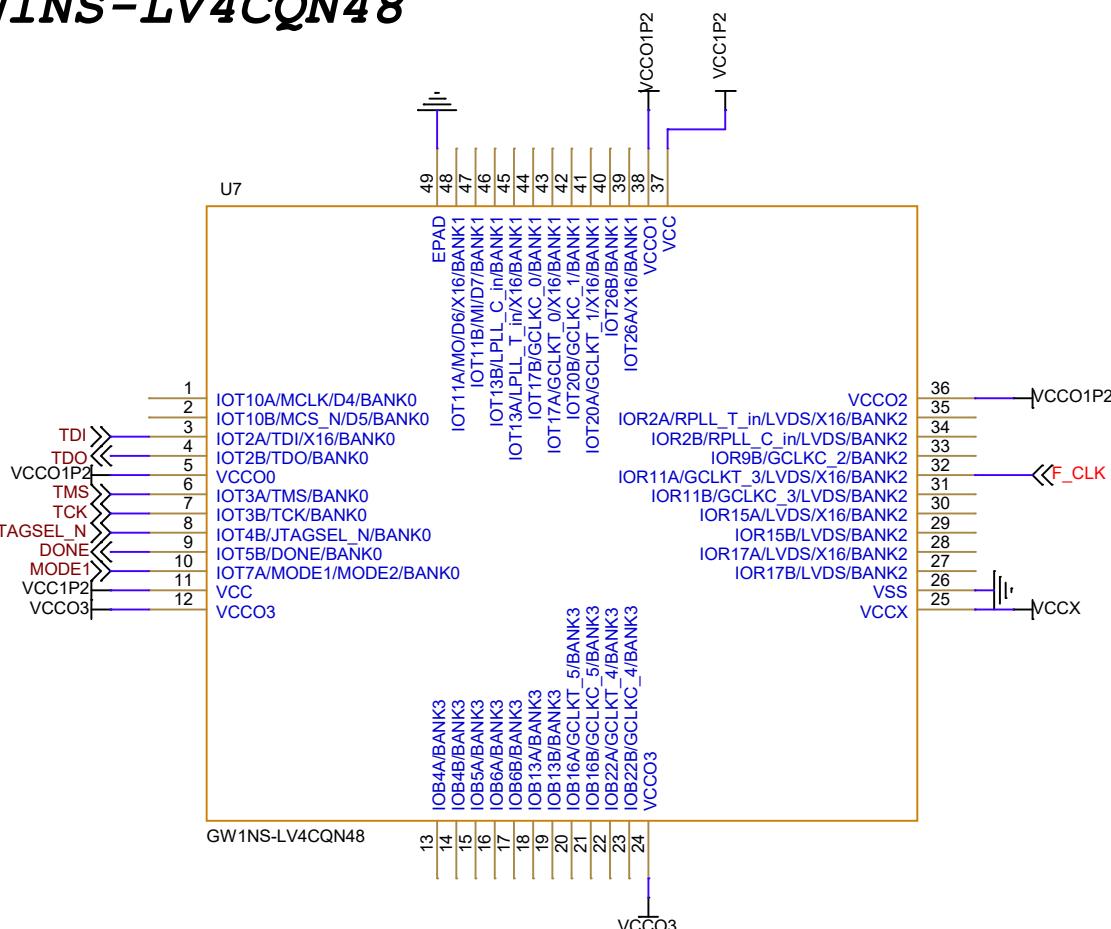


Notes:

1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.
3. The MG64 package supports GW1NS-4 & GW1NS-4C.

Title	
GOWIN Minimum System Diagram	
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GW1NS-LV4CQN48



Notes:

1. F_CLK signal is an external input clock signal.

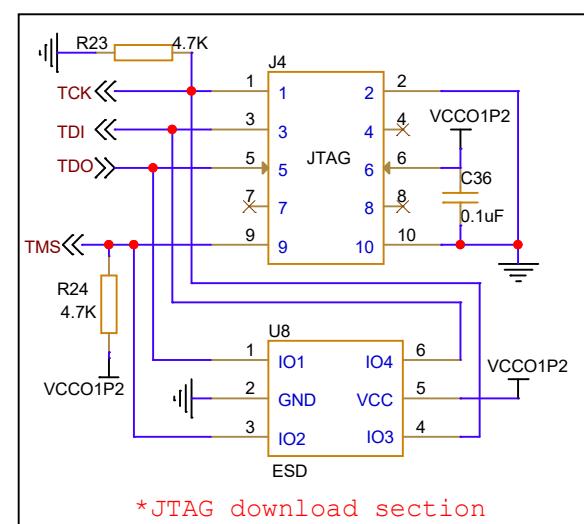
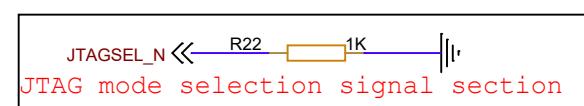
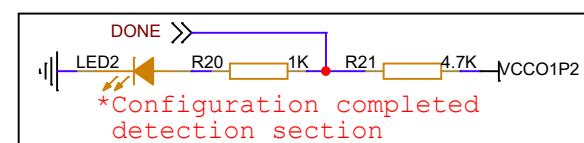
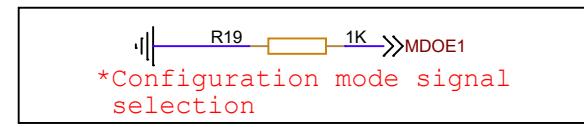
It is recommended that F_CLK signal be provided through an active oscillator crystal.

2. It is recommended that add an ESD protection chip to the JTAG download circuit.

3. The QN48 package supports GW1NS-4 & GW1NS-4C.

Recommended Operating Conditions of QN48 Package in GW1NS-4/GW1NS-4C			
Name	Description	Min.	Max.
VCC	Core voltage	1.14V	1.26V
VCCIO1, VCCIO2, VCCIO3	I/O Bank voltage When MIPI input is used in BANK0 and BANK1, VCCIO1 and VCCIO2 should provide 1.2V voltage. When MIPI output is used in BANK2, VCCIO2 should provide 1.2V voltage.	1.14V	3.6V
VCCX	Auxiliary voltage	1.71V	3.6V
Note! It is highly recommended that the EPAD connect to GND, but not a requirement.			

VCCX should be greater than or equal to VCCIO.



*JTAG download section

Title GOWIN Minimum System Diagram

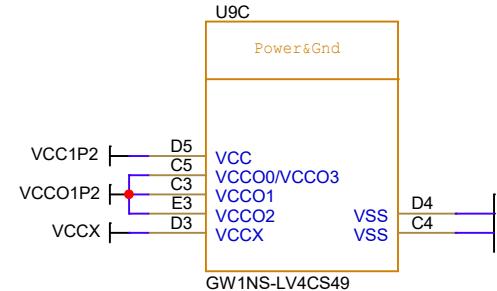
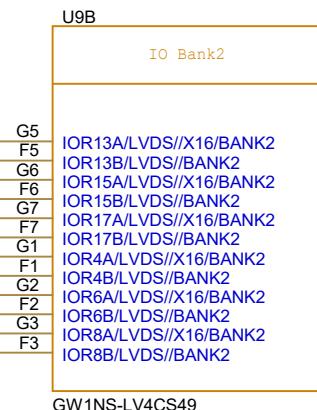
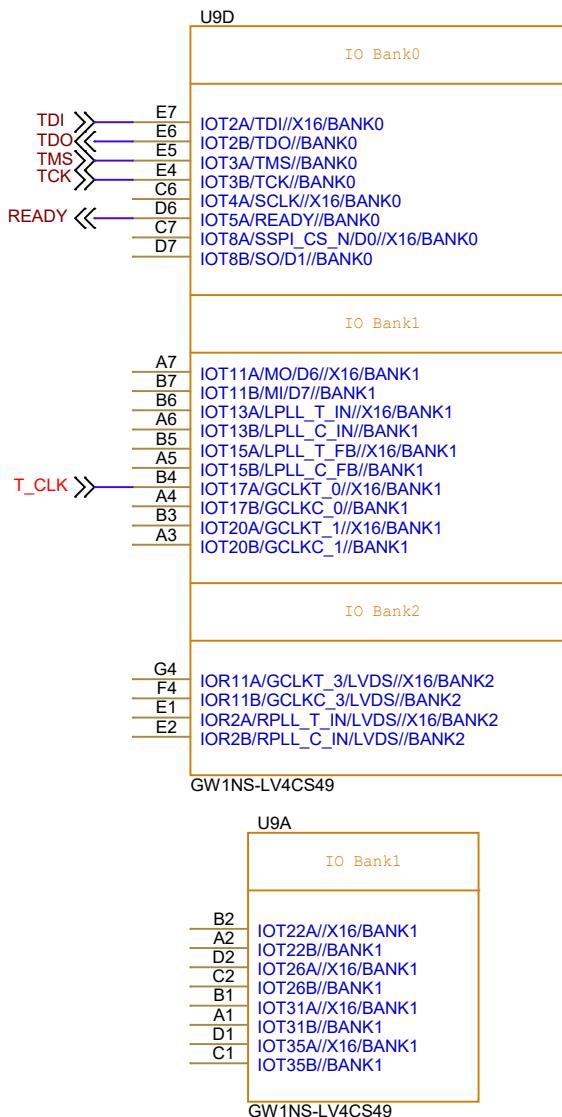
Size A4 Document Number GW1NS-LV4CQN48

Rev 2.4

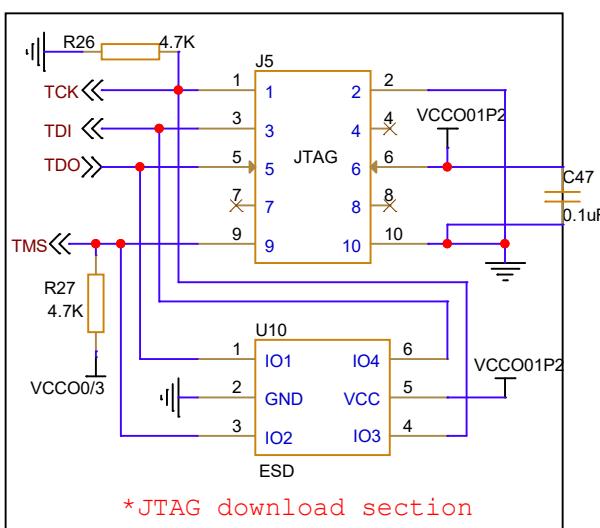
Date: Friday, March 14, 2025

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GW1NS-LV4CS49

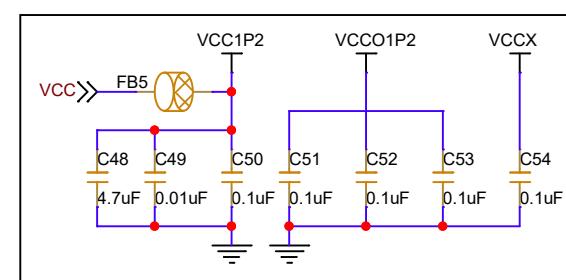


READY >> R25 4.7K VCCO1P2
***Configurable detection section**



Recommended Operating Conditions of CS49 Package in GW1NS-4/GW1NS-4C		
Name	Description	Min.
VCC	Core voltage	1.14V 1.26V
VCCIO1, VCCIO2	I/O Bank voltage When MIPI input is used in BANK1, VCCIO1 should provide 1.2V voltage. When MIPI output is used in BANK2, VCCIO2 should provide 1.2V voltage.	1.14V 3.6V
VCCIO0/VCCIO3	I/O Bank voltage, VCCIO0/VCCIO3 are internally connected. When MIPI input is used in BANK0, VCCIO0 should provide 1.2V voltage.	1.14V 3.6V
VCCX	Auxiliary voltage	1.71V 3.6V

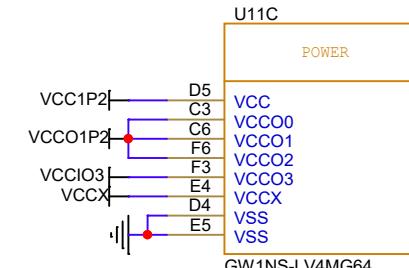
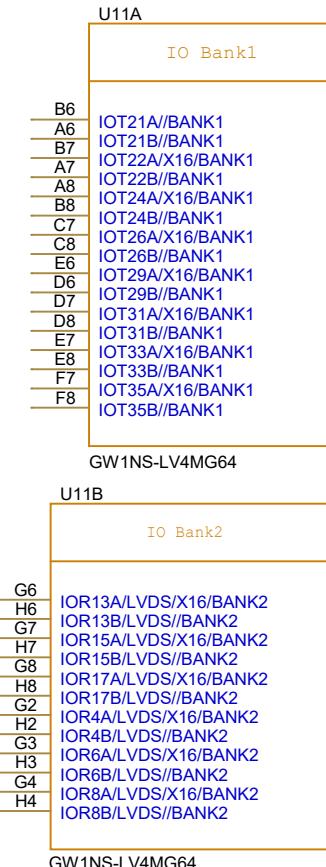
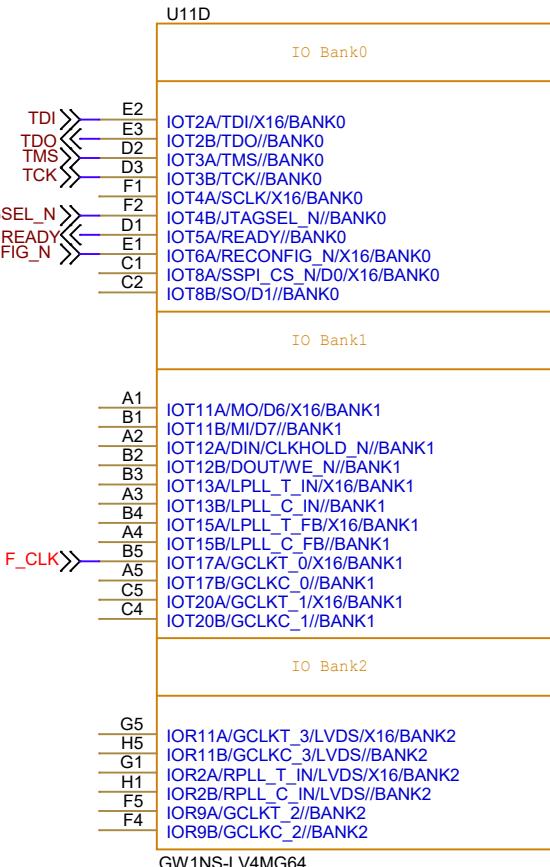
VCCX should be greater than or equal to VCCIO.



Notes:

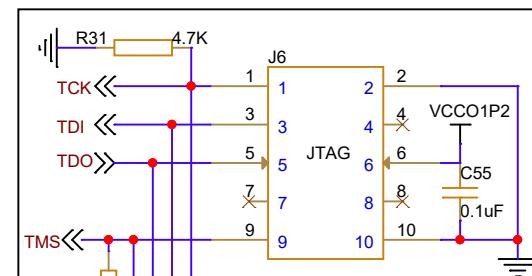
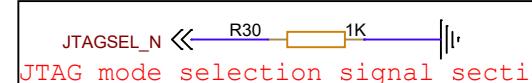
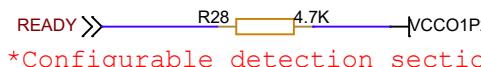
1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.
3. The CS49 package supports GW1NS-4 & GW1NS-4C.

GW1NS-LV4MG64



Recommended Operating Conditions of MG64 Package in GW1NS-4/GW1NS-4C	
Name	Description
VCC	Core voltage
VCCIO0, VCCIO1	I/O Bank voltage When MIPI input is used in BANK0 and BANK1, VCCIO0 and VCCIO1 should provide 1.2V voltage.
VCCIO2, VCCIO3	When MIPI output is used in BANK2, VCCIO2 should provide 1.2V voltage.
VCCX	Auxiliary voltage
Min.	Max.
1.14V	1.26V
1.14V	3.6V
1.71V	3.6V

VCCX should be greater than or equal to VCCIO.



Notes:

1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.
3. The MG64 package supports GW1NS-4 & GW1NS-4C.

Title	
GOWIN Minimum System Diagram	
Size A4	Document Number GW1NS-LV4MG64
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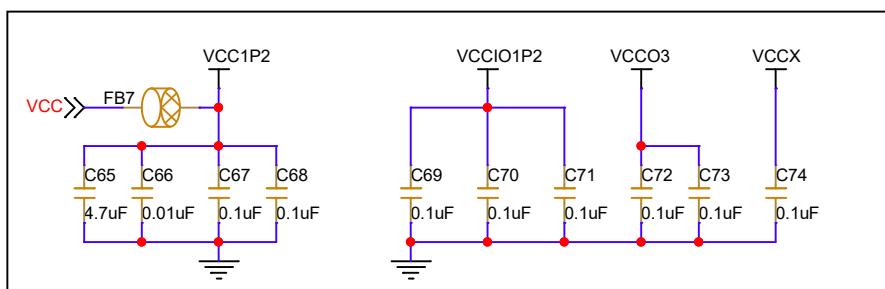
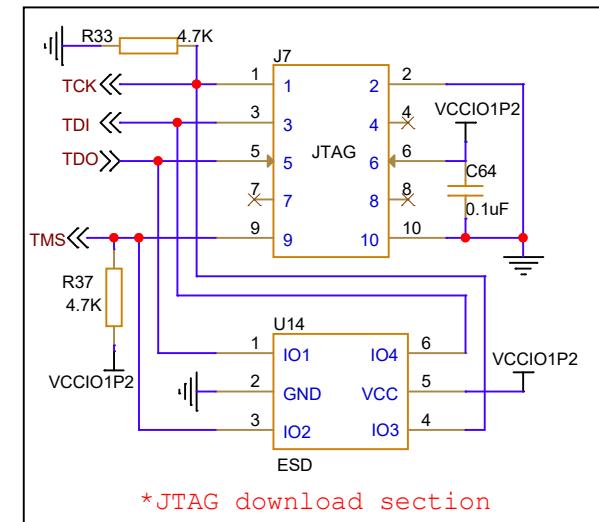
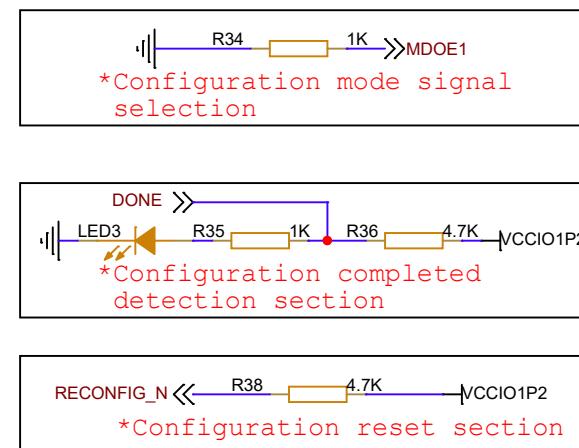
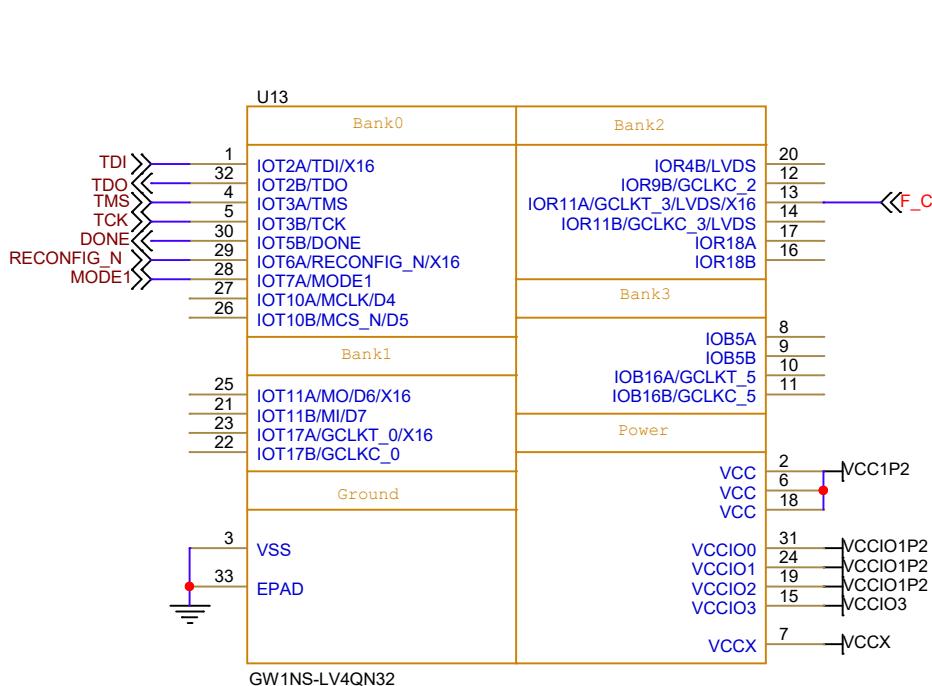
GW1NS-LV4QN32

D

C

B

A



Recommended Operating Conditions of QN32 Package in GW1NS-4

Name	Description	Min.	Max.
VCC	Core voltage	1.14V	1.26V
VCCIO0, VCCIO1, VCCIO2, VCCIO3	I/O Bank voltage When MIPI input is used in BANK0 and BANK1, VCCIO0 and VCCIO1 should provide 1.2V voltage. When MIPI output is used in BANK2, VCCIO2 should provide 1.2V voltage.	1.14V	3.6V
VCCX	Auxiliary voltage	1.71V	3.6V
Note !			
It is highly recommended that the EPAD connect to GND, but not a requirement.			

VCCX should be greater than or equal to VCCIO.

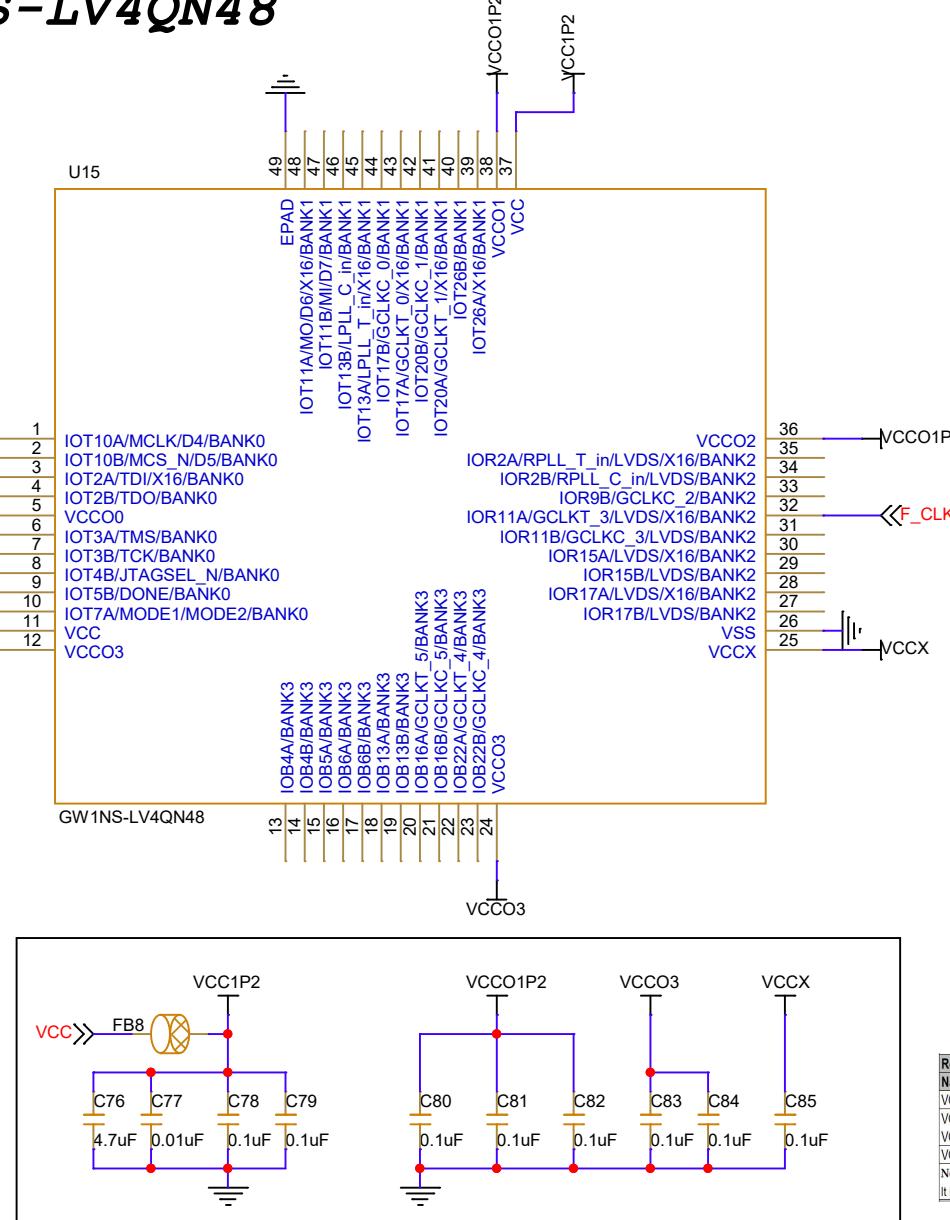
Notes:

1. F_CLK signal is an external input clock signal.

It is recommended that F_CLK signal be provided through an active oscillator crystal.

2. It is recommended that add an ESD protection chip to the JTAG download circuit.

GW1NS-LV4QN48



*Configuration mode signal selection

The diagram illustrates the connection of the JTAG interface to the U16 chip. The JTAG pins (TCK, TDI, TDO, TMS) are connected through resistors R43 and R44 to the U16 chip. The U16 chip is connected to VCCO1P2 and GND. A feedback path from U16 pin 10 is shown with a capacitor C75 and a 0.1uF bypass capacitor.

Recommended Operating Conditions of QN48 Package in GW1NS-4/GW1NS-4C		
Name	Description	Min.
VCC	Core voltage	1.14V
VCCIO0, VCCIO1, VCCIO2, VCCIO3	I/O Bank voltage When MIPI input is used in BANK0 and BANK1, VCCIO0 and VCCIO1 should provide 1.2V voltage. When MIPI output is used in BANK2, VCCIO2 should provide 1.2V voltage.	1.14V 3.6V
VCCX	Auxiliary voltage	1.71V
Note !	It is highly recommended that the EPAD connect to GND, but not a requirement.	

VCCX should be greater than or equal to VCCIO.

Notes:

- 1.F_CLK signal is an external input clock signal.
A It is recommended that F_CLK signal be provided through an active oscillator crystal
2.It is recommended that add an ESD protection chip to the JTAG download circuit.
3.The ON48 package supports GW1NS-4 & GW1NS-4C.