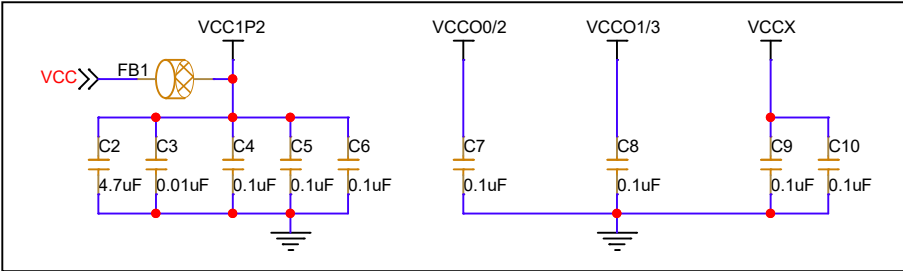
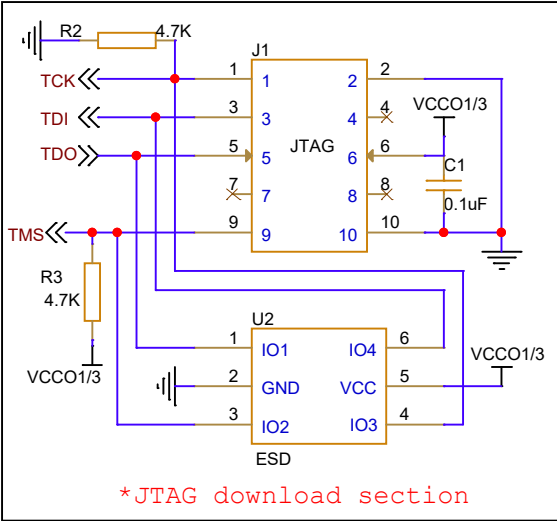
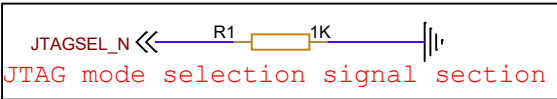
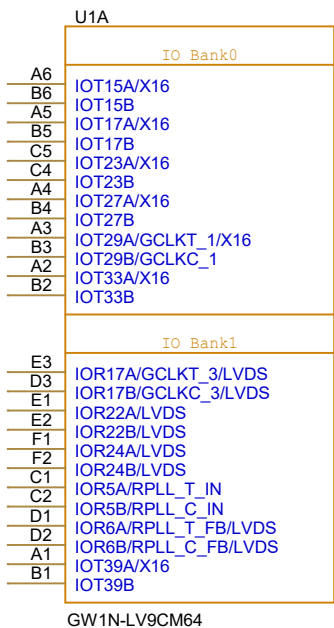
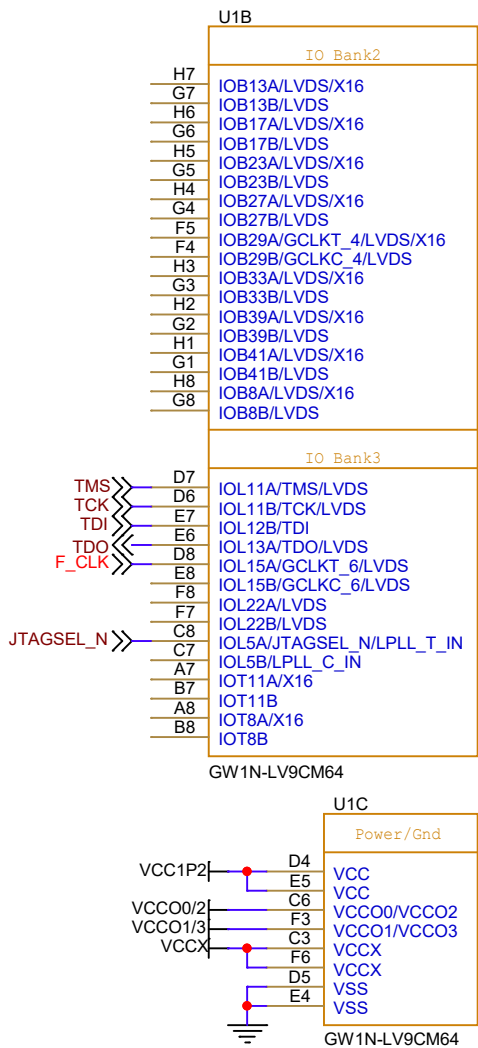


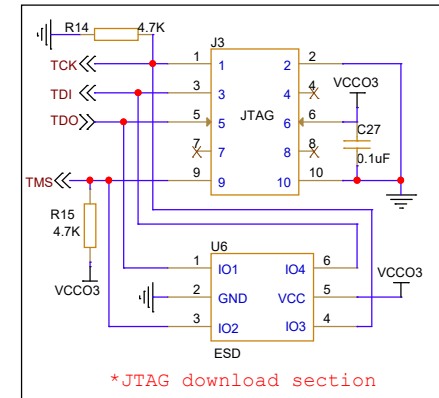
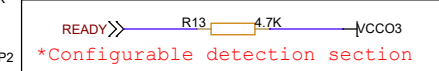
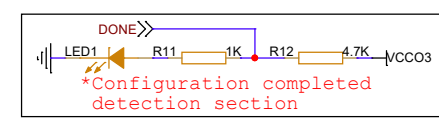
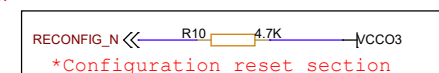
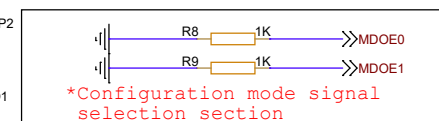
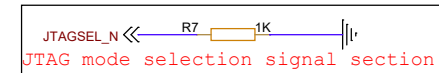
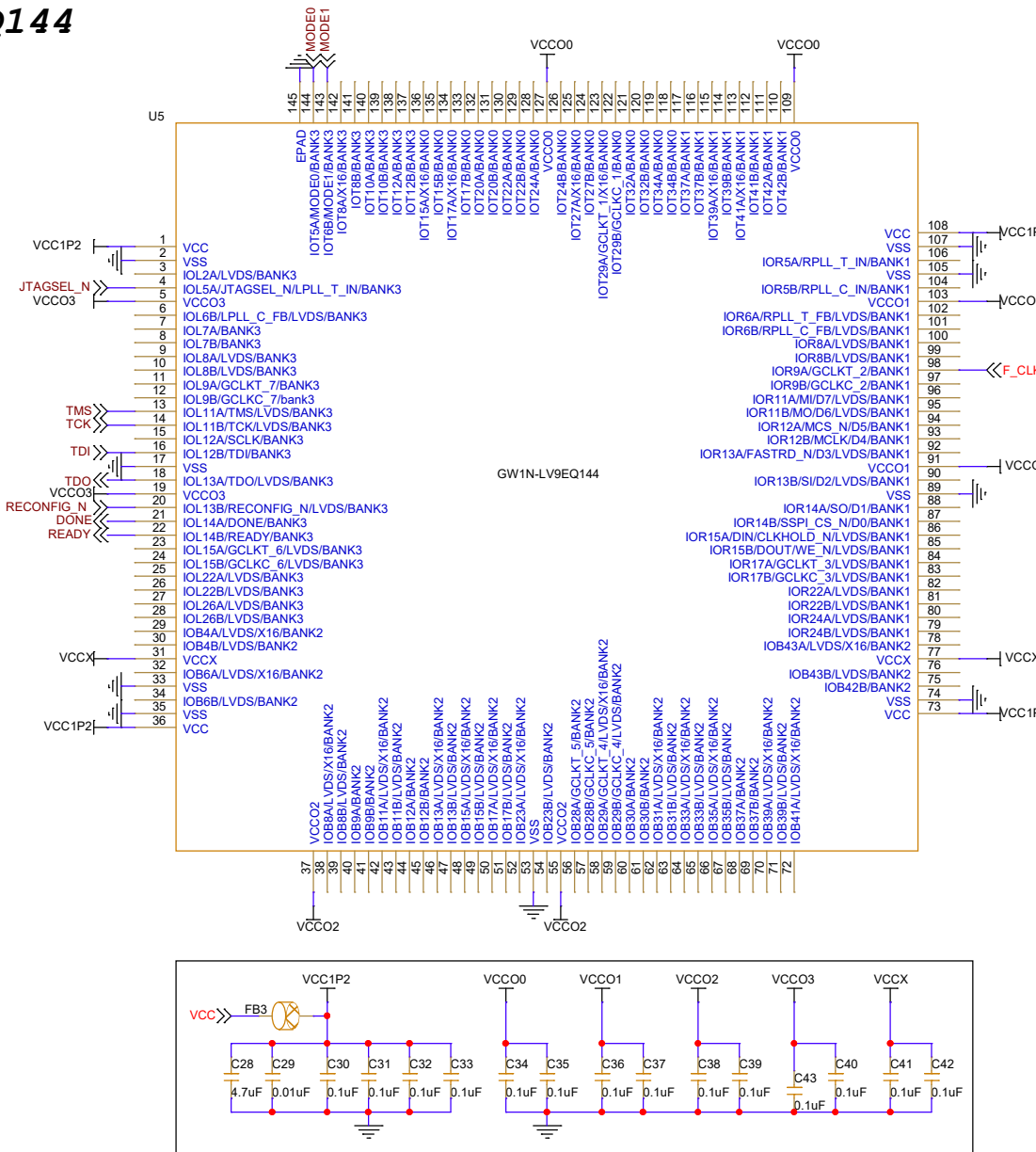
GW1N-LV9CM64



Notes:

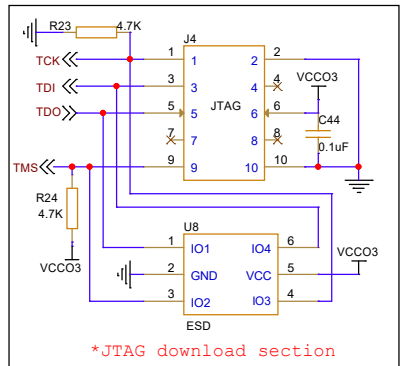
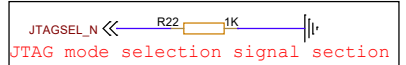
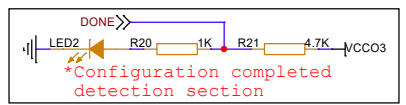
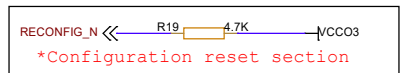
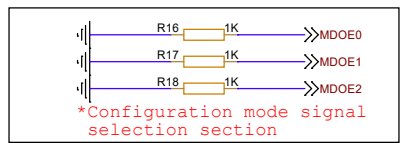
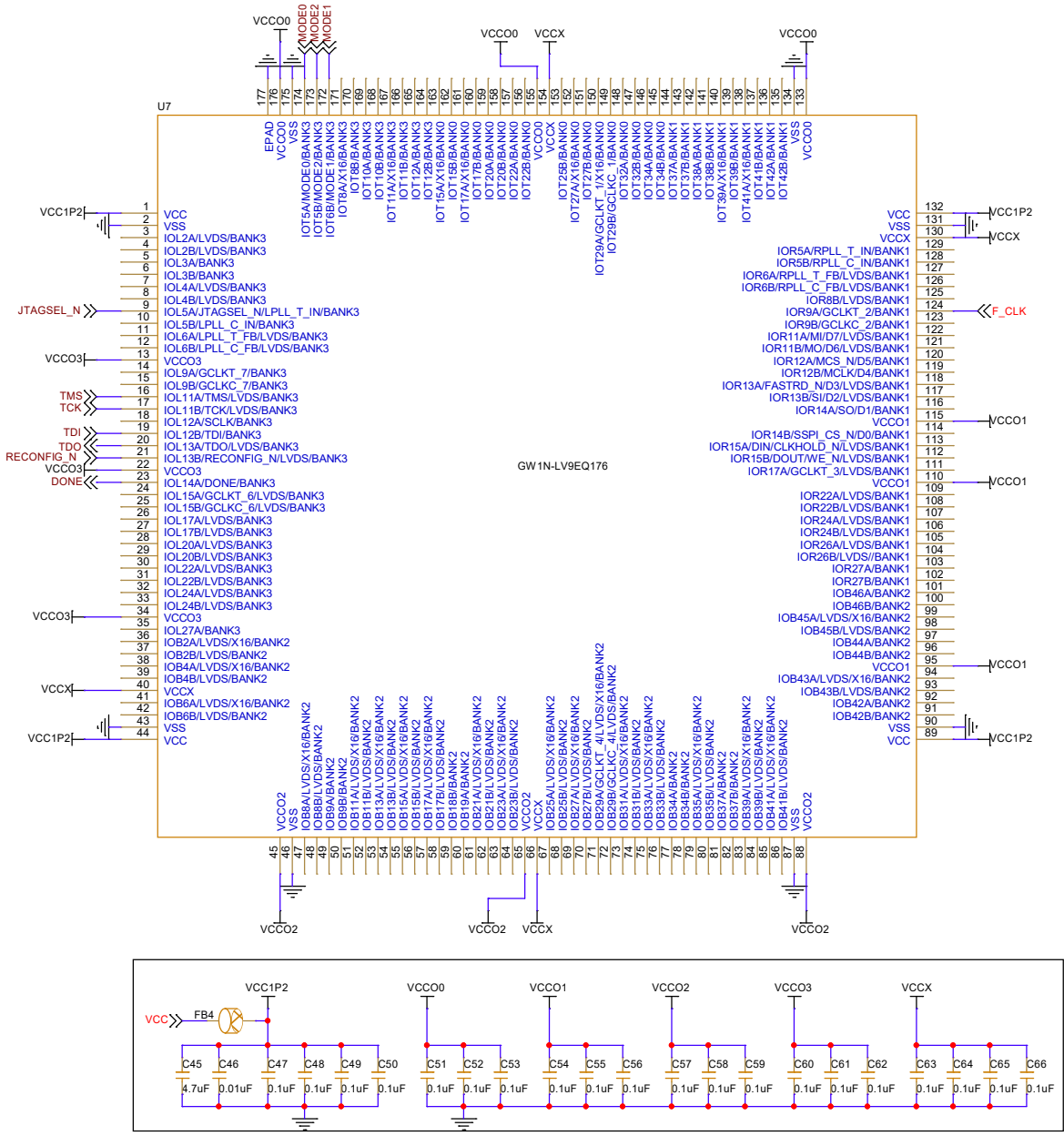
1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.

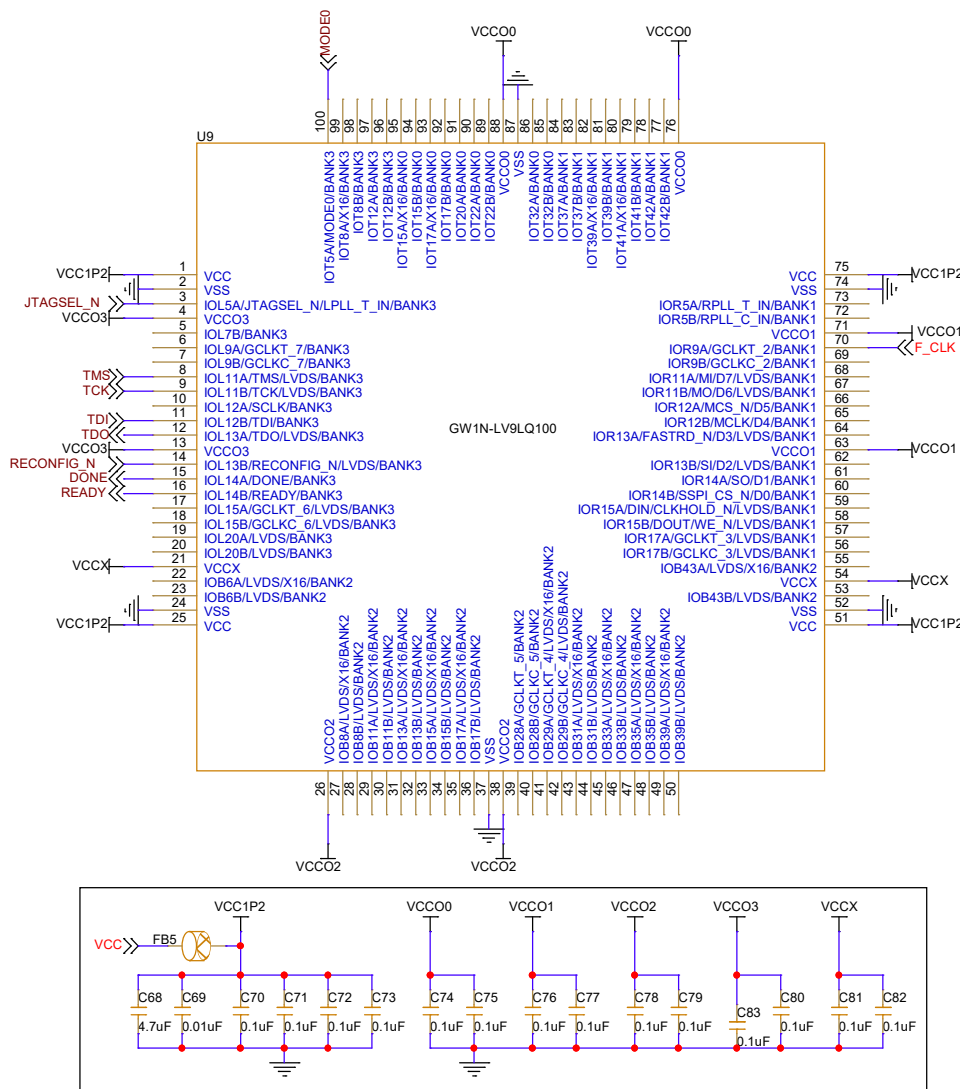


Notes:
1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

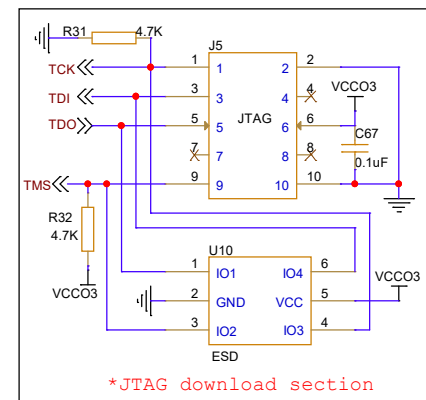
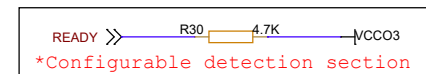
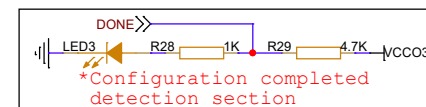
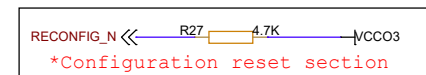
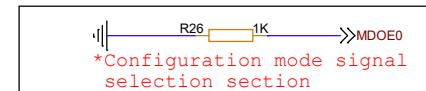
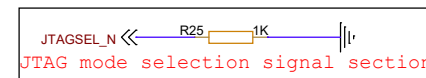
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GOWIN Minimum System Diagram		
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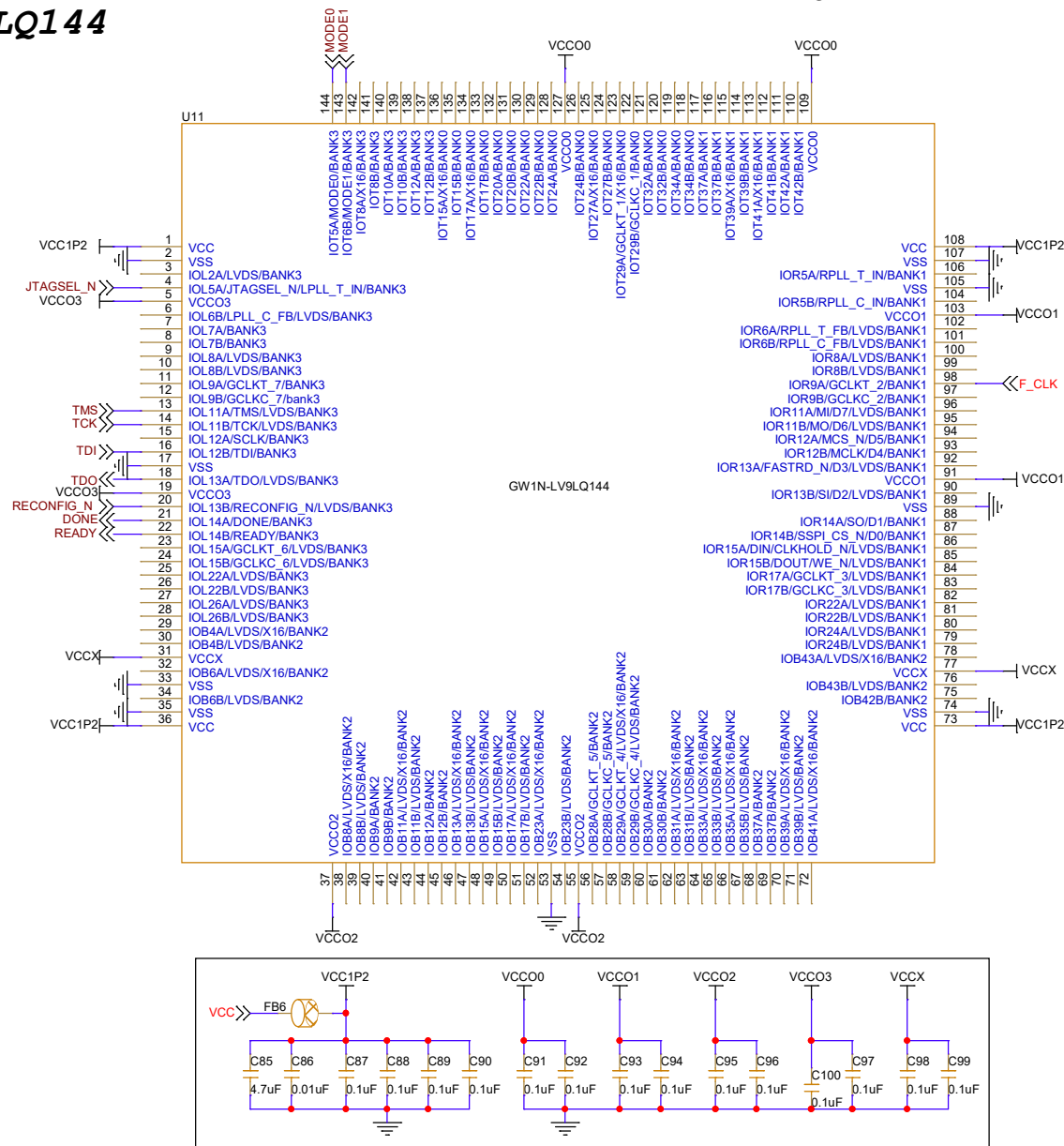
Notes:
1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.It is recommended that add an ESD protection circuit to the JTAG download circuit.



- Notes:
- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

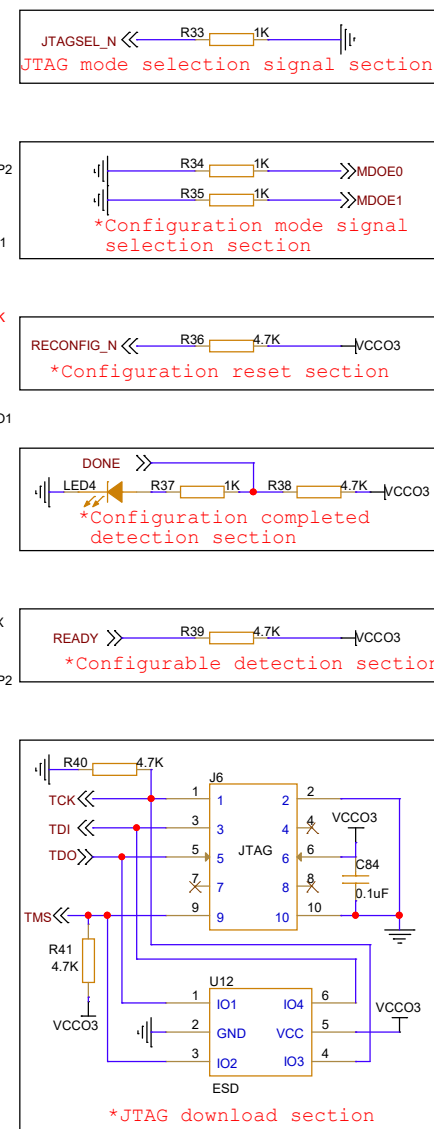


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GOWIN Minimum System Diagram		
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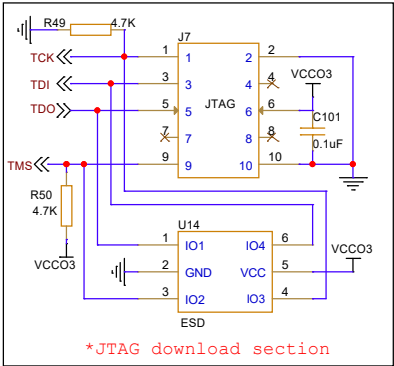
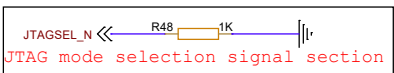
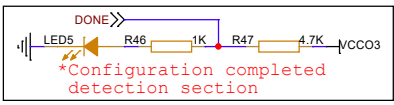
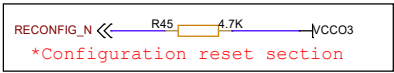
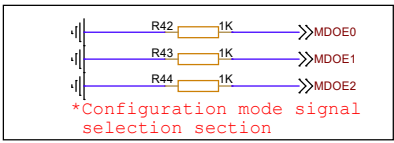
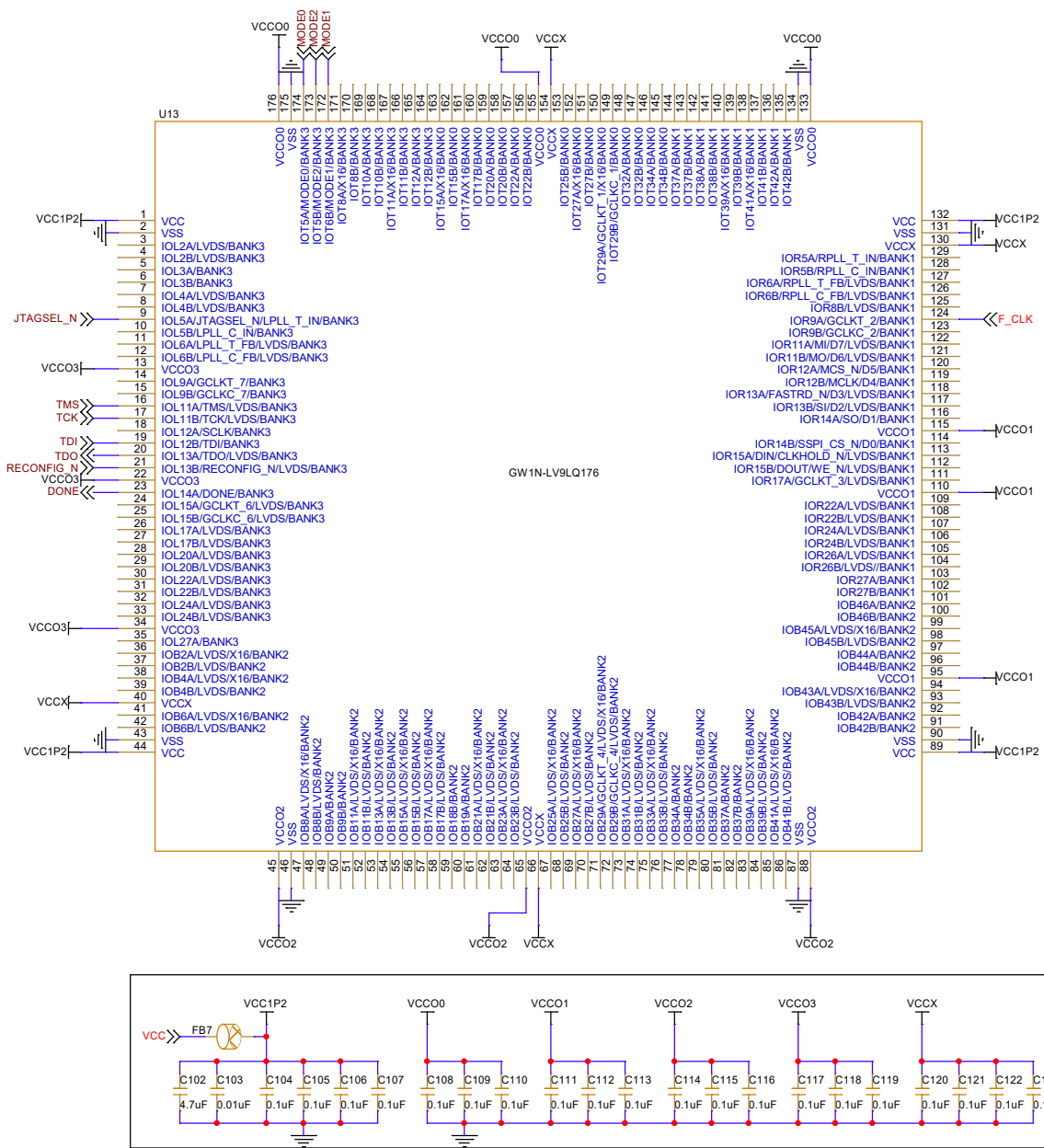


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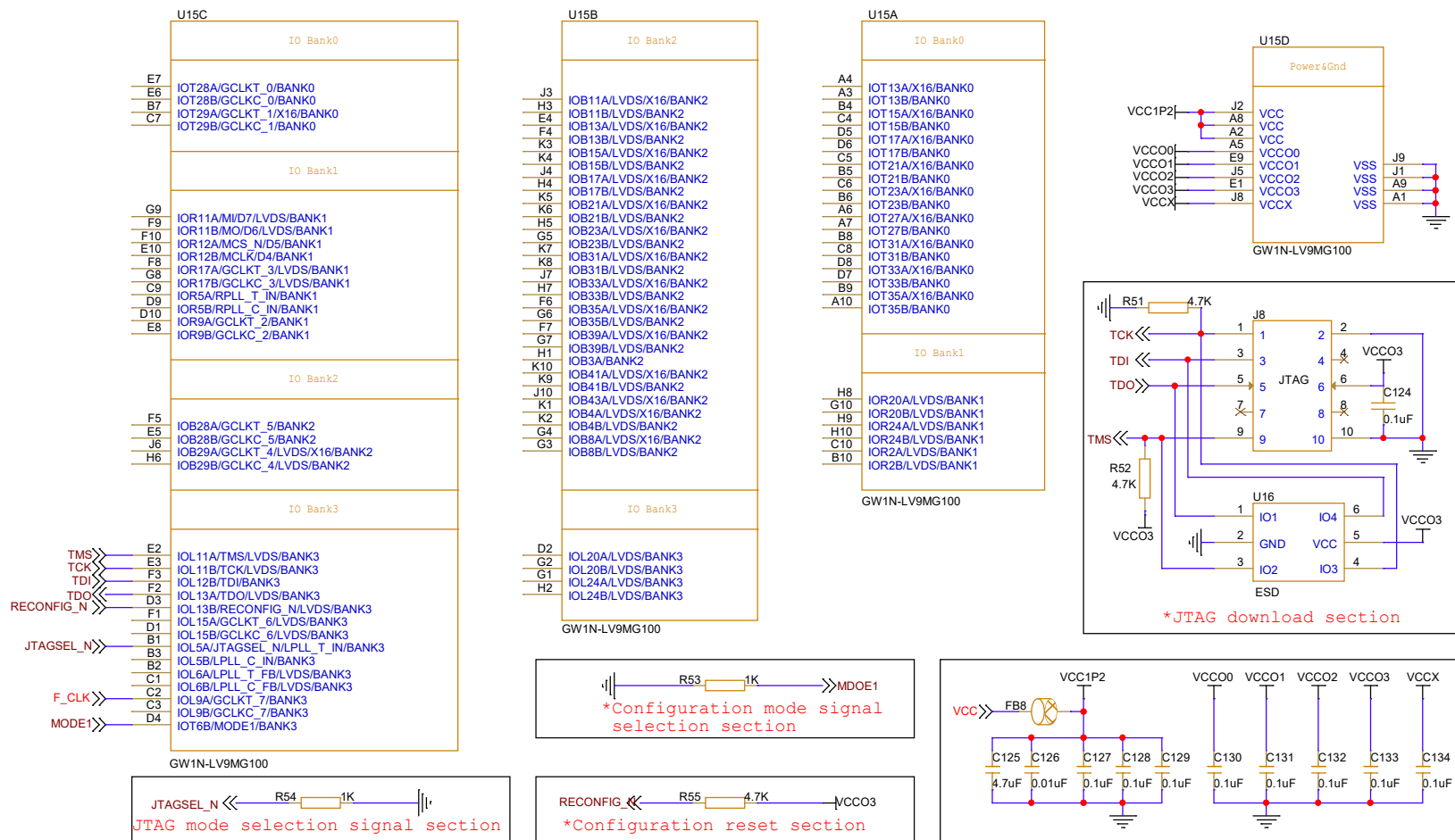
- NOTES:
- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



Title				
GOWIN Minimum System Diagram				
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Notes:
1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

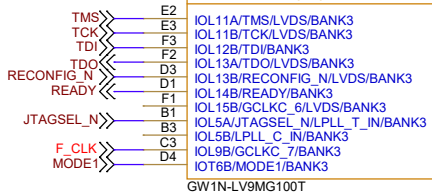
**Notes:**

1.F_CLK signal is an external input clock signal.

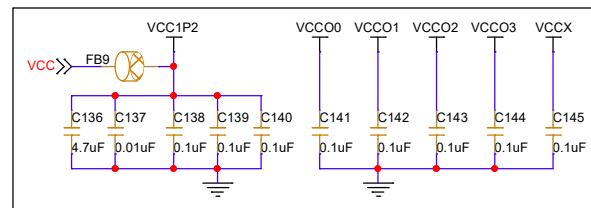
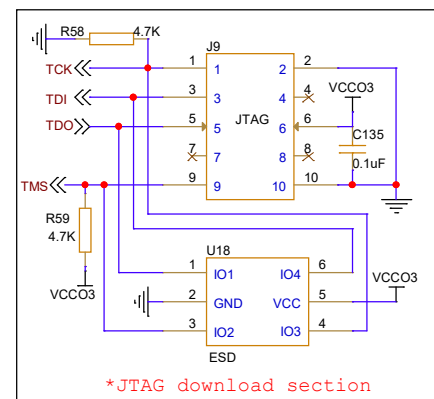
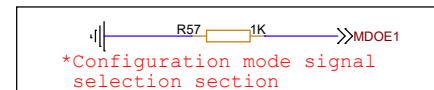
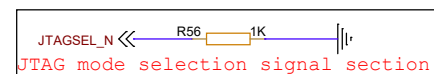
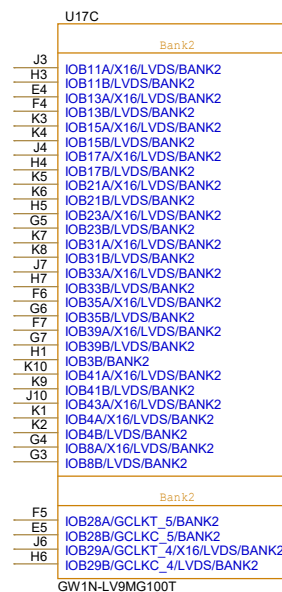
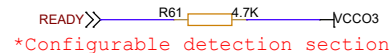
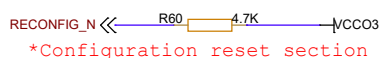
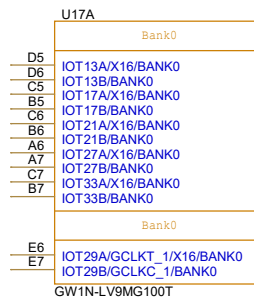
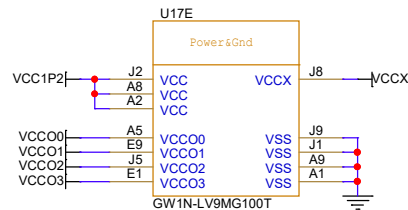
It is recommended that F_CLK signal be provided through an active oscillator crystal.

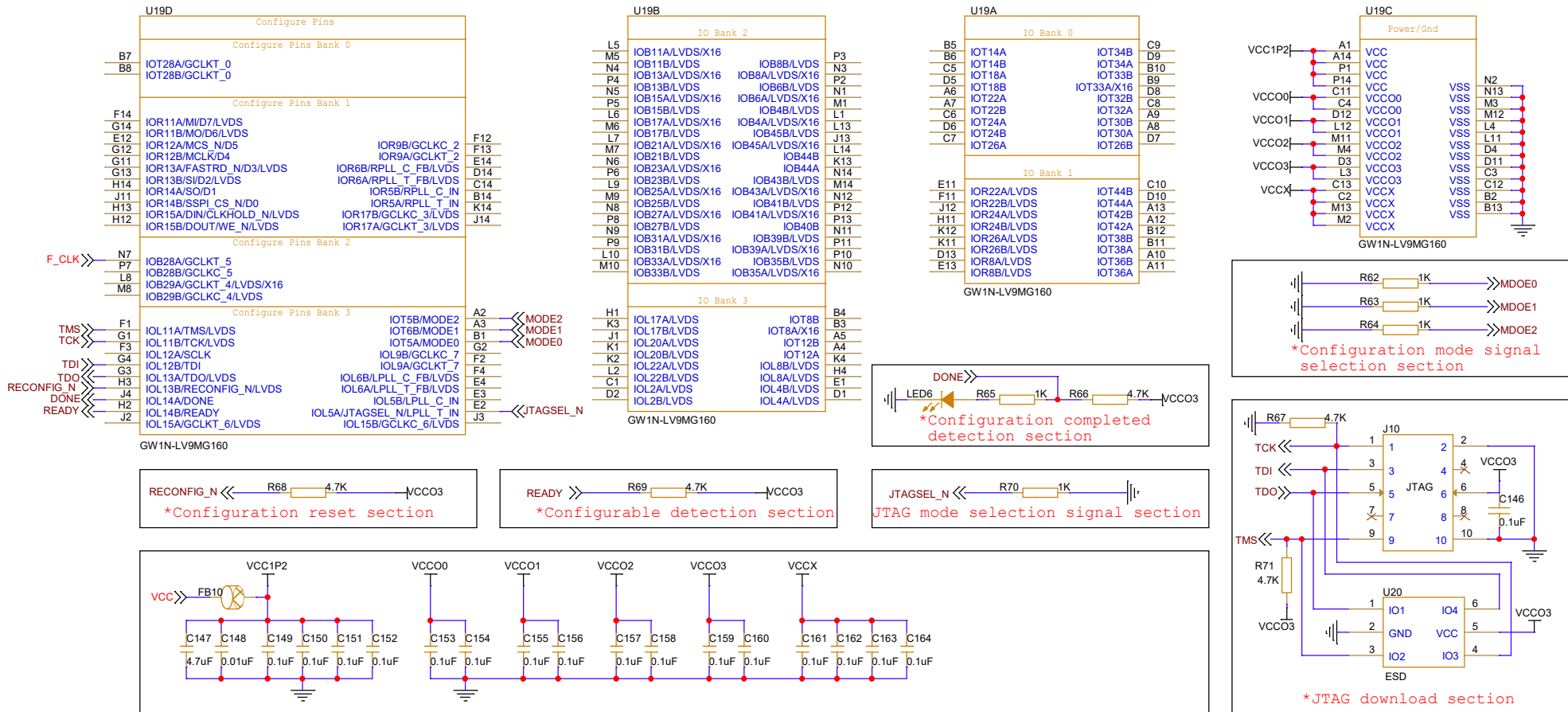
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

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GOWIN Minimum System Diagram		
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B	GW1N-LV9MG100	2.3
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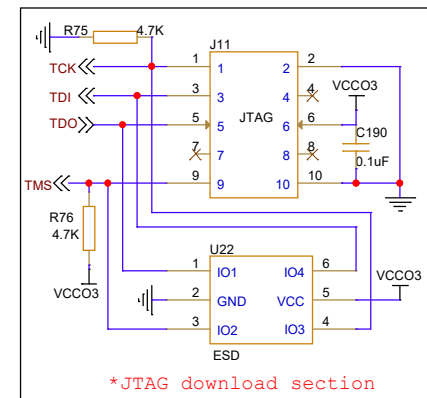
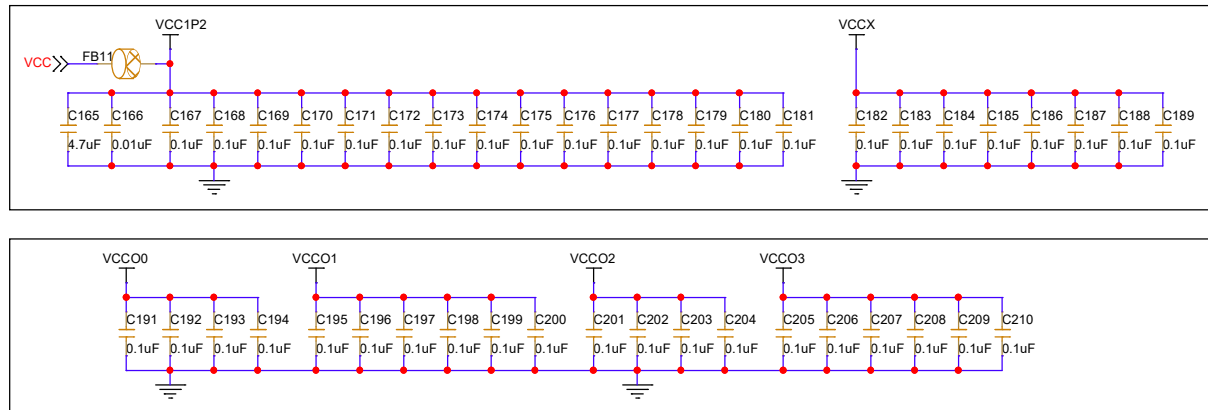
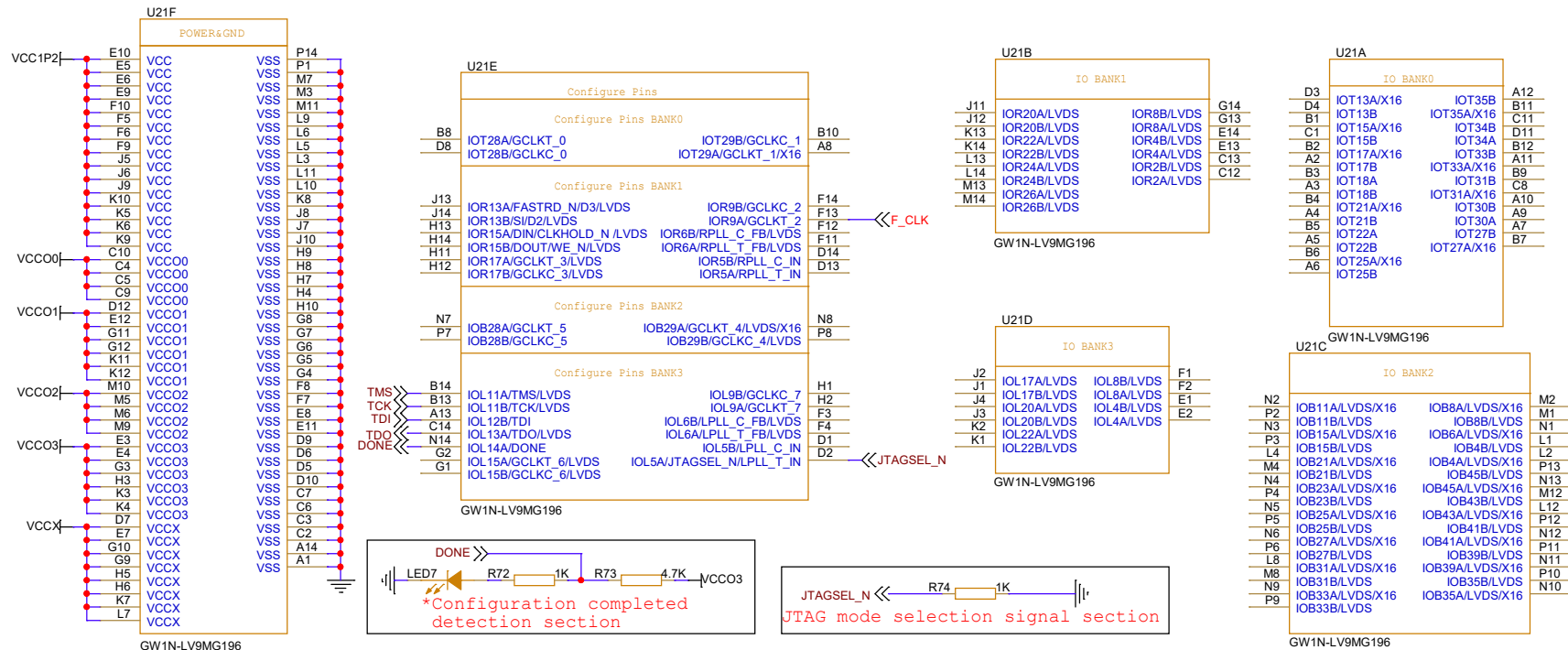


2. It is recommended that add an ESD protection chip to the JTAG download circuit.





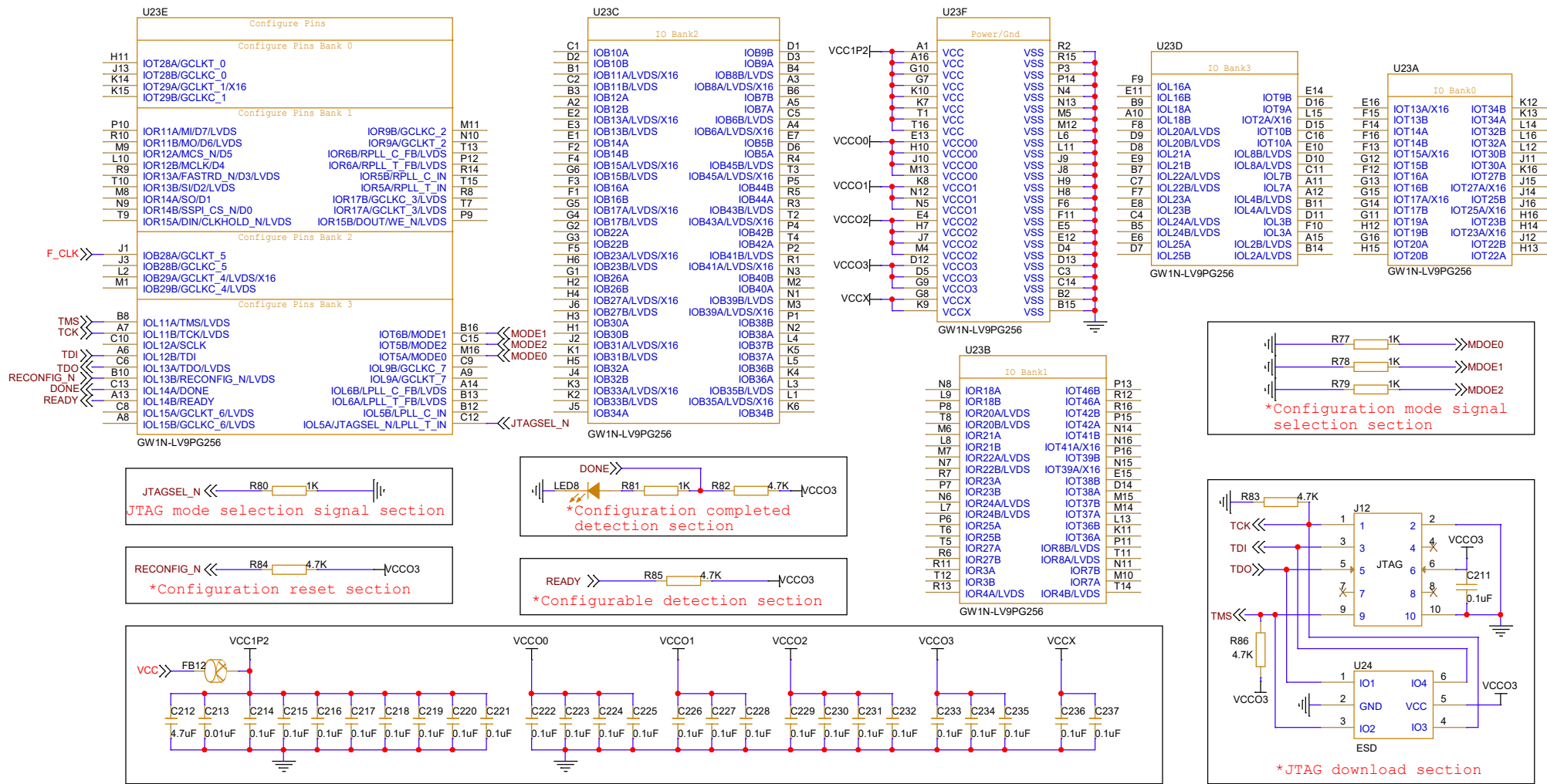
Notes:
1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
2.It is recommended that add an ESD protection chip to the JTAG download circuit.



Notes:

- 1.F CLK signal is an external input clock signal. It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
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B	GW1N-LV9MG196	2.3
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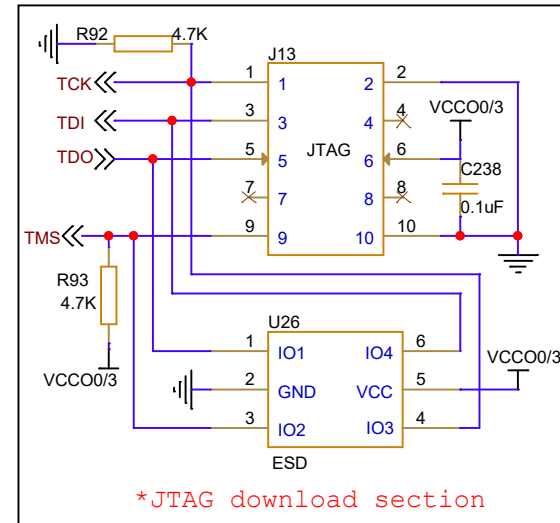
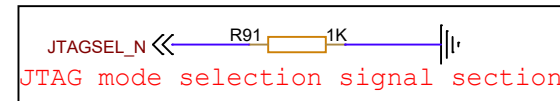
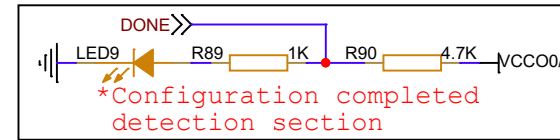
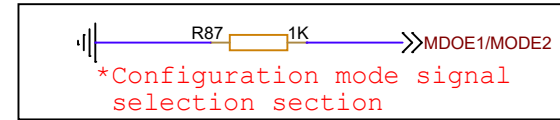
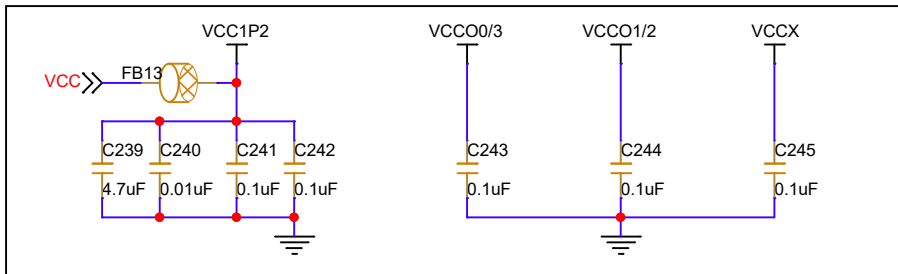
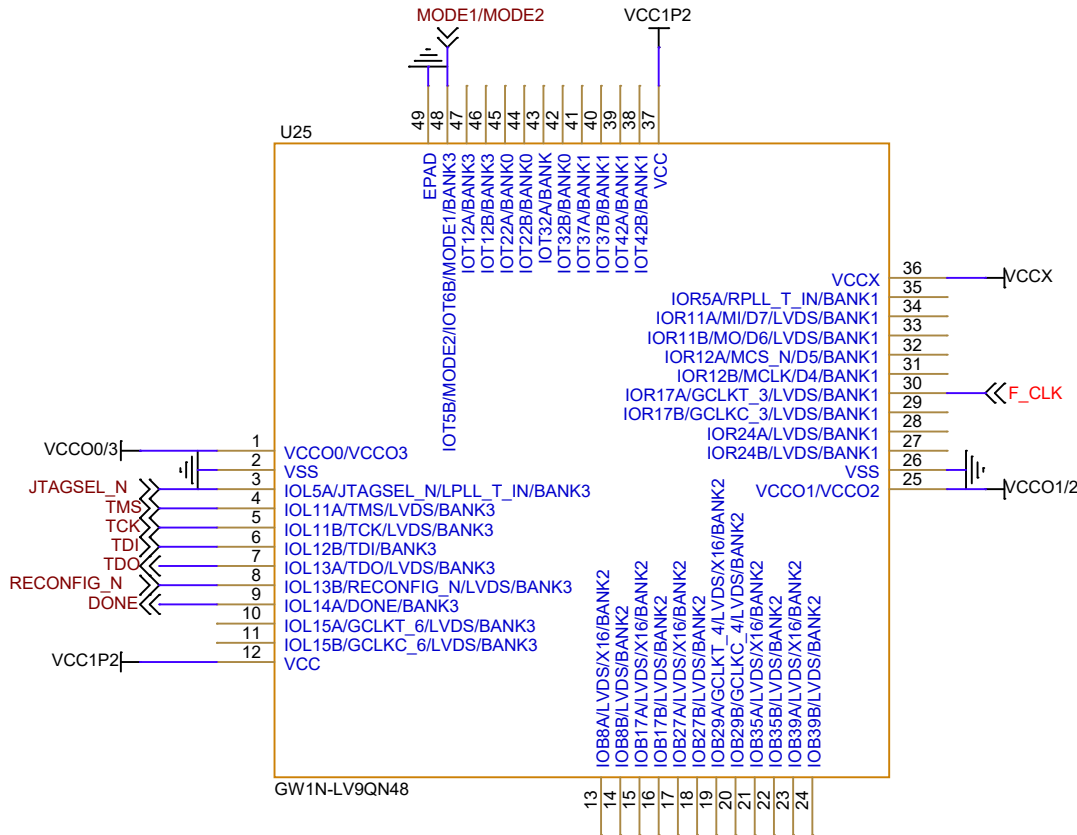


Notes:

- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

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GOWIN Minimum System Diagram		
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B	GW1N-LV9PG256	2.3
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GW1N-LV9QN48



Notes:

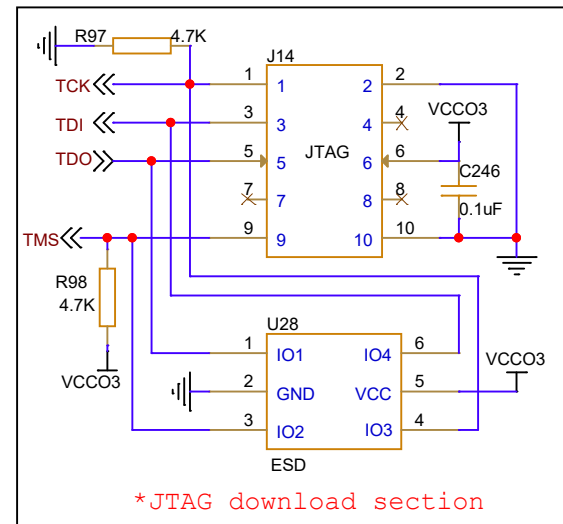
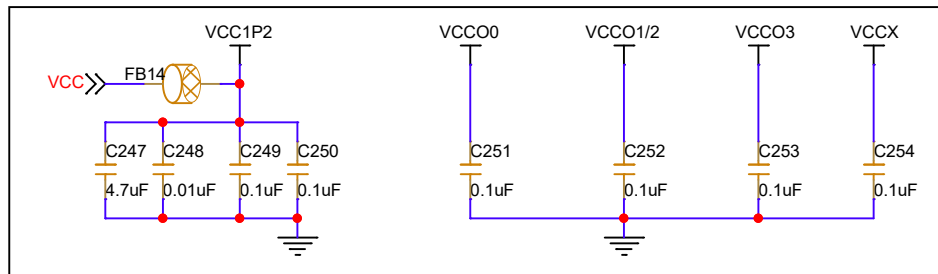
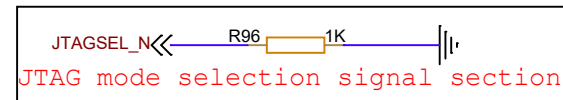
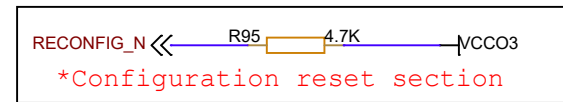
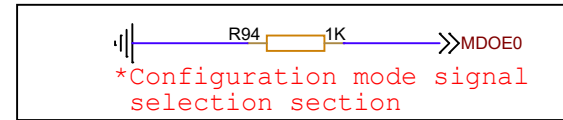
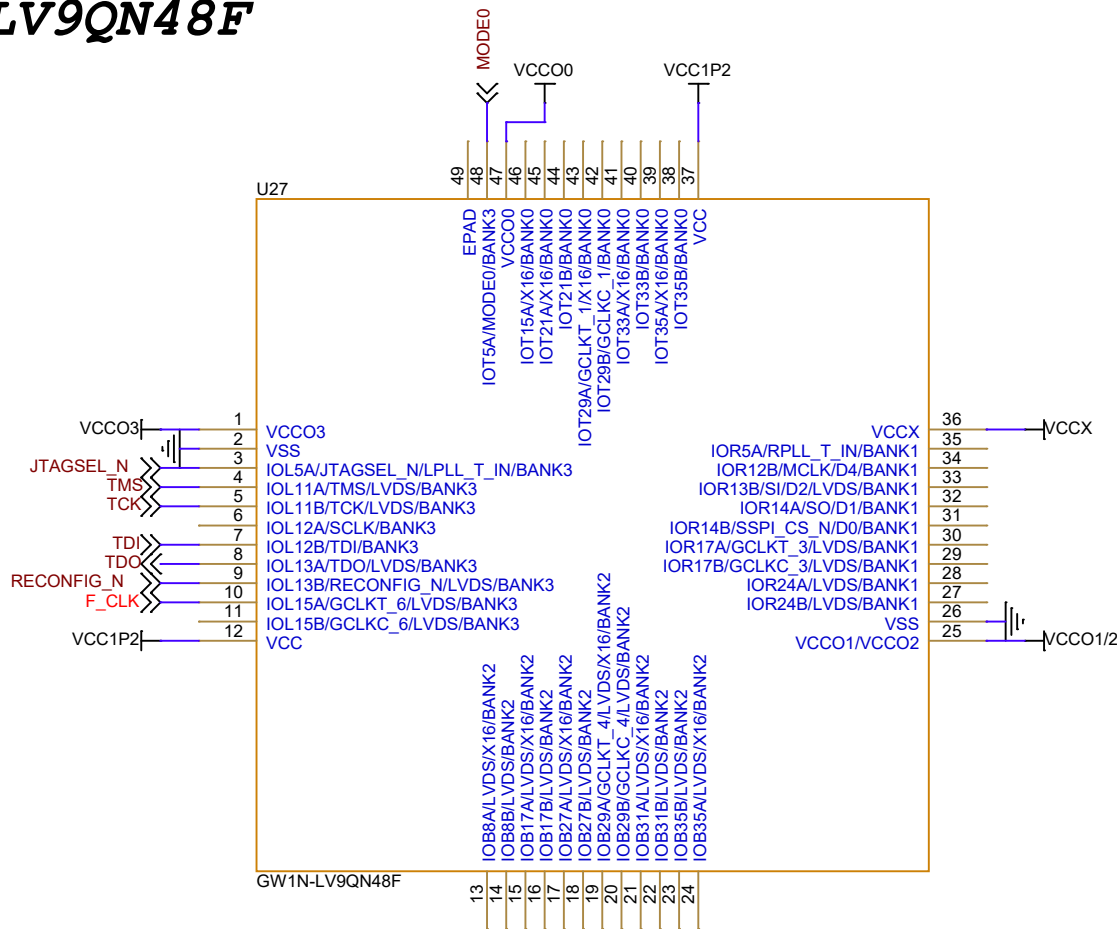
1.F_CLK signal is an external input clock signal.

It is recommended that F_CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
A4	GW1N-LV9QN48	2.3
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GW1N-LV9QN48F



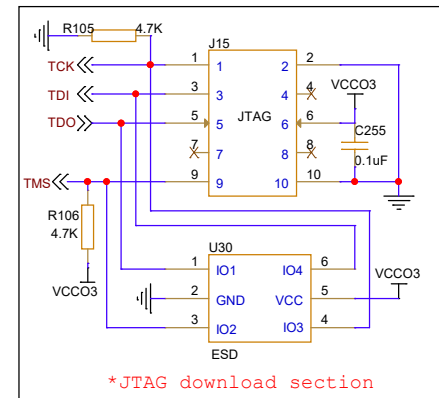
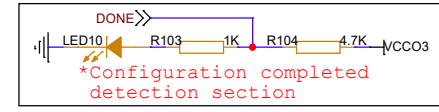
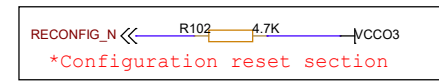
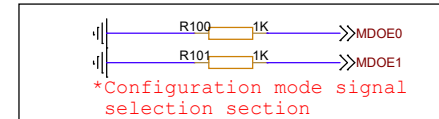
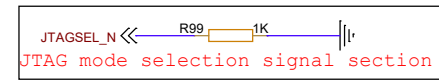
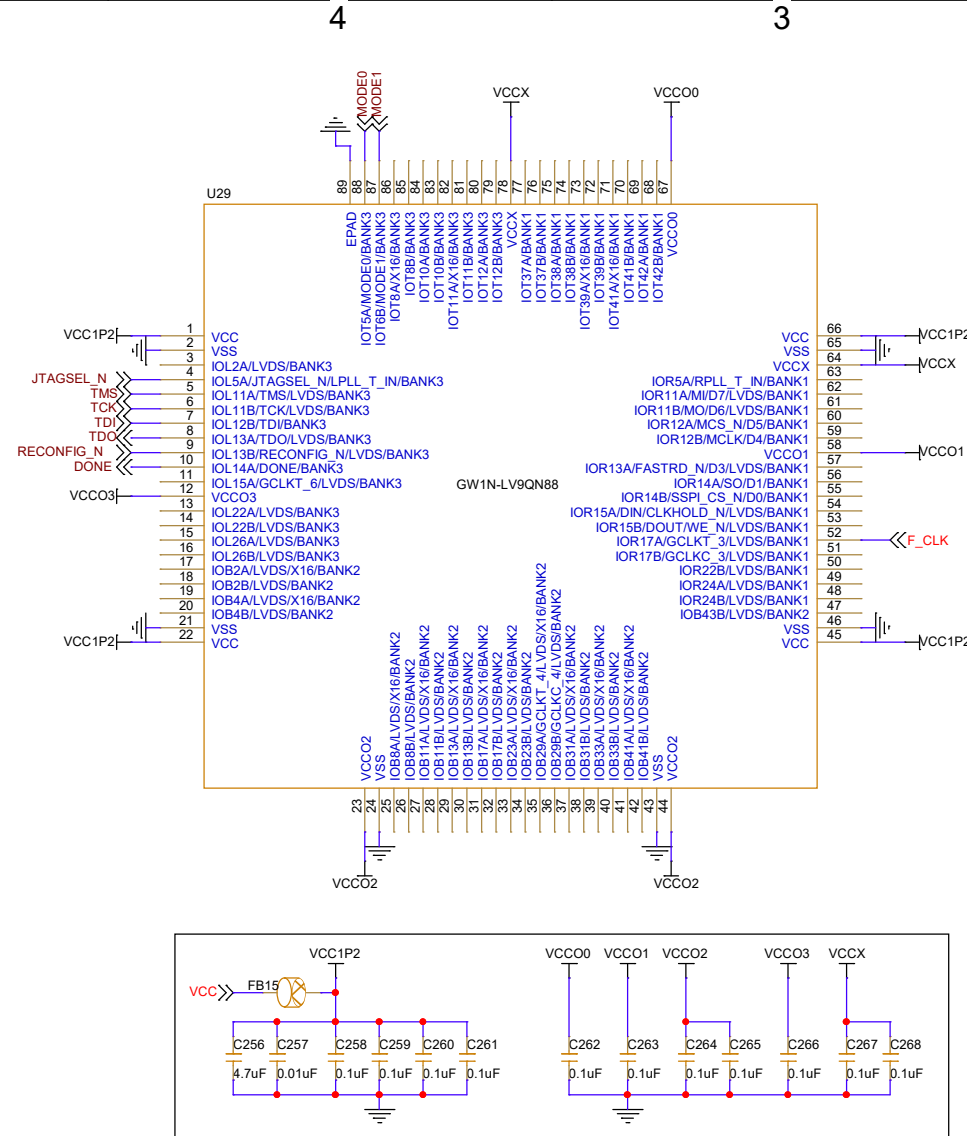
Notes:

1.F CLK signal is an external input clock signal.

It is recommended that F CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
A4	GW1N-LV9QN48F	2.3
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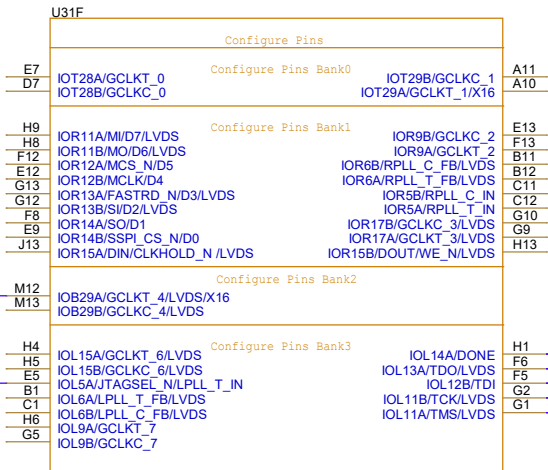


Notes:
1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

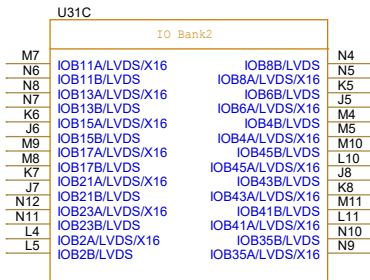
Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-LV9QN88	2.3
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F_CLK

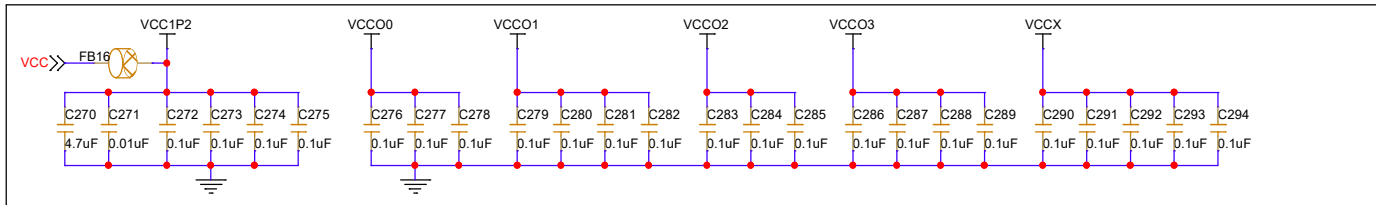
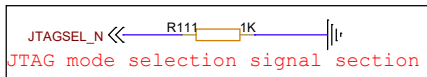
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GW1N-LV9UG169

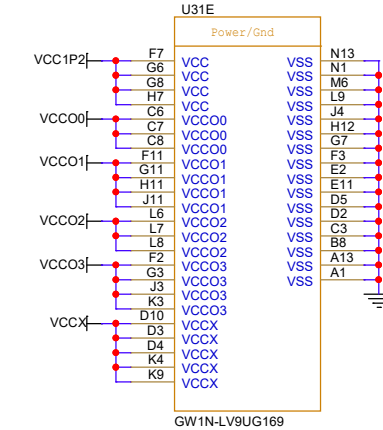
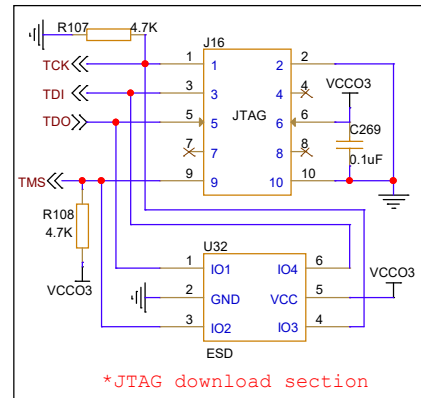
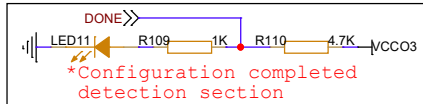


GW1N-LV9UG169

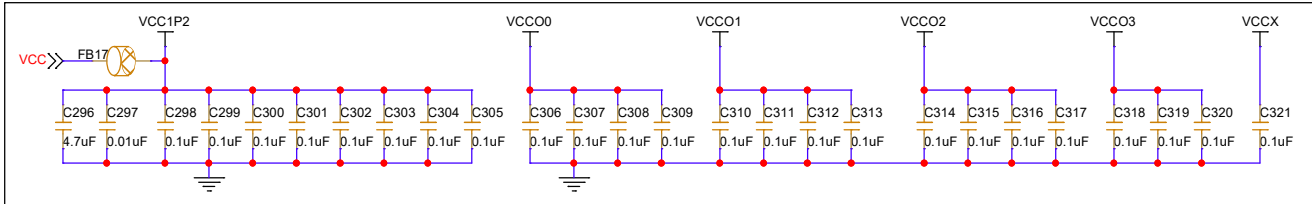
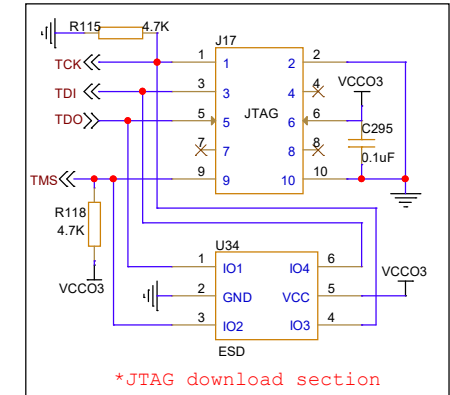
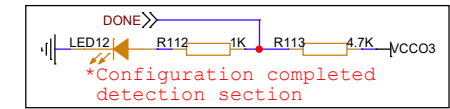
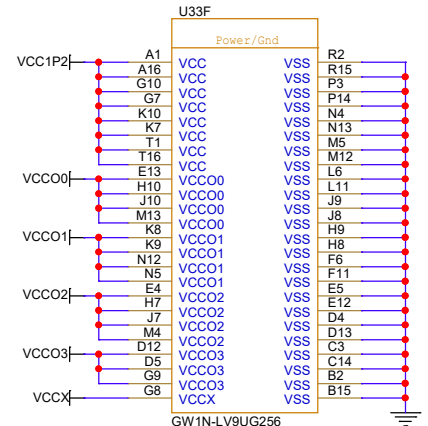
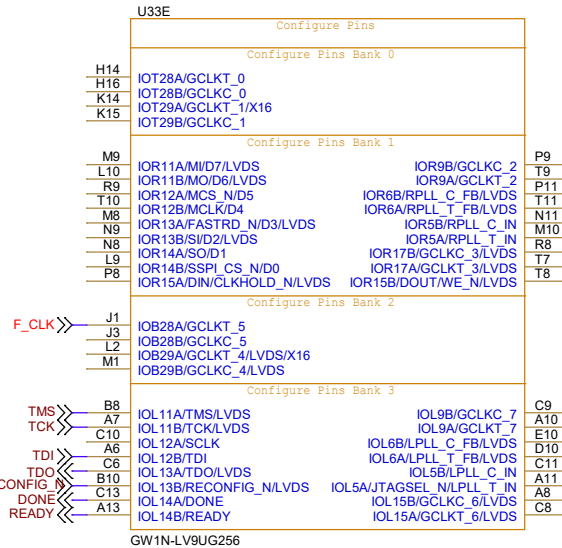
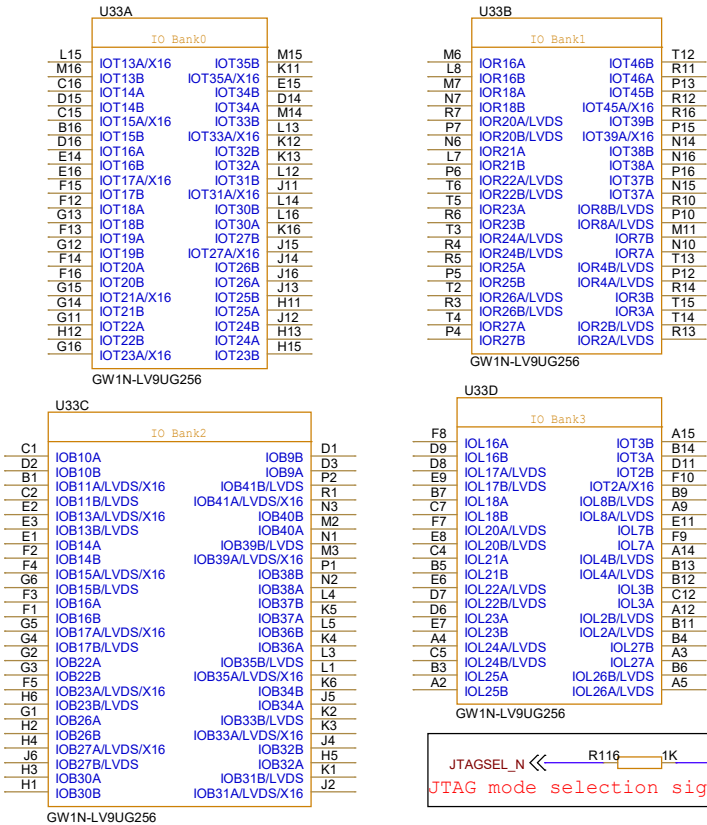


Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



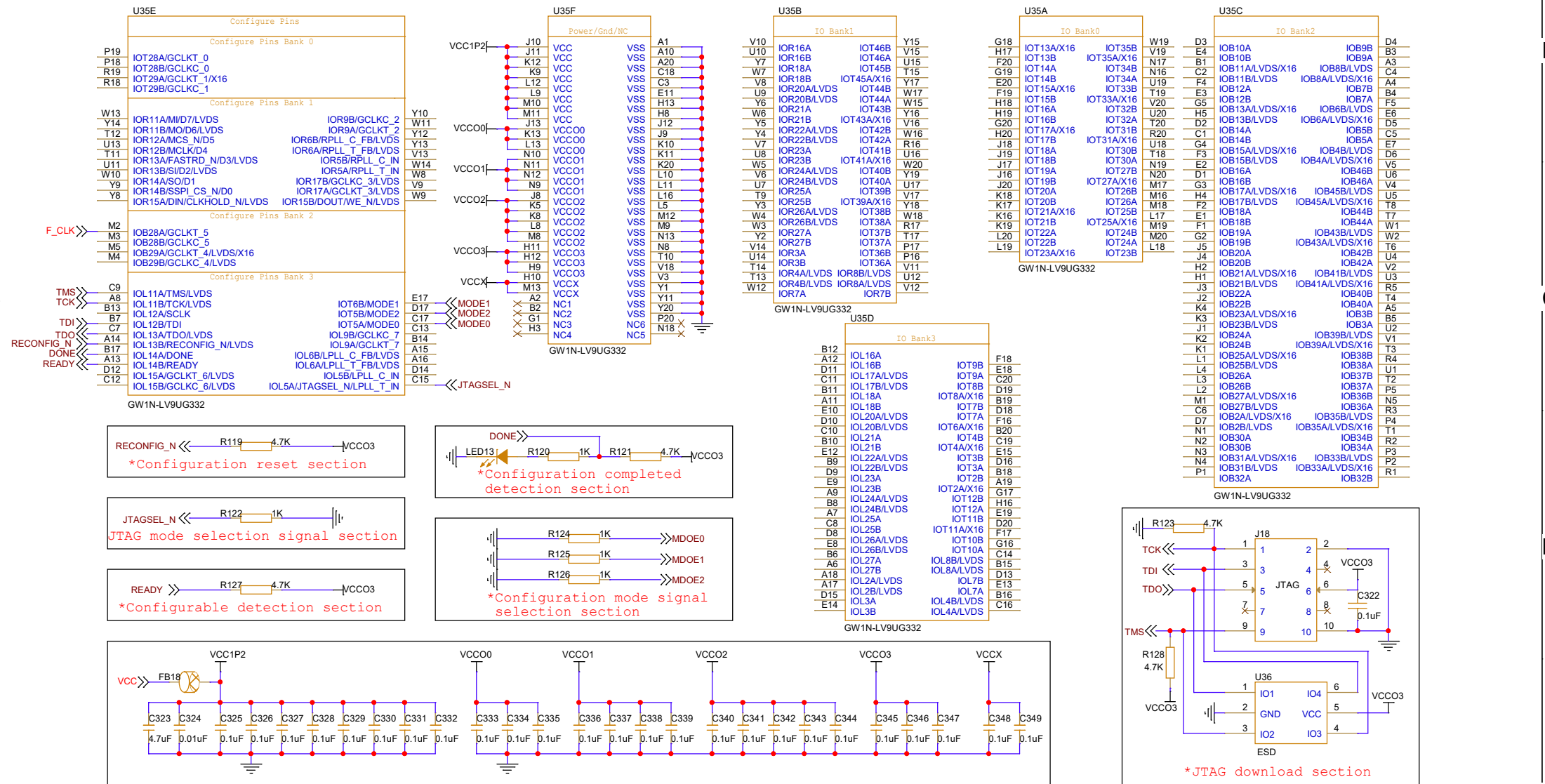
Title		
GOWIN Minimum System Diagram		
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B	GW1N-LV9UG169	2.3
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Notes:

- 1.F CLK signal is an external input clock signal. It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
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B	GW1N-LV9UG256	2.3
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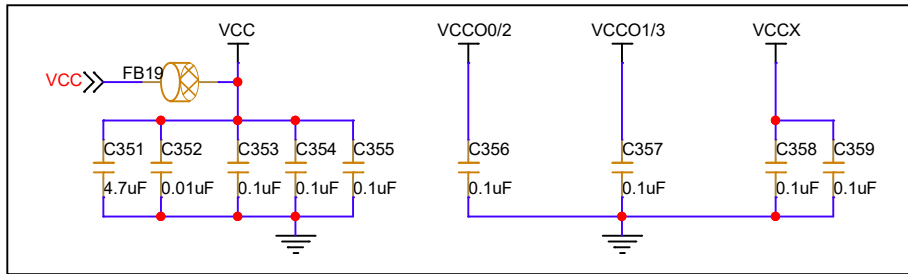
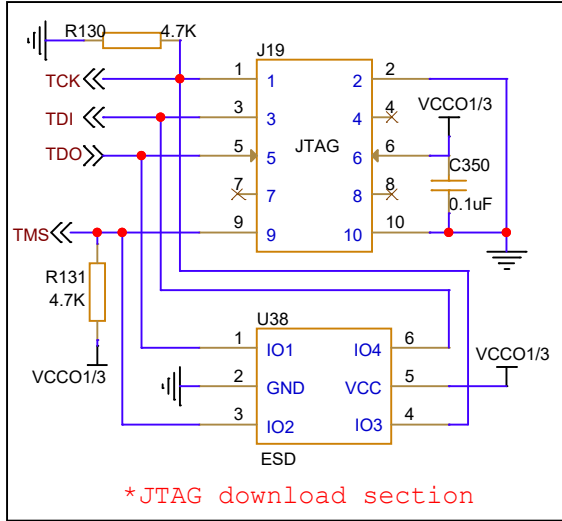
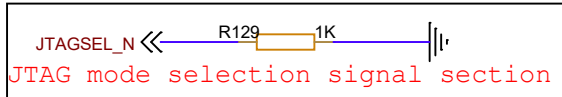
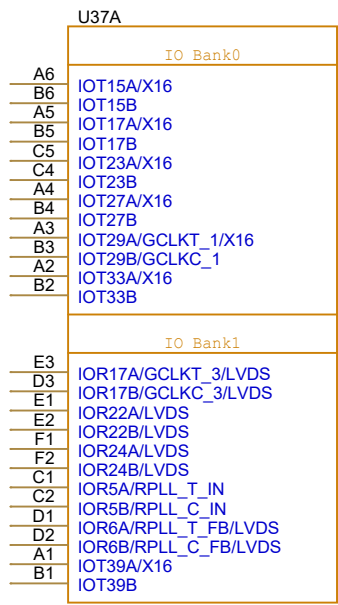
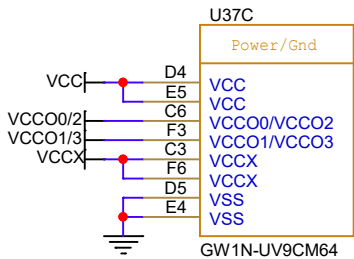
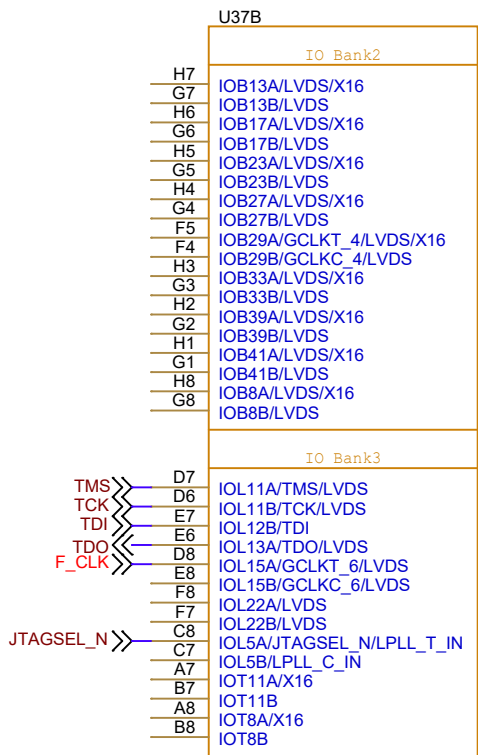


Notes:

- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
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B	GW1N-LV9UG332	2.3
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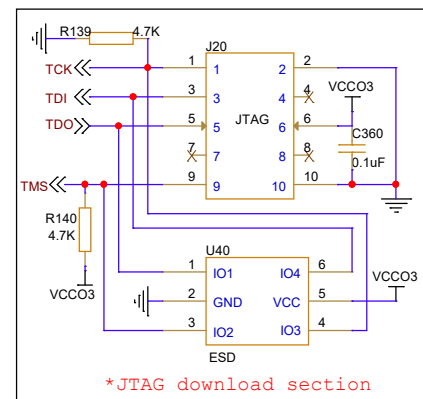
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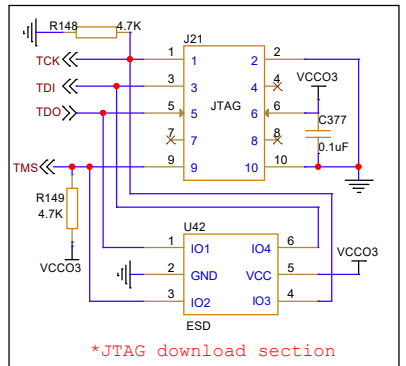
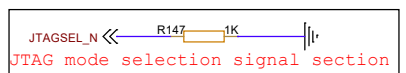
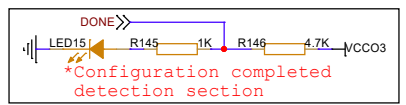
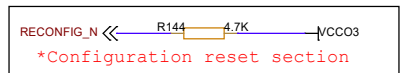
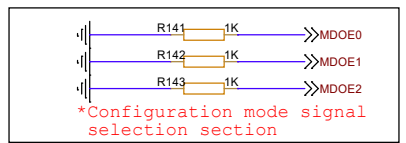
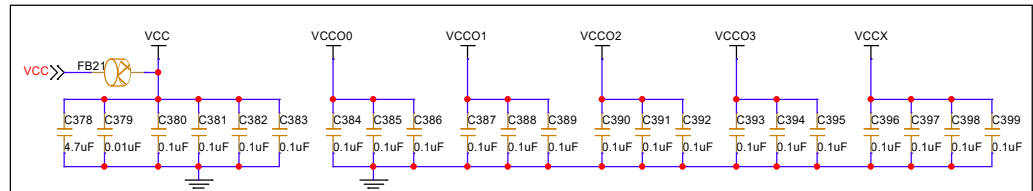
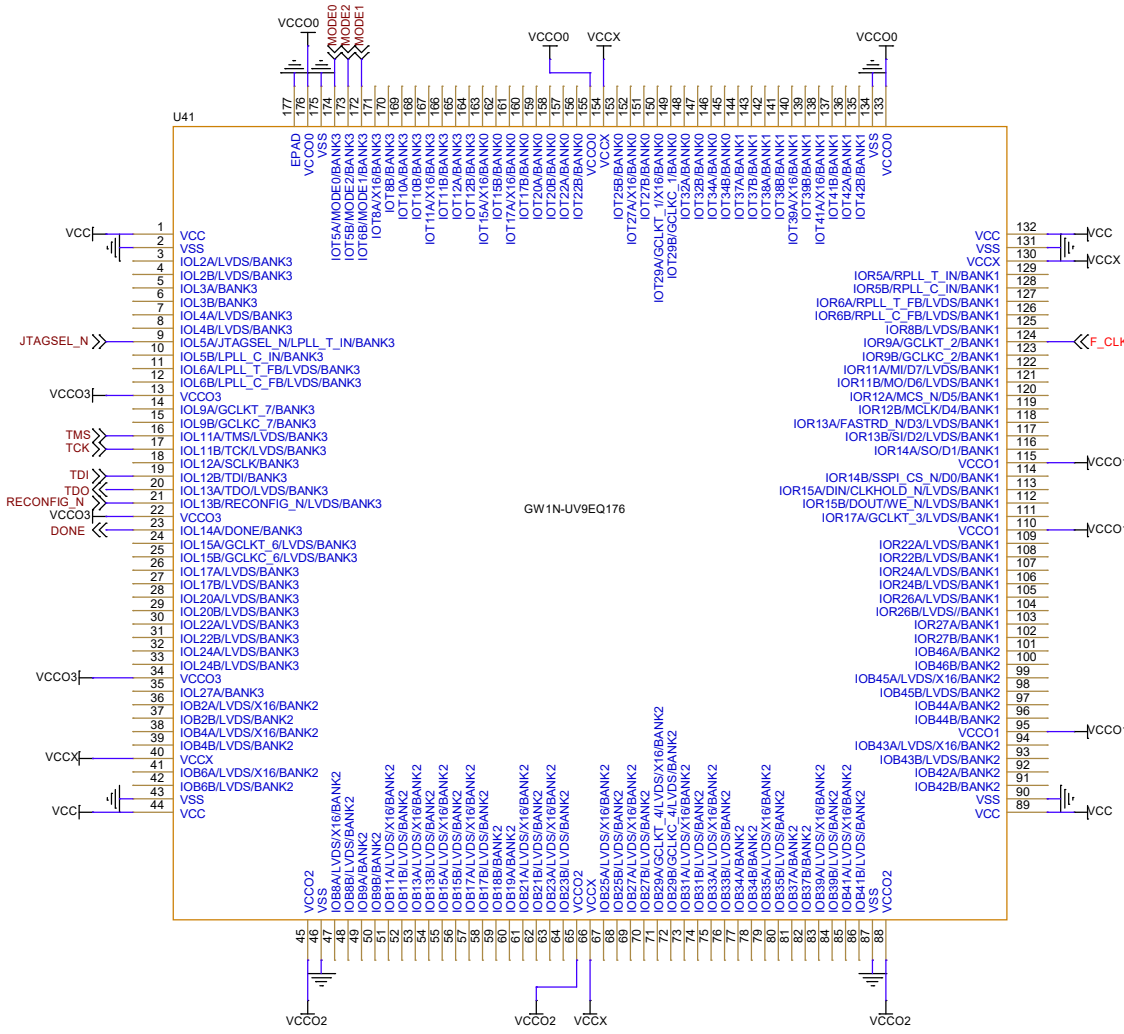
1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.

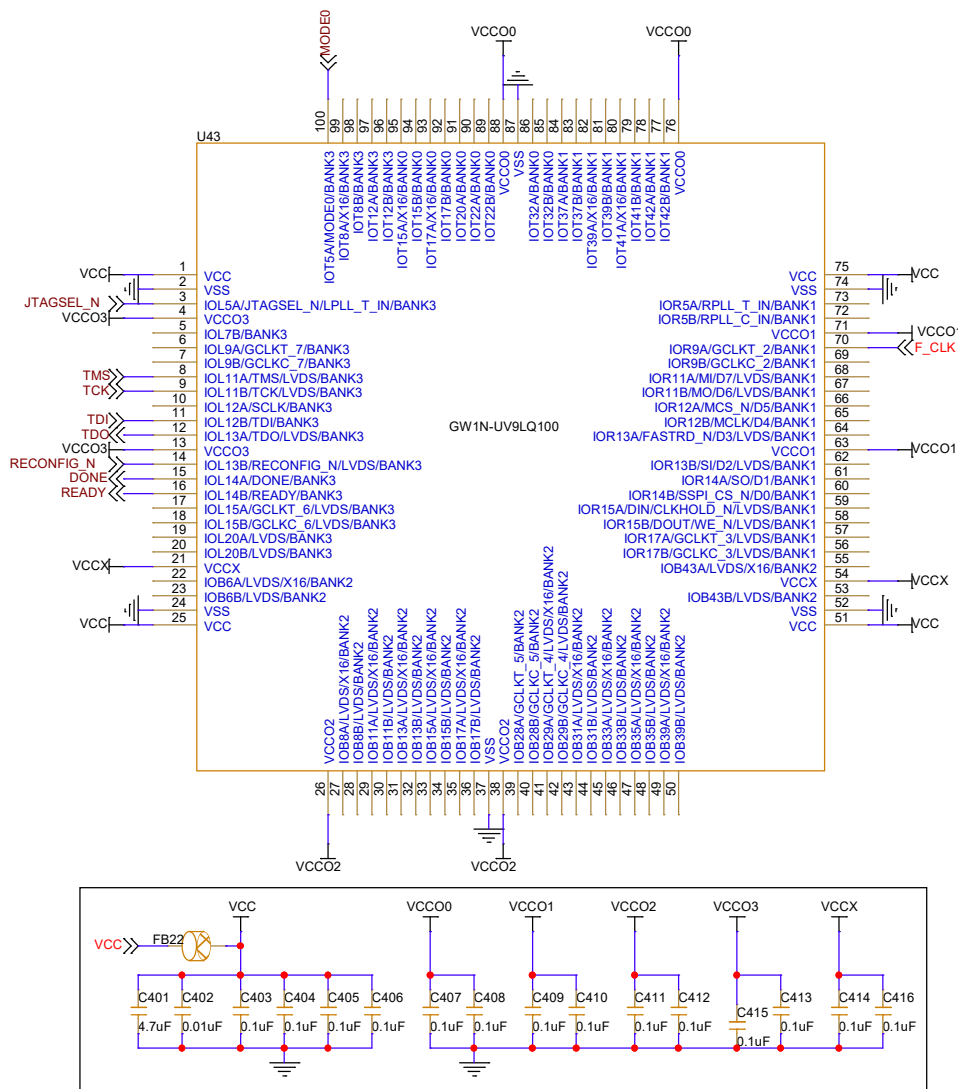


- 1.F CLK signal is an external input clock signal.
 \bar{I} is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title			
GOWIN Minimum System Diagram			
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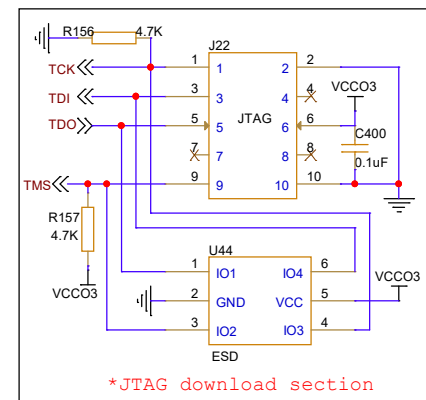
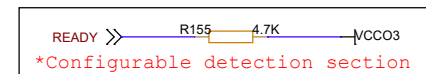
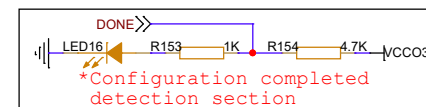
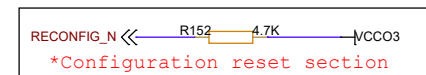
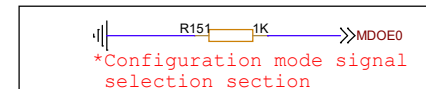
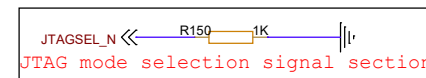


Notes:
1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

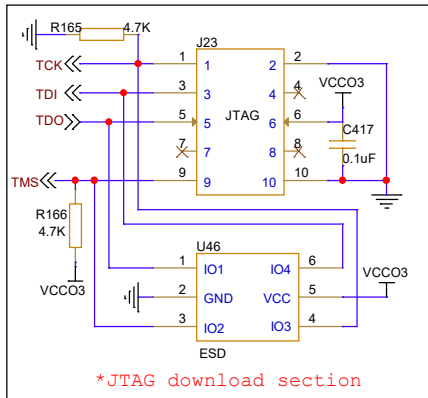
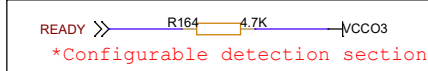
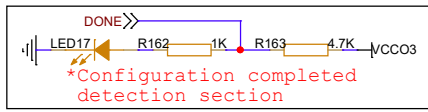
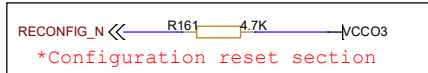
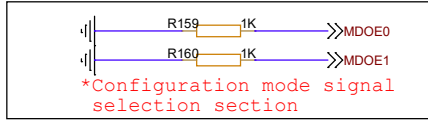
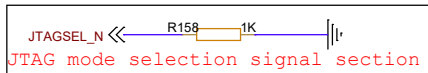
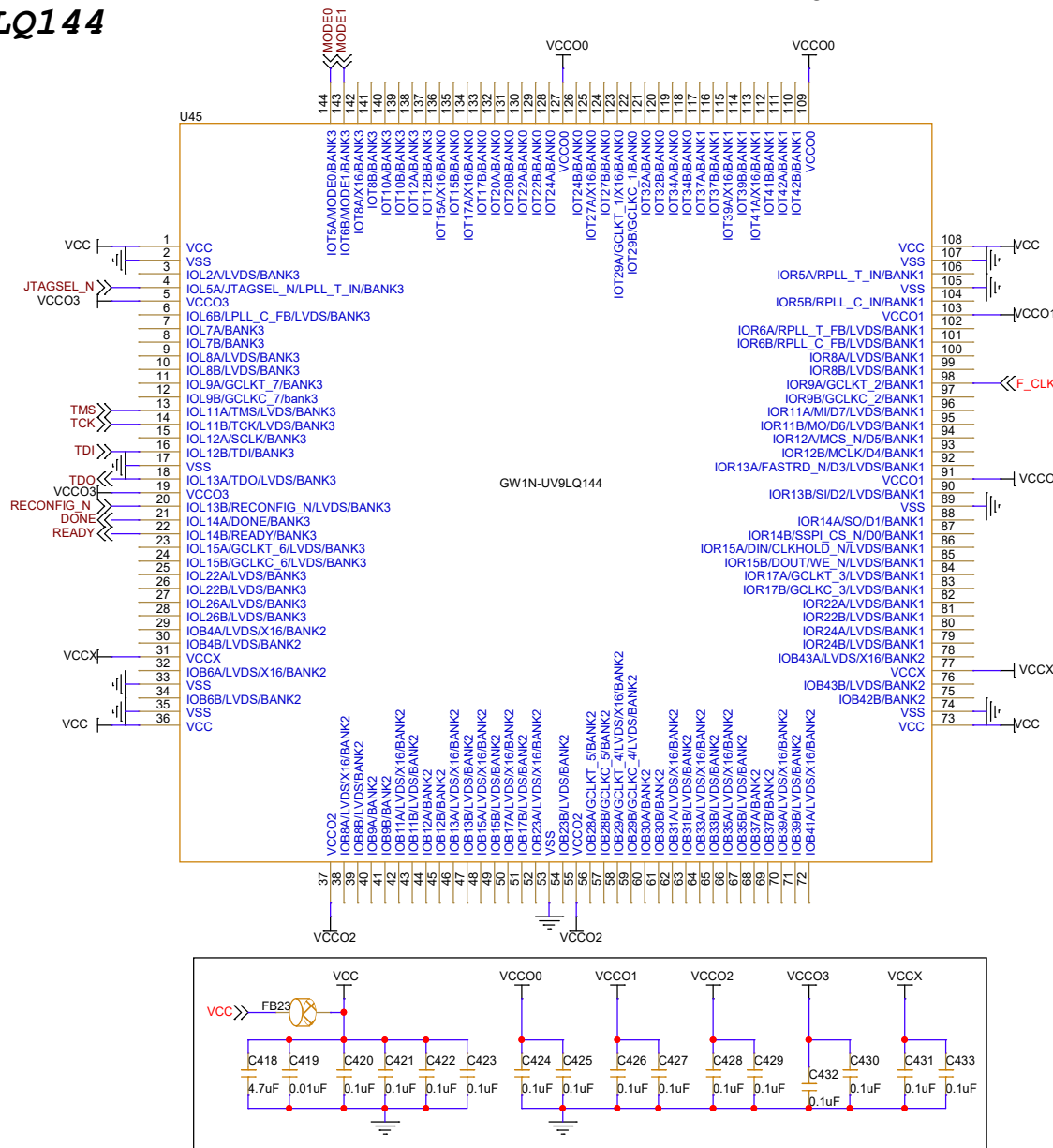


Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

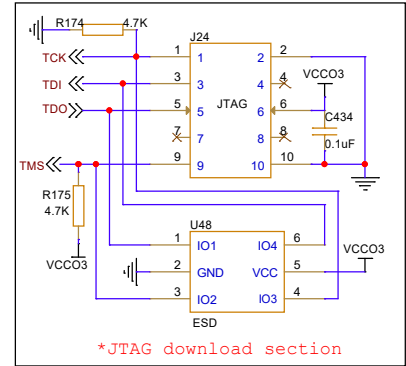


Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-UV9LQ100	2.3
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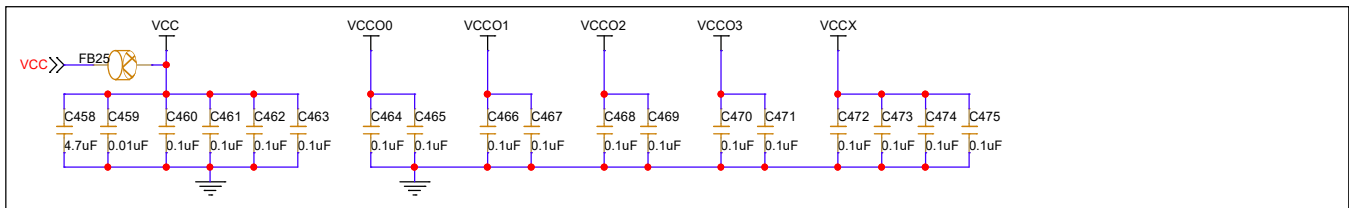
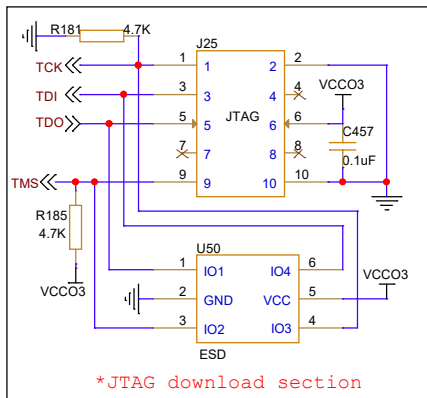
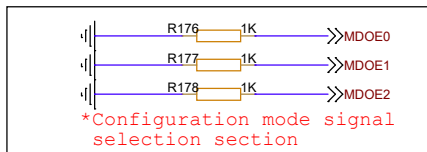
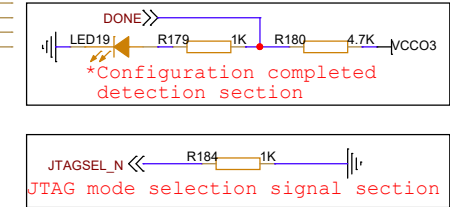
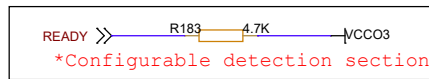
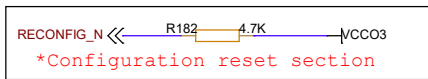
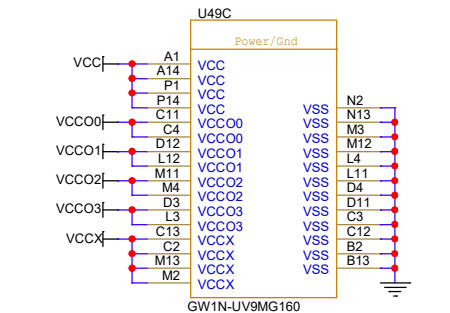
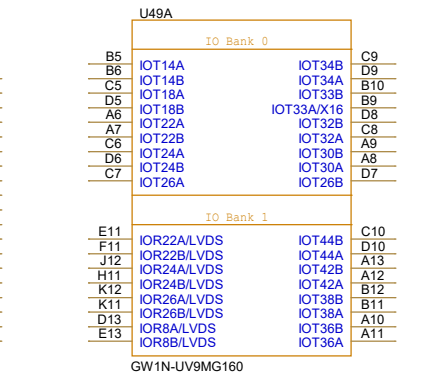
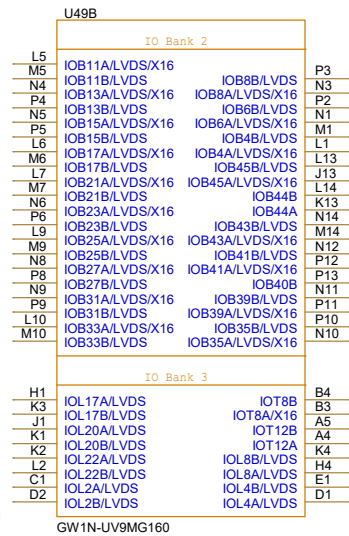
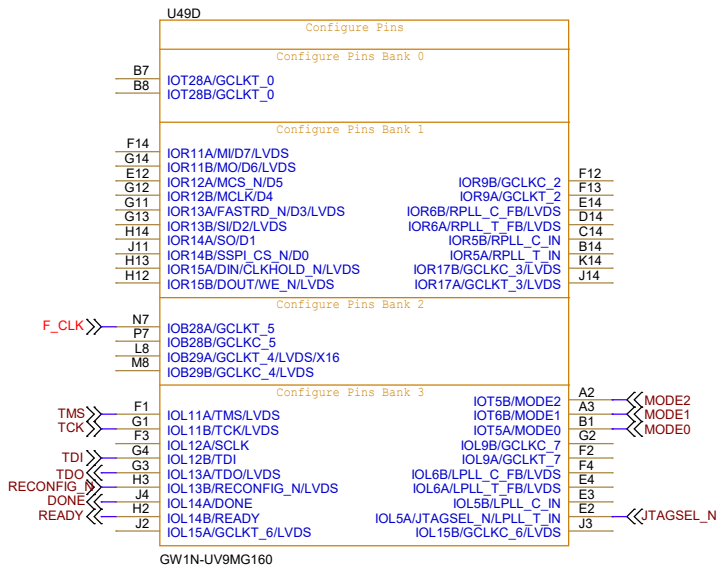


Notes:
 1.F CLK signal is an external input clock signal.
 It is recommended that F_CLK signal be provided through an active oscillator crystal.
 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
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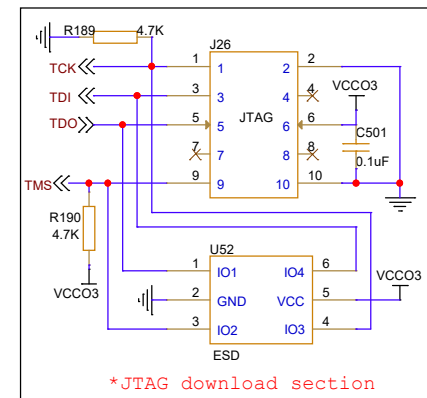
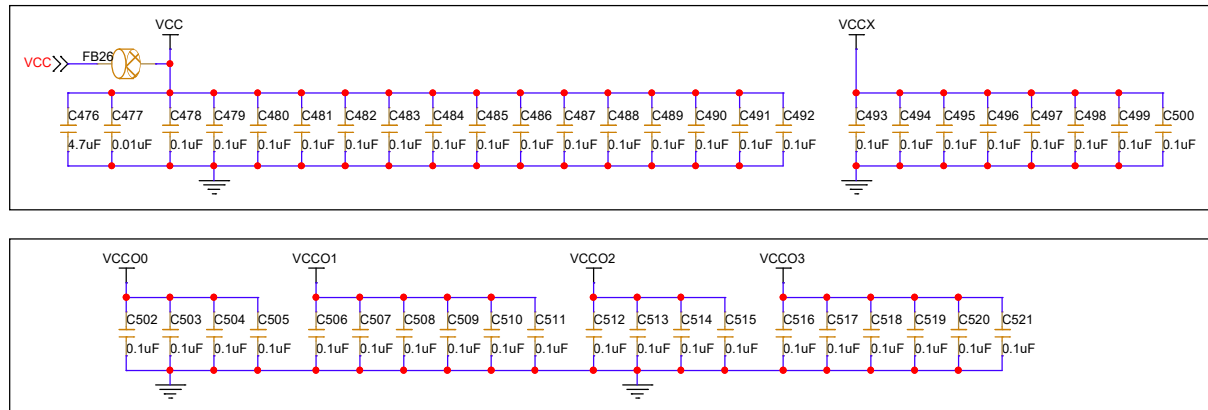
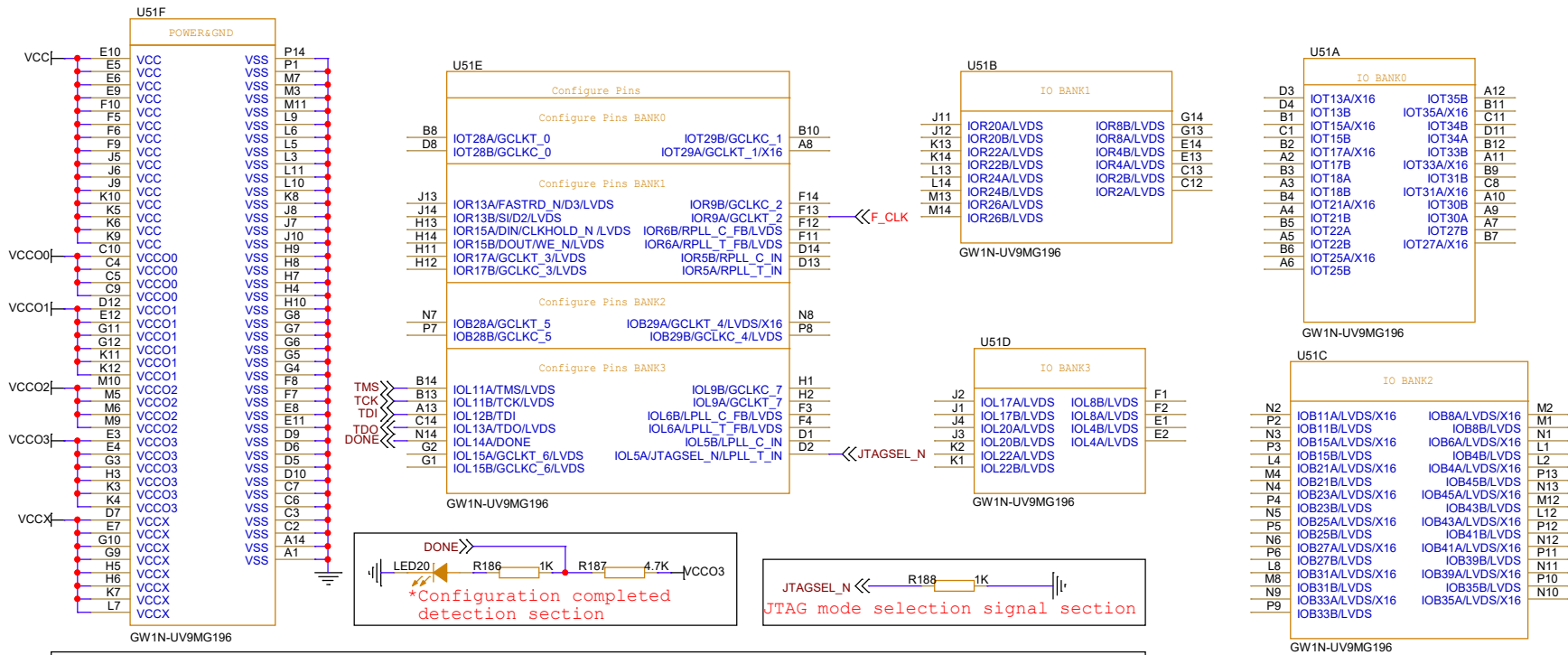


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| Title | | | | |
| GOWIN Minimum System Diagram | | | | |
| Size | Document Number | | | Rev |
| A3 | GW 1N-UV9LQ176 | | | 2.3 |
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Notes:

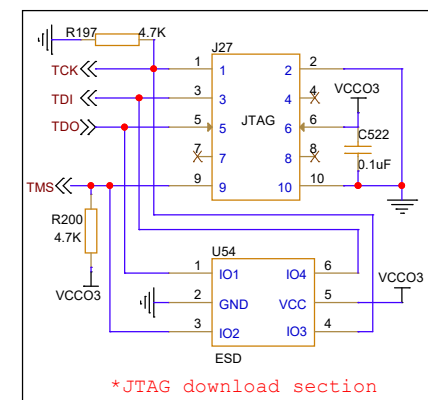
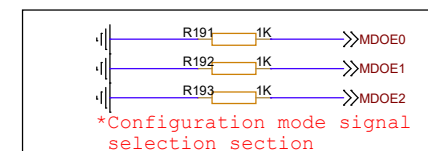
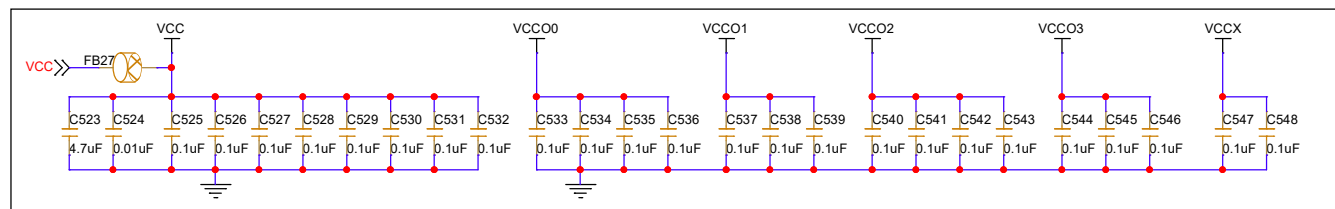
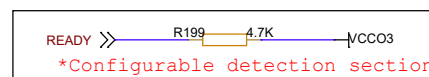
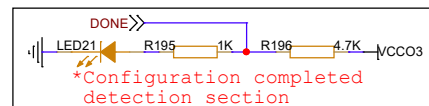
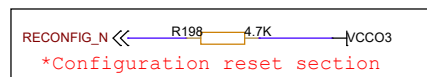
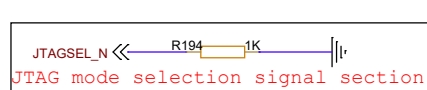
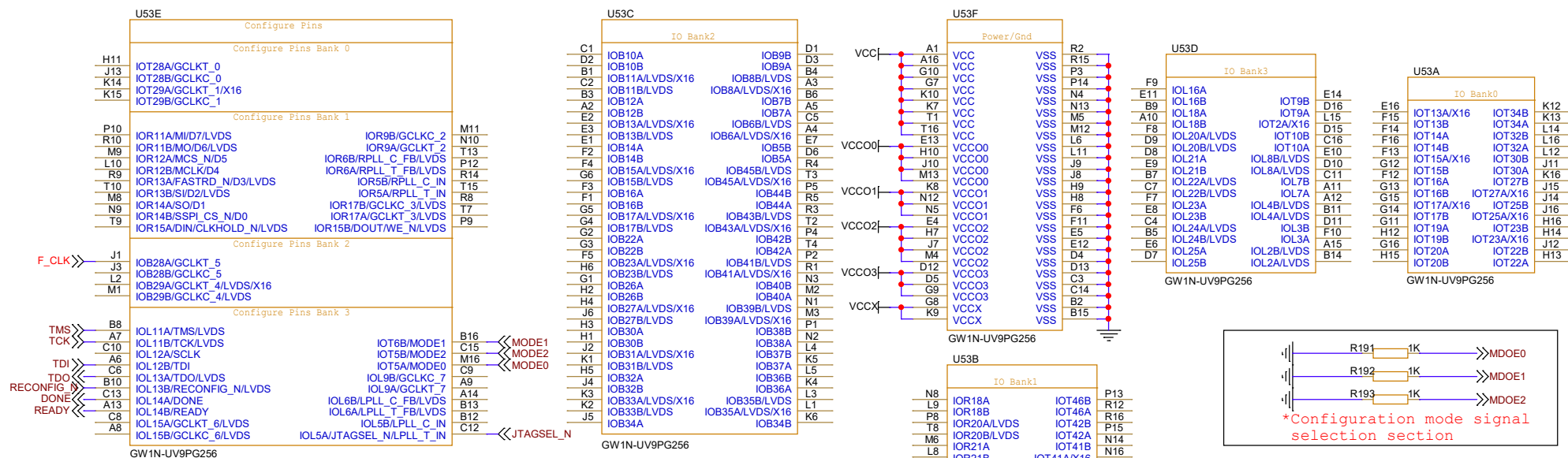
- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

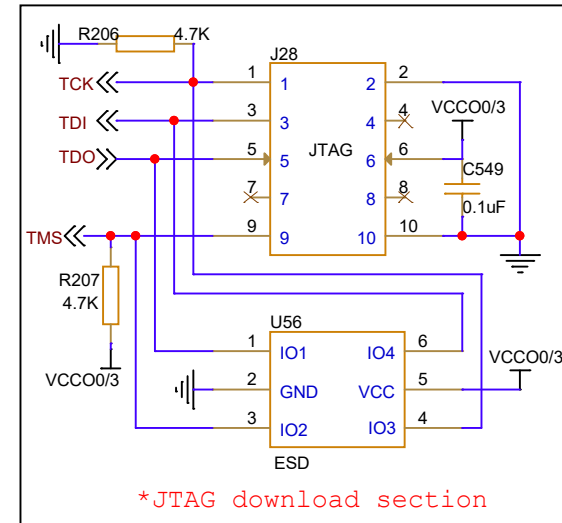
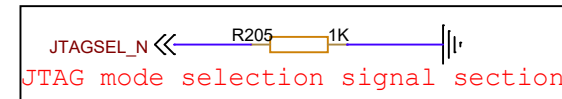
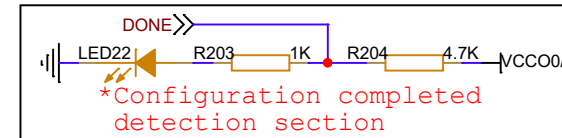
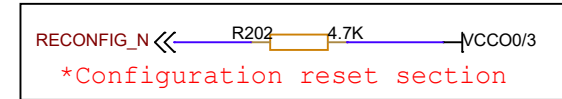
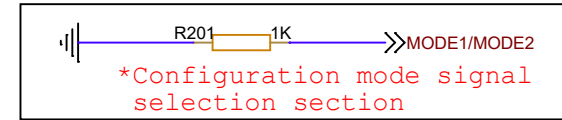
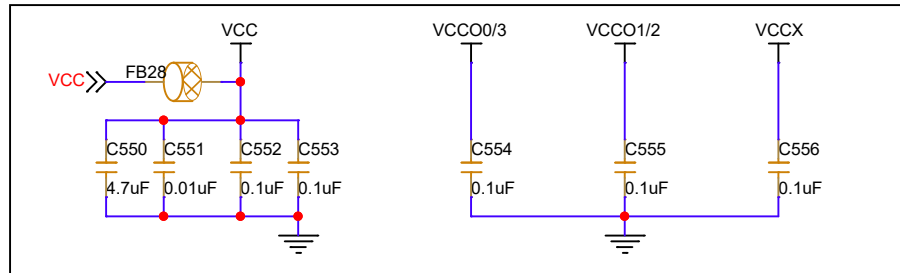
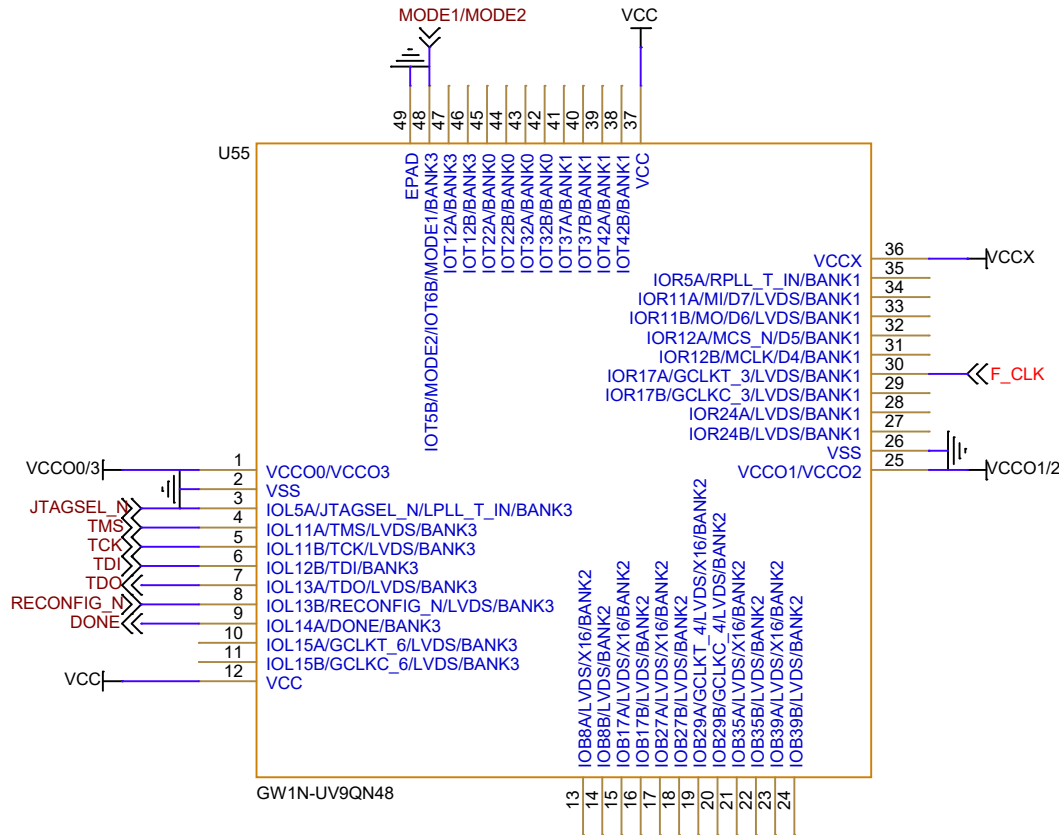
Title		
GOWIN Minimum System Diagram		
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Notes:

- 1.F CLK signal is an external input clock signal.
 $\bar{I_T}$ is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

GW1N-UV9QN48

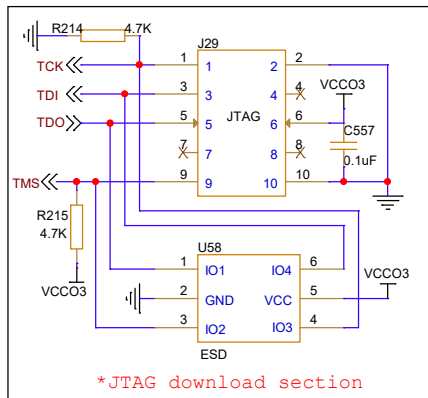
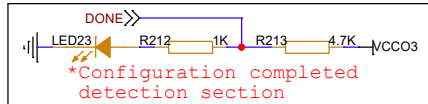
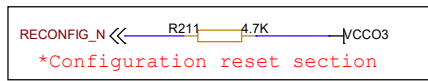
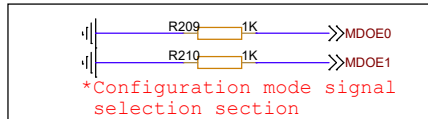
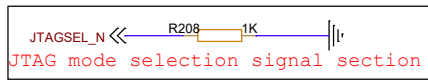
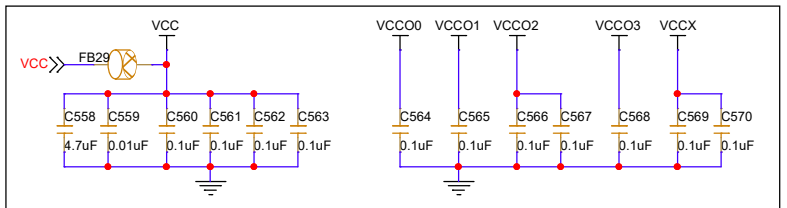
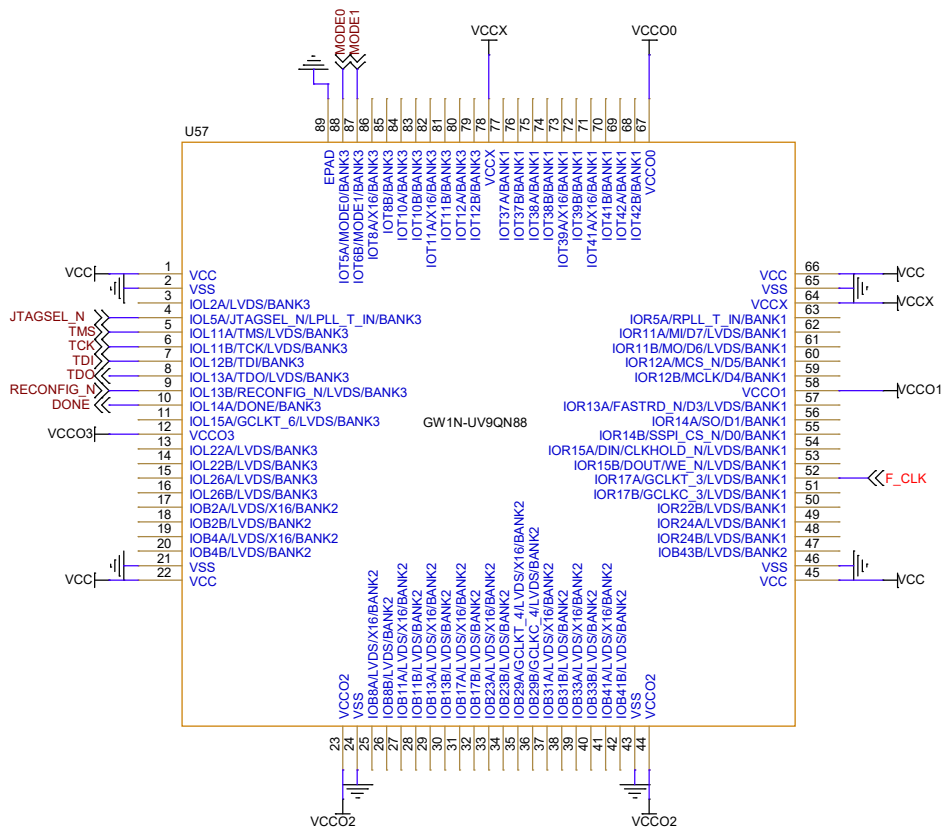


Notes:

1.F_CLK signal is an external input clock signal.

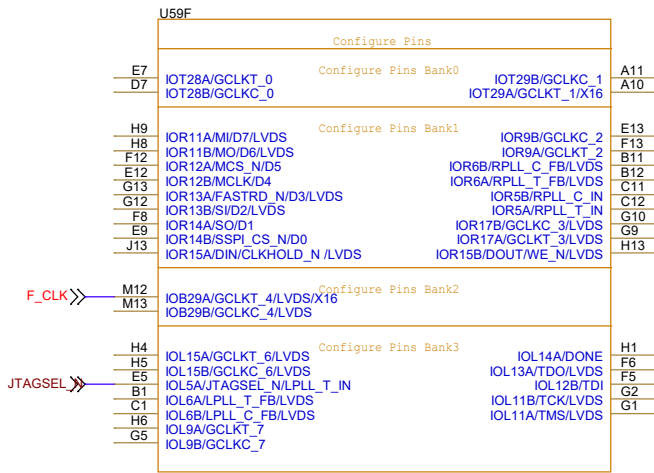
It is recommended that F_CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.

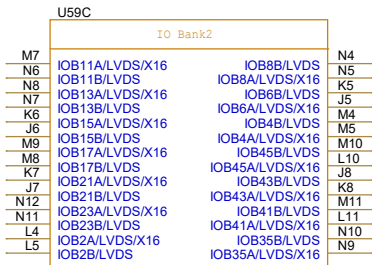


Notes:
1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

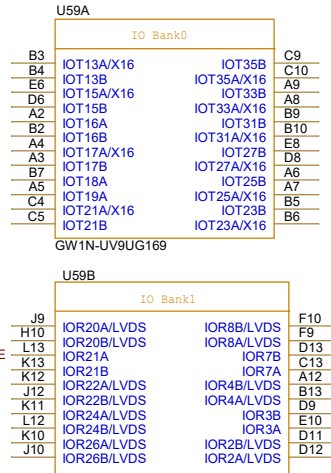
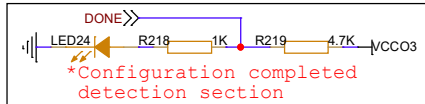
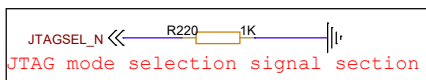
Title			
GOWIN Minimum System Diagram			
Size	Document Number	Rev	
B	GW1N-UV9QN88	2.3	
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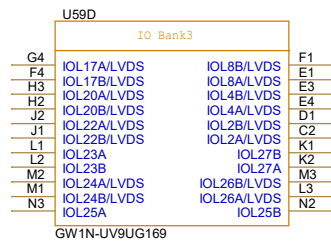
GW1N-UV9UG169



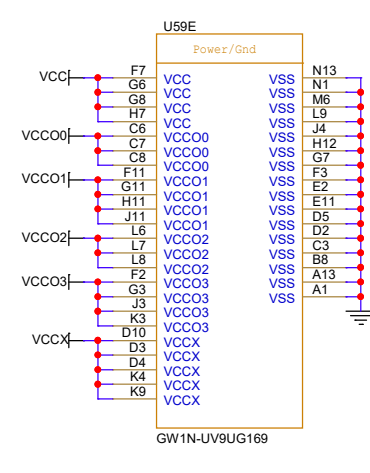
GW1N-UV9UG169



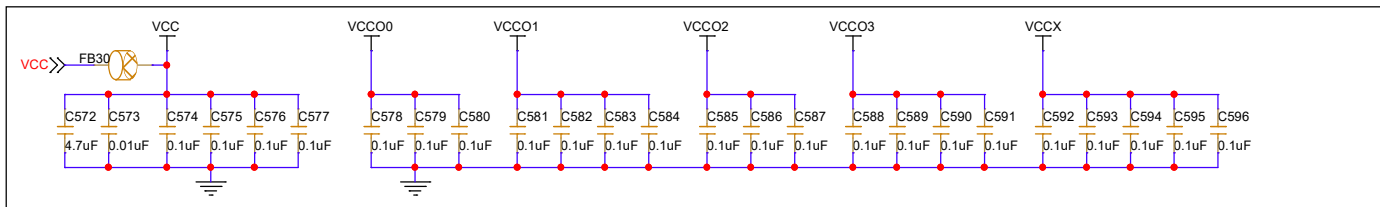
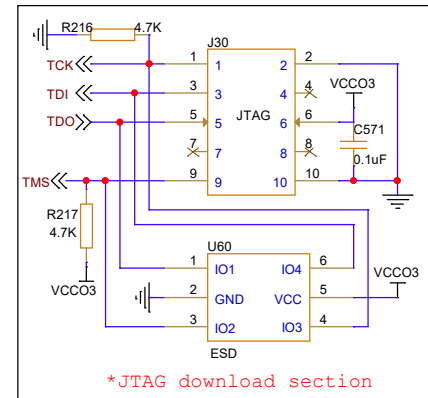
GW1N-UV9UG169



GW1N-UV9UG169



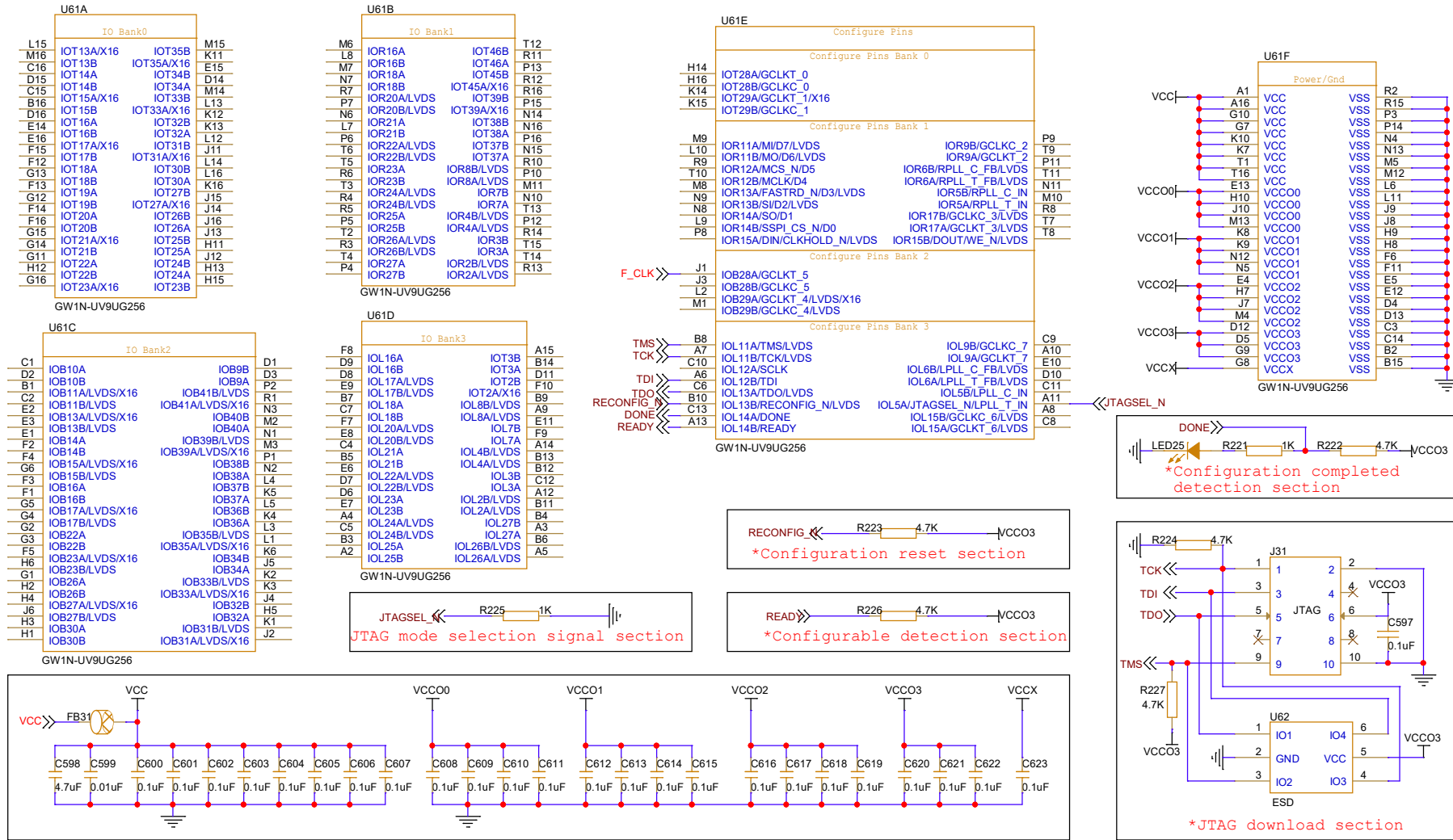
GW1N-UV9UG169



Notes:

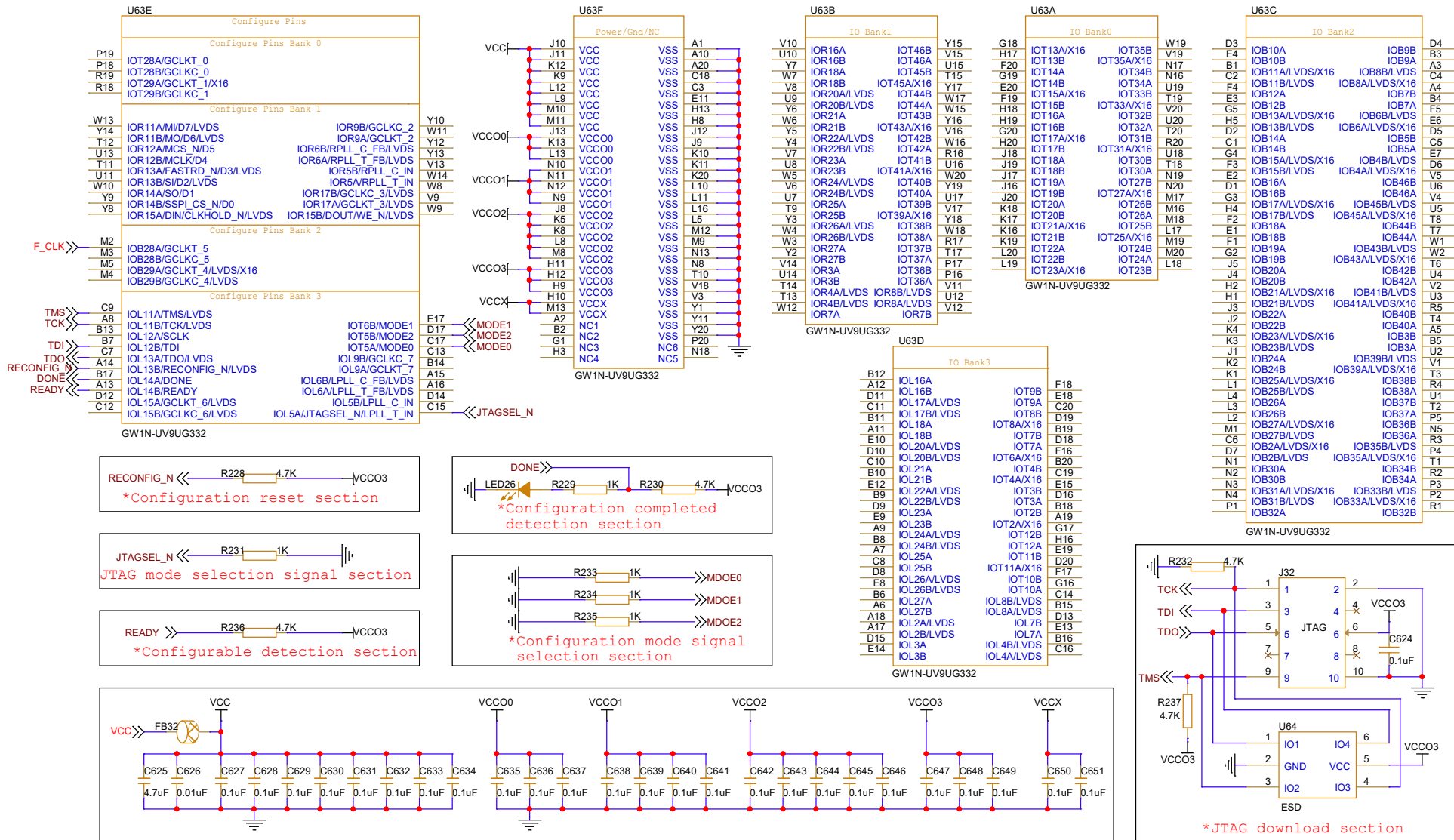
- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
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B	GW1N-UV9UG169	2.3
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- Notes:
- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
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B	GW1N-UV9UG256	2.3
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- Notes:
- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
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B	GW1N-UV9UG332	2.3
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