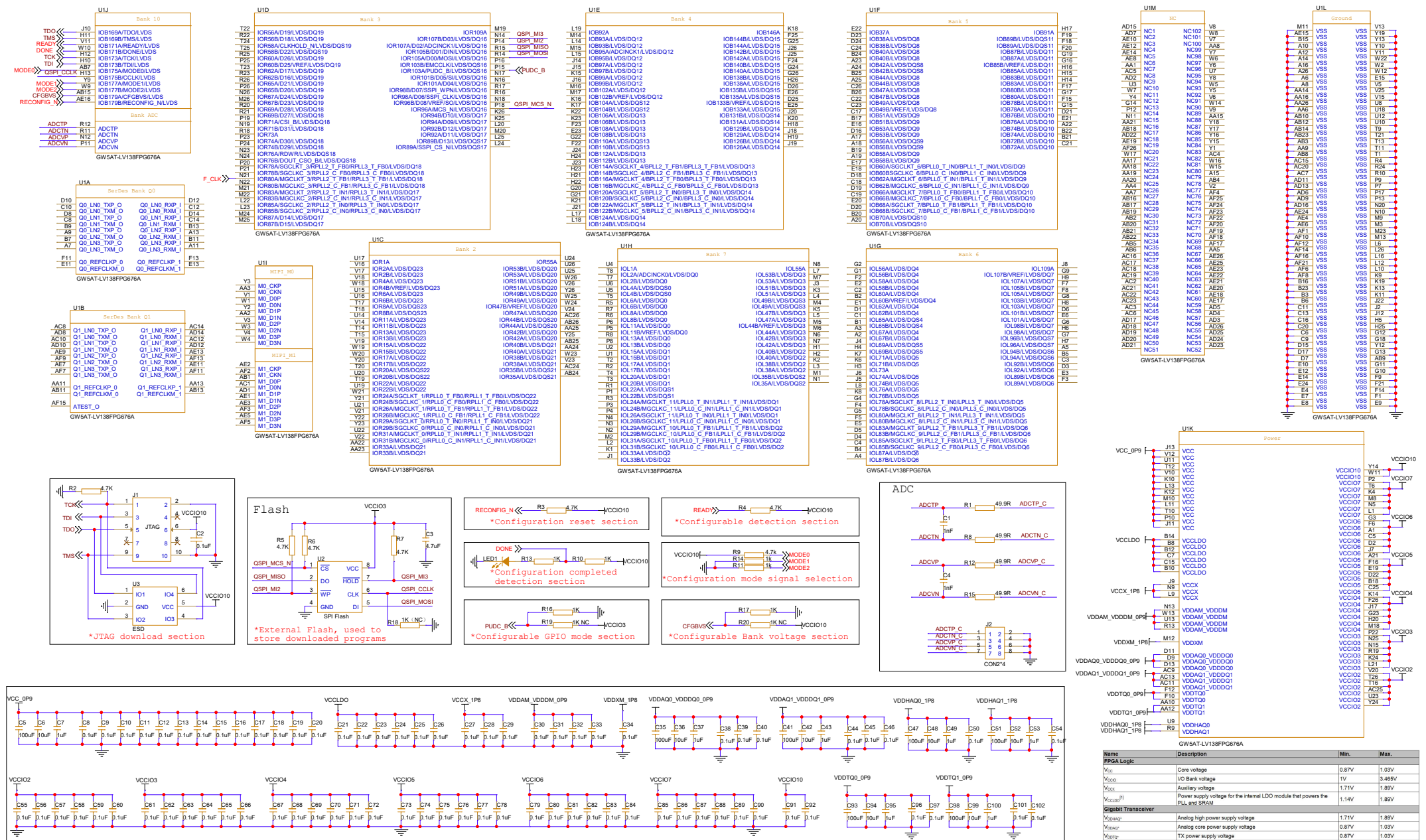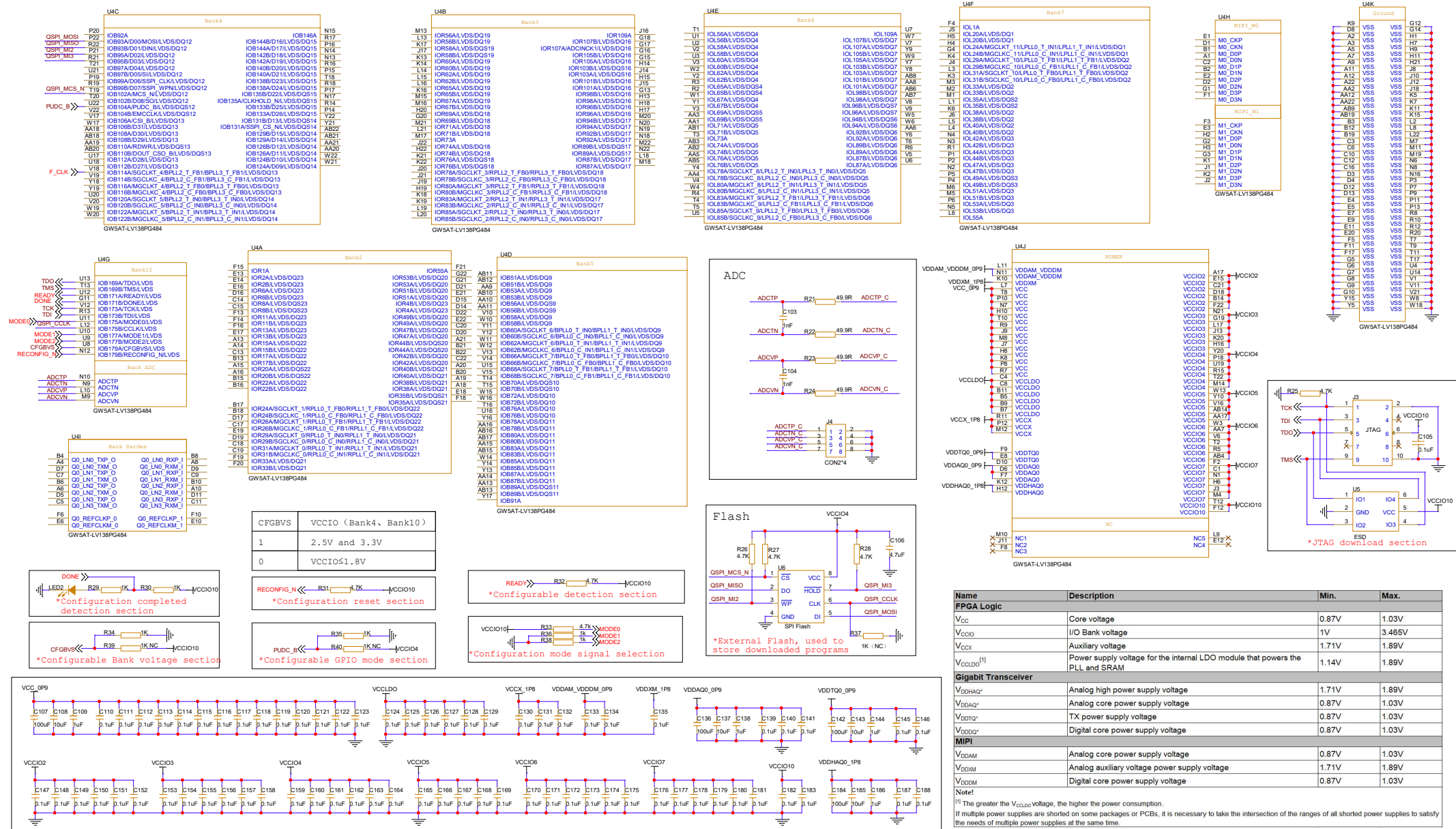# GW5AT-LV138FPG676A

Notes:
1. F_CLK signal is an external input clock signal.
   It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
   For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG704, Arora V 138K FPGA Products Programming and Configuration Guide .
3. It is recommended that add an ESD protection code to the JTAG download circuit.
4. VCC core voltage requires a large current, so it is recommended to supply power separately.
5. The MODE pin is the GowinCONFIG configuration mode selection signal.
   For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, Arora V 138K FPGA Products Programming and Configuration Guide.

Section annotations
- *JTAG download section
- Flash — *External Flash, used to store downloaded programs
- *Configuration reset section
- *Configuration completed detection section
- *Configurable GPIO mode section
- *Configurable detection section
- *Configuration mode signal selection
- *Configurable Bank voltage section
- ADC

CFGBVS	VCCIO (Bank3、Bank10)
1	2.5V and 3.3V
0	VCCIO≤1.8V

Name	Description	Min.	Max.
FPGA Logic			
V_CC	Core voltage	0.87V	1.03V
V_CCIO	I/O Bank voltage	1V	3.465V
V_CCX	Auxiliary voltage	1.71V	1.89V
V_CCLDO [1]	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	1.89V
Gigabit Transceiver			
V_DDHAQ*	Analog high power supply voltage	1.71V	1.89V
V_DDAQ*	Analog core power supply voltage	0.87V	1.03V
V_DDTQ*	TX power supply voltage	0.87V	1.03V
V_DDDQ*	Digital core power supply voltage	0.87V	1.03V
MIPI			
V_DDAM	Analog core power supply voltage	0.87V	1.03V
V_DDXM	Analog auxiliary voltage power supply voltage	1.71V	1.89V
V_DDDM	Digital core power supply voltage	0.87V	1.03V

Note!
[1] The greater the V_CCLDO voltage, the higher the power consumption.
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.

GW5AT-LV138PG484

Notes:
1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG704,
Arora V 138K FPGA Products Programming and Configuration Guide .
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. VCC core voltage requires a large current, so it is recommended to supply power separately.
5. The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704,
Arora V 138K FPGA Products Programming and Configuration Guide.

Bank / Block labels

- U4C — Bank4 — GW5AT-LV138PG484
- U4B — Bank3 — GW5AT-LV138PG484
- U4E — Bank6 — GW5AT-LV138PG484
- U4F — Bank7 — GW5AT-LV138PG484
- U4H — MIPI_M0 / MIPI_M1 — GW5AT-LV138PG484
- U4K — Ground — GW5AT-LV138PG484
- U4G — Bank10 — GW5AT-LV138PG484
- U4A — Bank2 — GW5AT-LV138PG484
- U4D — Bank5 — GW5AT-LV138PG484
- Bank ADC
- U4I — Bank Serdes — GW5AT-LV138PG484
- U4J — POWER / NC — GW5AT-LV138PG484
- ADC
- Flash

CFGBVS table

CFGBVS	VCCIO（Bank4、Bank10）
1	2.5V and 3.3V
0	VCCIO≤1.8V

Configuration completed detection section
Configuration reset section
Configurable detection section
Configurable Bank voltage section
Configurable GPIO mode section
Configuration mode signal selection
External Flash, used to store downloaded programs
JTAG download section

SPI Flash
CON2*4

Power specification table

Name	Description	Min.	Max.
FPGA Logic			
V_{CC}	Core voltage	0.87V	1.03V
V_{CCIO}	I/O Bank voltage	1V	3.465V
V_{CCX}	Auxiliary voltage	1.71V	1.89V
V_{CCLDO}[1]	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	1.89V
Gigabit Transceiver			
V_{DDHAQ*}	Analog high power supply voltage	1.71V	1.89V
V_{DDAQ*}	Analog core power supply voltage	0.87V	1.03V
V_{DDTQ*}	TX power supply voltage	0.87V	1.03V
V_{DDDQ*}	Digital core power supply voltage	0.87V	1.03V
MIPI			
V_{DDAM}	Analog core power supply voltage	0.87V	1.03V
V_{DDXM}	Analog auxiliary voltage power supply voltage	1.71V	1.89V
V_{DDDM}	Digital core power supply voltage	0.87V	1.03V

Note!
[1] The greater the V_{CCLDO} voltage, the higher the power consumption.
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.

Decoupling capacitor rails

VCC_0P9, VCCLDO, VCCX_1P8, VDDAM_VDDDM_0P9, VDDXM_1P8, VDDAQ0_0P9, VDDTQ0_0P9
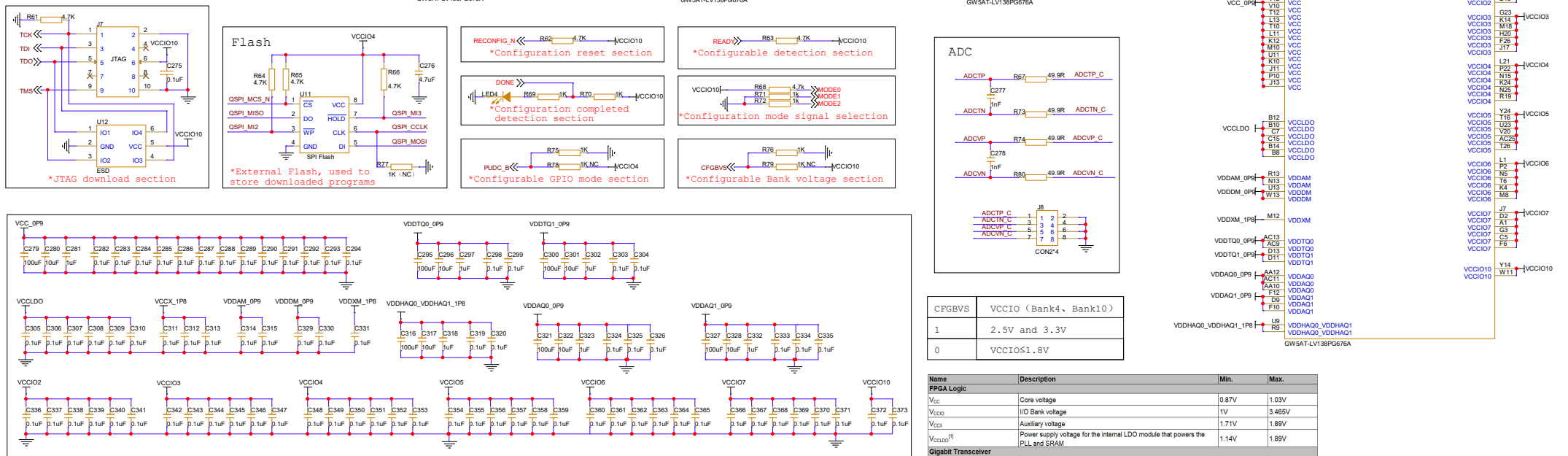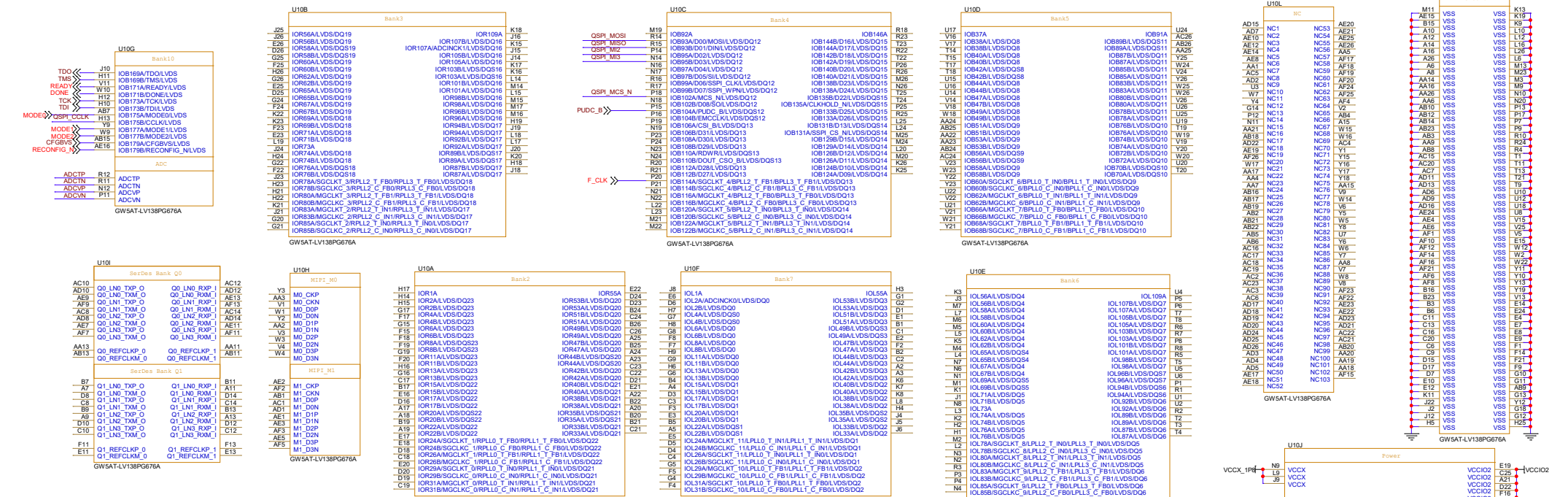VCCIO2, VCCIO3, VCCIO4, VCCIO5, VCCIO6, VCCIO7, VCCIO10, VDDHAQ0_1P8
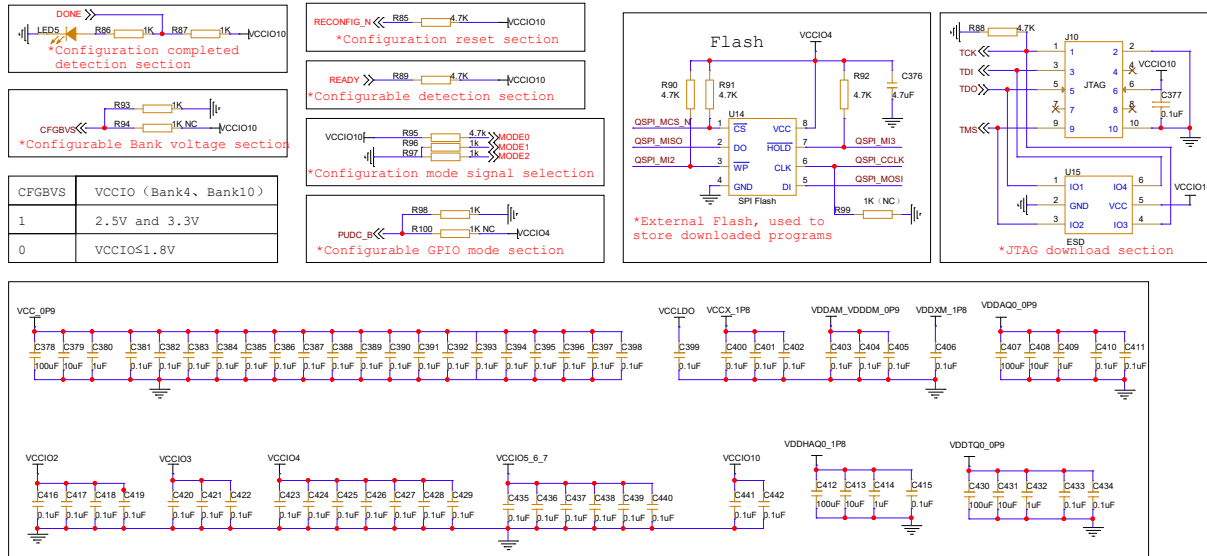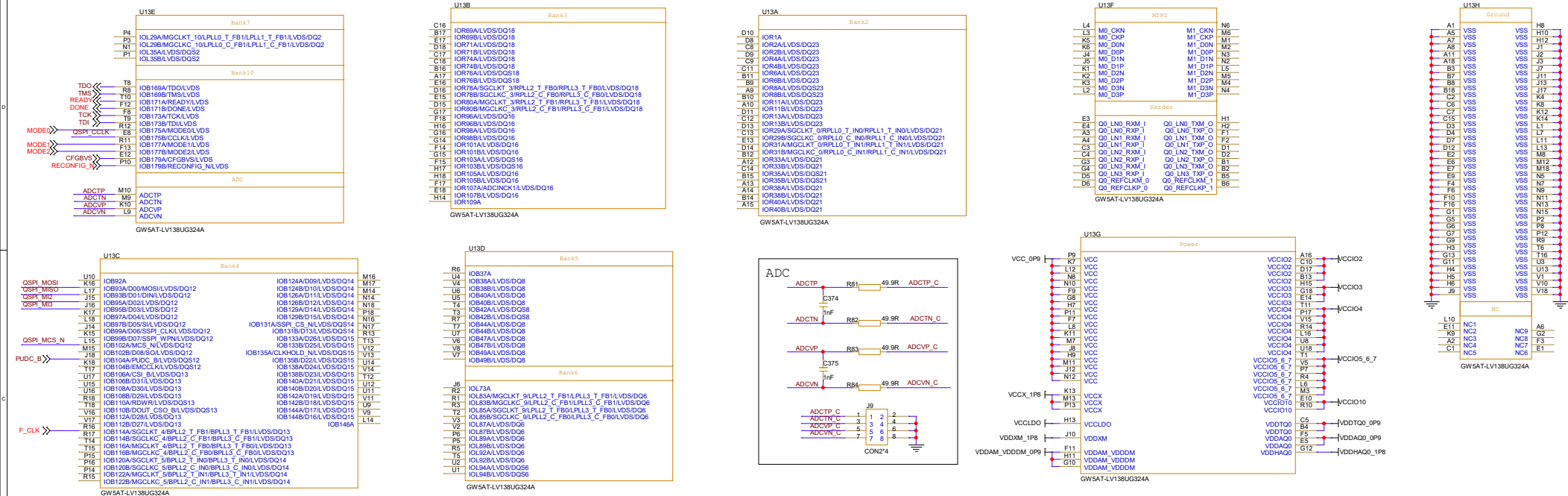
GW5AT-LV138PG484A

Notes:
1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG704,
Arora V 138K FPGA Products Programming and Configuration Guide .
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. VCC core voltage requires a large current, so it is recommended to supply power separately.
5. The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704,
Arora V 138K FPGA Products Programming and Configuration Guide.

CFGBVS	VCCIO（Bank4、Bank10）
1	2.5V and 3.3V
0	VCCIO≤1.8V

*Configuration reset section
*Configurable detection section
*Configurable GPIO mode section
*Configuration mode signal selection
*Configurable Bank voltage section
*External Flash, used to store downloaded programs
*Configuration completed detection section
*JTAG download section

Flash
SPI Flash
ADC
Power
Ground

Name	Description	Min.	Max.
FPGA Logic			
V_{CC}	Core voltage	0.87V	1.03V
V_{CCO}	I/O Bank voltage	1V	3.465V
V_{CCX}	Auxiliary voltage	1.71V	1.89V
V_{CCLDO}[1]	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	1.89V
Gigabit Transceiver			
V_{DDHAQ}	Analog high power supply voltage	1.71V	1.89V
V_{DDAQ}	Analog core power supply voltage	0.87V	1.03V
V_{DDTQ}	TX power supply voltage	0.87V	1.03V
V_{DDDQ}	Digital core power supply voltage	0.87V	1.03V
MIPI			
V_{DDAM}	Analog core power supply voltage	0.87V	1.03V
V_{DDAM}	Analog auxiliary voltage power supply voltage	1.71V	1.89V
V_{DDDM}	Digital core power supply voltage	0.87V	1.03V

Note!
[1] The greater the V_{CCLDO} voltage, the higher the power consumption.
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.

Bank 4 — U7C — GW5AT-LV138PG484A
Bank 2 — U7A — GW5AT-LV138PG484A
Bank 3 — U7B — GW5AT-LV138PG484A
Bank 10 — U7G
Bank 7 — U7F — GW5AT-LV138PG484A
Bank 6 — U7E — GW5AT-LV138PG484A
Bank 5 — U7D — GW5AT-LV138PG484A
Bank ADC — GW5AT-LV138PG484A
SerDes Bank Q0 — U7H — GW5AT-LV138PG484A
U7J — Power — GW5AT-LV138PG484A
U7I — Ground — GW5AT-LV138PG484A

ESD — U9

GW5AT-LV138PG676A

Flash

ADC

*JTAG download section

*External Flash, used to store downloaded programs

*Configuration reset section

*Configurable detection section

*Configuration completed detection section

*Configuration mode signal selection

*Configurable GPIO mode section

*Configurable Bank voltage section

CFGBVS	VCCIO（Bank4、Bank10）
1	2.5V and 3.3V
0	VCCIO≤1.8V

Notes:
1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG704,
Arora Ⅴ 138K FPGA Products Programming and Configuration Guide .
3.It is recommended that add an ESD protection chip to the JTAG download circuit.
4.VCC core voltage requires a large current, so it is recommended to supply power separately.
5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704,
Arora Ⅴ 138K FPGA Products Programming and Configuration Guide.

Name	Description	Min.	Max.
FPGA Logic			
V_{CC}	Core voltage	0.87V	1.03V
V_{CCIO}	I/O Bank voltage	1V	3.465V
V_{CCX}	Auxiliary voltage	1.71V	1.89V
V_{CCLDO}[1]	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	1.89V
Gigabit Transceiver			
V_{DDHAQ*}	Analog high power supply voltage	1.71V	1.89V
V_{DDAQ*}	Analog core power supply voltage	0.87V	1.03V
V_{DDTQ*}	TX power supply voltage	0.87V	1.03V
V_{DDDQ*}	Digital core power supply voltage	0.87V	1.03V
MIPI			
V_{DDAM}	Analog core power supply voltage	0.87V	1.03V
V_{DDIM}	Analog auxiliary voltage power supply voltage	1.71V	1.89V
V_{DDDM}	Digital core power supply voltage	0.87V	1.03V

[1] The greater the V_{CCLDO} voltage, the higher the power consumption.
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.

GW5AT-LV138UG324A

(Schematic sheet — FPGA minimum system diagram. Key text blocks below.)

Power Supply Specification Table

Name	Description	Min.	Max.
FPGA Logic			
VCC	Core voltage	0.87V	1.03V
VCCIO	I/O Bank voltage	1V	3.465V
VCCX	Auxiliary voltage	1.71V	1.89V
VCCLDO [1]	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	1.89V
Gigabit Transceiver			
VDDHAQ*	Analog high power supply voltage	1.71V	1.89V
VDDAQ*	Analog core power supply voltage	0.87V	1.03V
VDDTQ*	TX power supply voltage	0.87V	1.03V
VDDDQ*	Digital core power supply voltage	0.87V	1.03V
MIPI			
VDDAM	Analog core power supply voltage	0.87V	1.03V
VDDXM	Analog auxiliary voltage power supply voltage	1.71V	1.89V
VDDDM	Digital core power supply voltage	0.87V	1.03V

Note!

[1] The greater the VCCLDO voltage, the higher the power consumption.
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.

CFGBVS Table

CFGBVS	VCCIO（Bank4、Bank10）
1	2.5V and 3.3V
0	VCCIO≤1.8V

Section labels

- *Configuration completed detection section
- *Configurable Bank voltage section
- *Configuration reset section
- *Configurable detection section
- *Configuration mode signal selection
- *Configurable GPIO mode section
- *External Flash, used to store downloaded programs
- *JTAG download section

Flash

ADC

Notes:

1. F_CLK signal is an external input clock signal.
   It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
   For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG704,
   Arora V 138K FPGA Products Programming and Configuration Guide .
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. VCC core voltage requires a large current, so it is recommended to supply power separately.
5. The MODE pin is the GowinCONFIG configuration mode selection signal.
   For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704,
   Arora V 138K FPGA Products Programming and Configuration Guide.