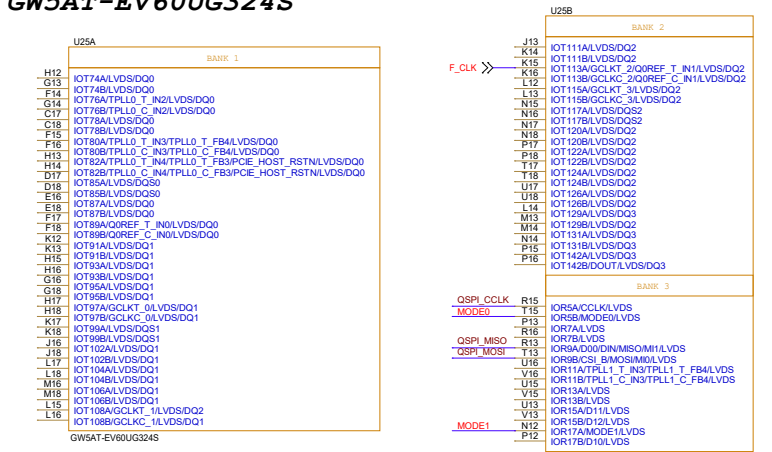
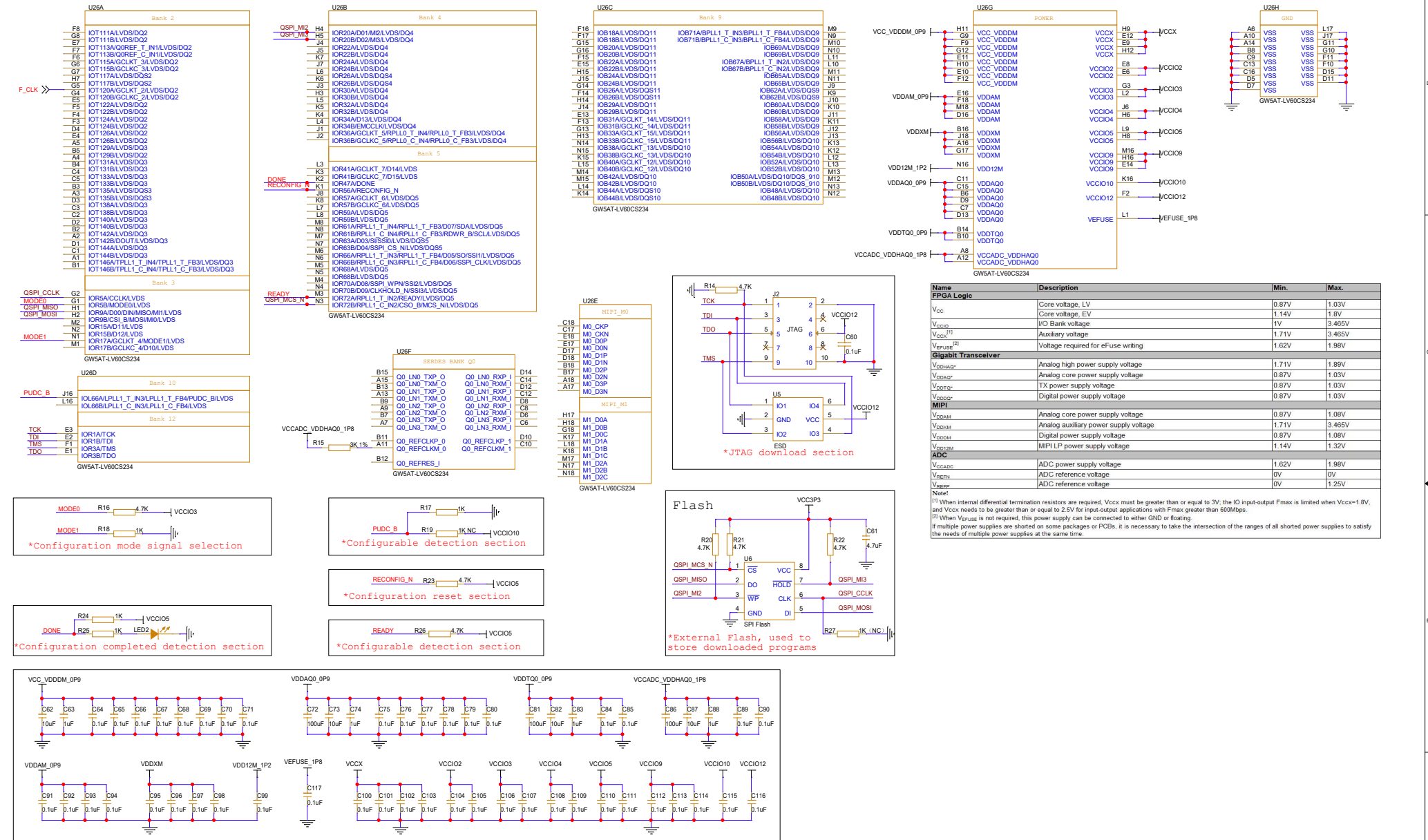


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GW5AT-LV60CS234

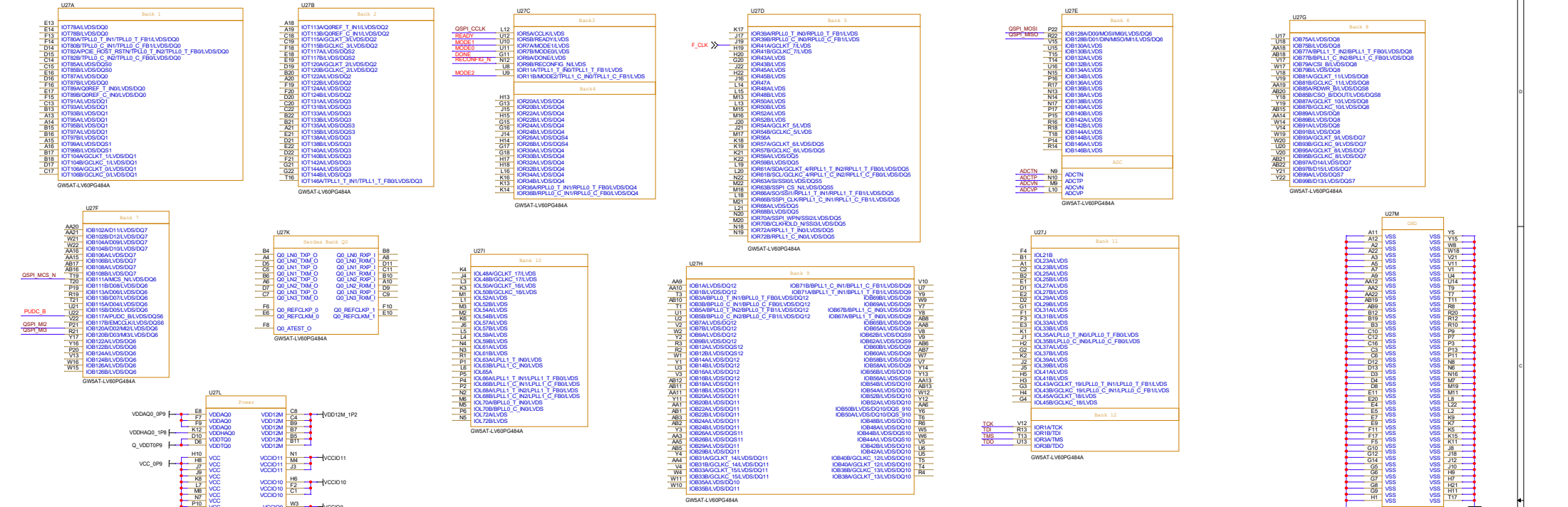


Notes:

- 1.F CLK signal is an external input clock signal.
- It is recommended that F.CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.
- If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

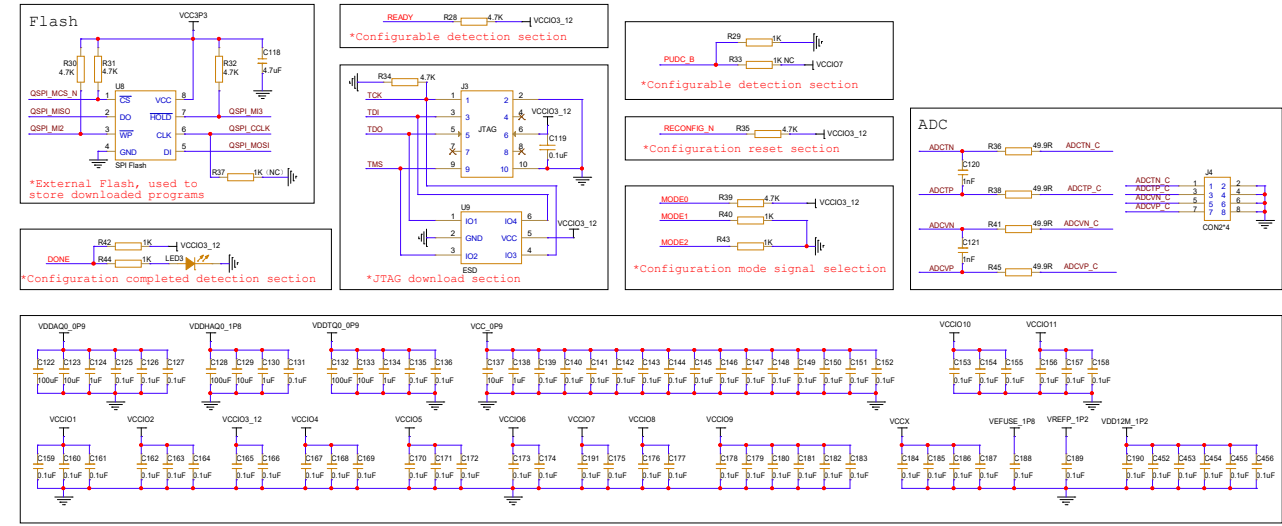
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GOWIN Minimum System Diagram		
Size	Document Number	Rev
C	GW5AT-LV60CS234	1.5
Date:	Wednesday, May 28, 2025	Sheet 2 of 7

GW5AT-LV60PG484A

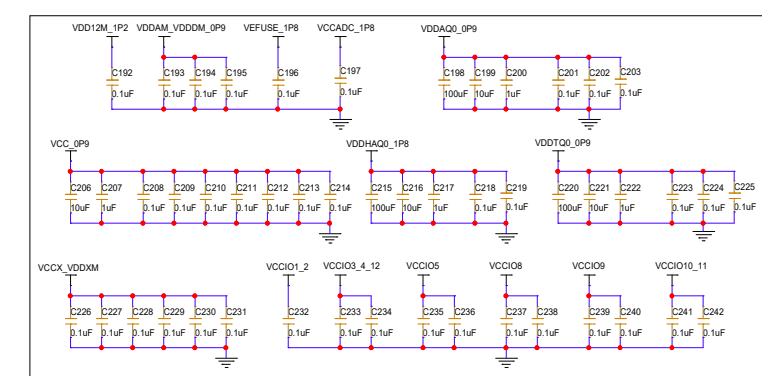
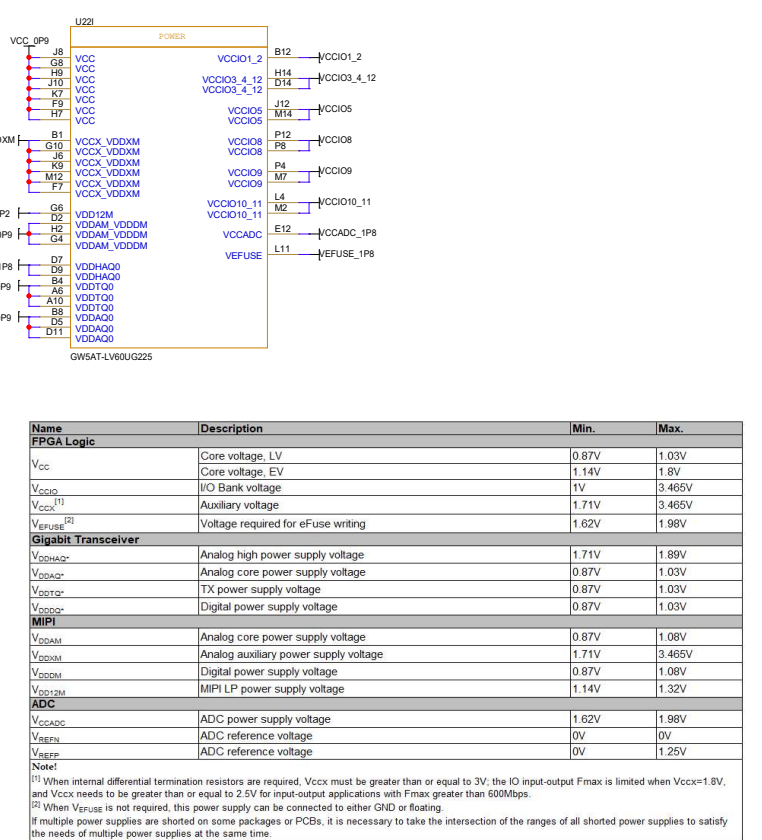


Name	Description	I _{Min}	I _{Max}
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
V _{CC}	Core voltage, EV	1.14V	1.8V
V _{DDIO}	I/O Bank voltage	1.1V	3.465V
V _{CCIO1}	Auxiliary voltage	1.71V	3.465V
V _{DDIO1}	Voltage required for eFUSE writing	1.62V	1.88V
Digital Transceiver			
V _{DDIOA0}	Analog high power supply voltage	1.71V	1.88V
V _{DDIOA1}	Analog core power supply voltage	0.87V	1.03V
V _{DDIOA2}	TX power supply voltage	0.87V	1.03V
V _{DDIOA3}	Digital core power supply voltage	0.87V	1.03V
MIPI			
V _{DDIOA4}	Analog core power supply voltage	0.87V	1.08V
V _{DDIOA5}	Analog auxiliary power supply voltage	1.71V	3.465V
V _{DDIOA6}	Digital power supply voltage	0.87V	1.08V
V _{DDIOA7}	MIPI LP power supply voltage	1.14V	1.32V
ADC			
V _{DDIOA8}	ADC power supply voltage	1.62V	1.88V
V _{DDIOA9}	ADC reference voltage	0V	0V
V _{DDIOA10}	ADC reference voltage	0V	1.25V

Notes:
1.F.CLK signal is an external input clock signal.
2.External Flash memory is used to store downloaded programs.
For details about SPI Flash mode selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide .
3.It is recommended that add an ESD protection chip to the JTAG download circuit.
4.VCC core voltage requires a large current, so it is recommended to supply power separately.
5.The MODE pin is the GwinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide .
6.The MSPi signal levels must match the Flash power supply voltage.
If the voltage of the MSPi BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.



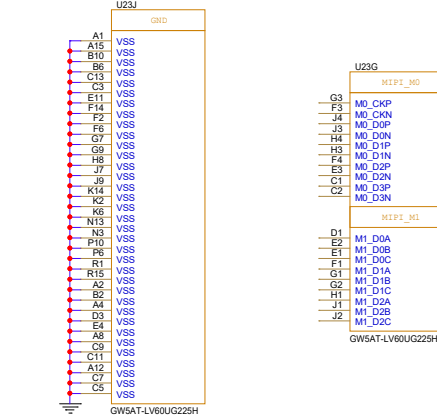
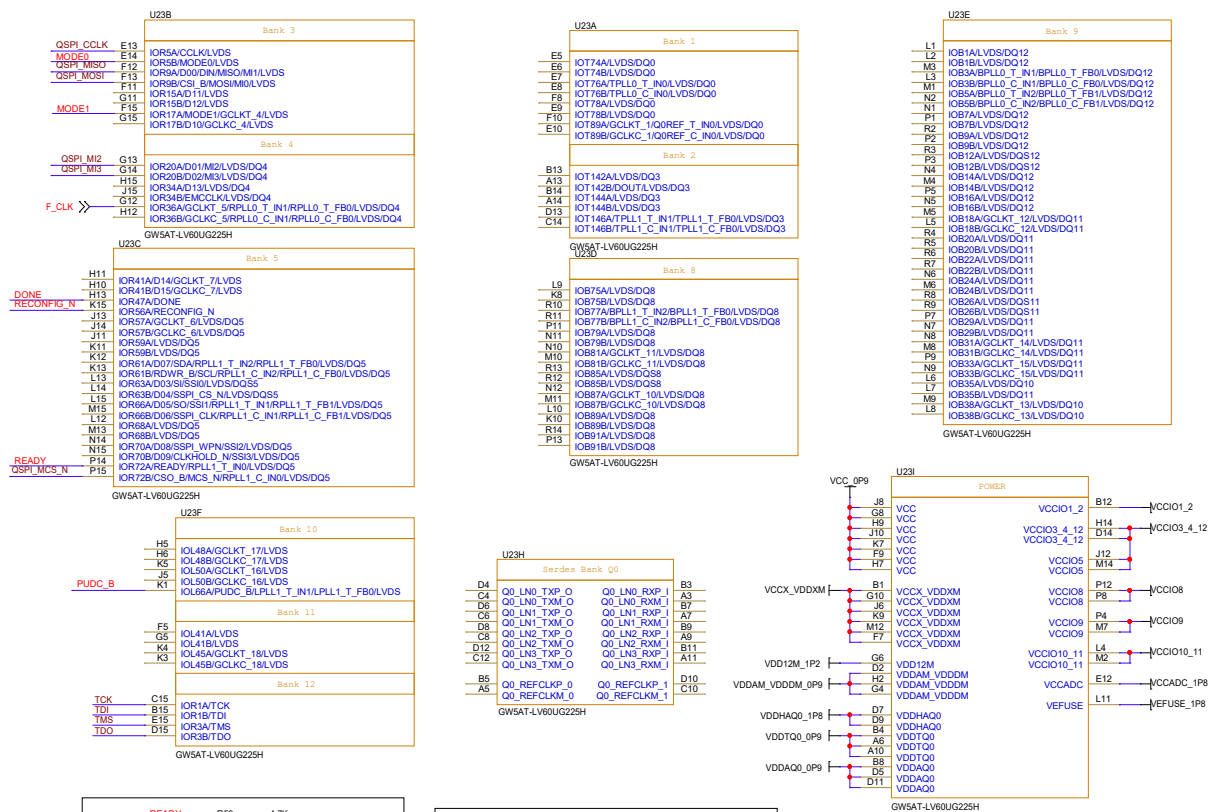
GW5AT-LV60UG225



Notes:

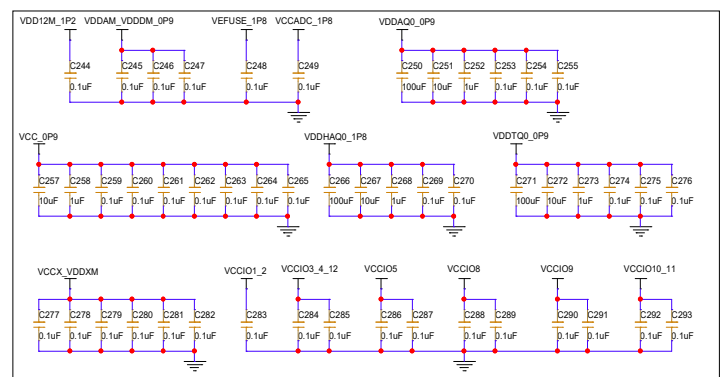
- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide .
- 6.The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

GW5AT-LV60UG225H



Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1V	3.465V
V _{CCM} ^[1]	Auxiliary voltage	1.71V	3.465V
V _{EFUSE} ^[2]	Voltage required for eFuse writing	1.62V	1.98V
Gigabit Transceiver			
V _{DHIOA} ⁺	Analog high power supply voltage	1.71V	1.89V
V _{DIOA} ⁺	Analog core power supply voltage	0.87V	1.03V
V _{DIO} ⁺	TX power supply voltage	0.87V	1.03V
V _{DIOA} ⁺	Digital power supply voltage	0.87V	1.03V
MIPI			
V _{CCDM}	Analog core power supply voltage	0.87V	1.08V
V _{CCDM}	Analog auxiliary power supply voltage	1.71V	3.465V
V _{CCDM}	Digital power supply voltage	0.87V	1.08V
V _{CCDM}	MIPI LP power supply voltage	1.14V	1.32V
ADC			
V _{CCADC}	ADC power supply voltage	1.62V	1.98V
V _{REFN}	ADC reference voltage	0V	0V
V _{REFP}	ADC reference voltage	0V	1.25V

[2] When V_{FUSE} is not required, this power supply can be connected to either GND or floating.

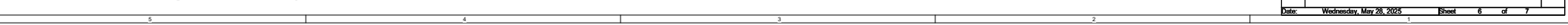
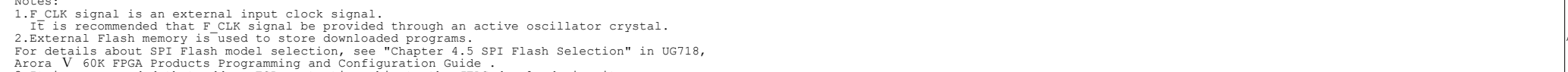
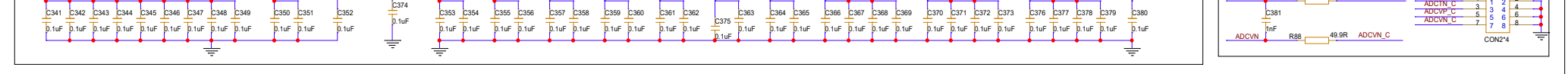
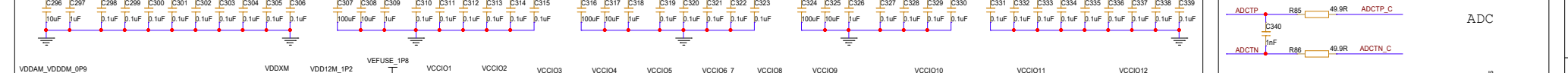
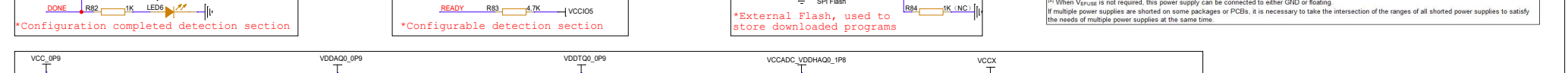
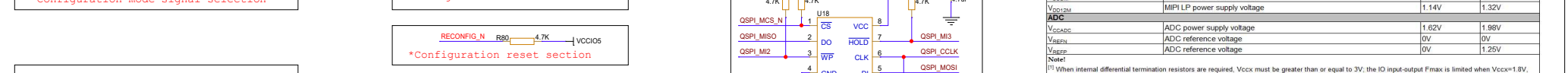
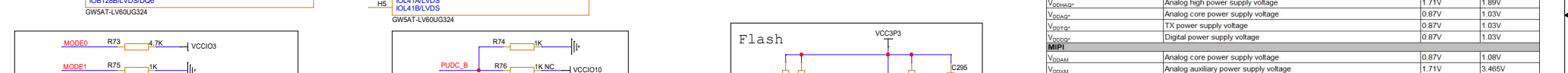
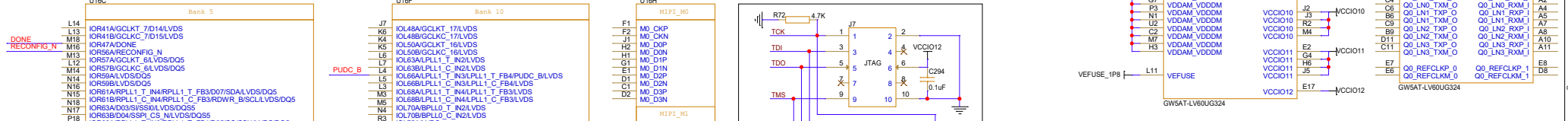
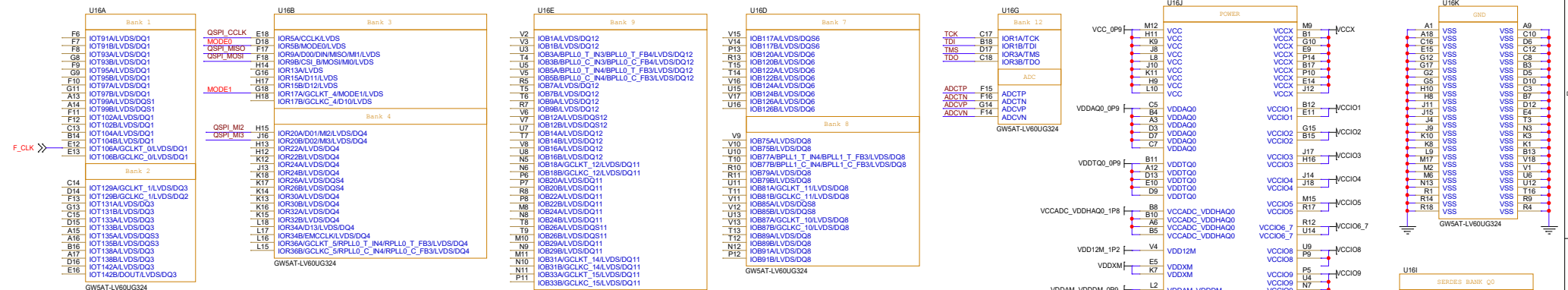


Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

Title			
GOWIN Minimum System Diagram			
Size C	Document Number GWSAT-LV60UG225H		Rev 1.5
Date:	Wednesday, May 28, 2025	Sheet	5 of 7

GW5AT-LV60UG324

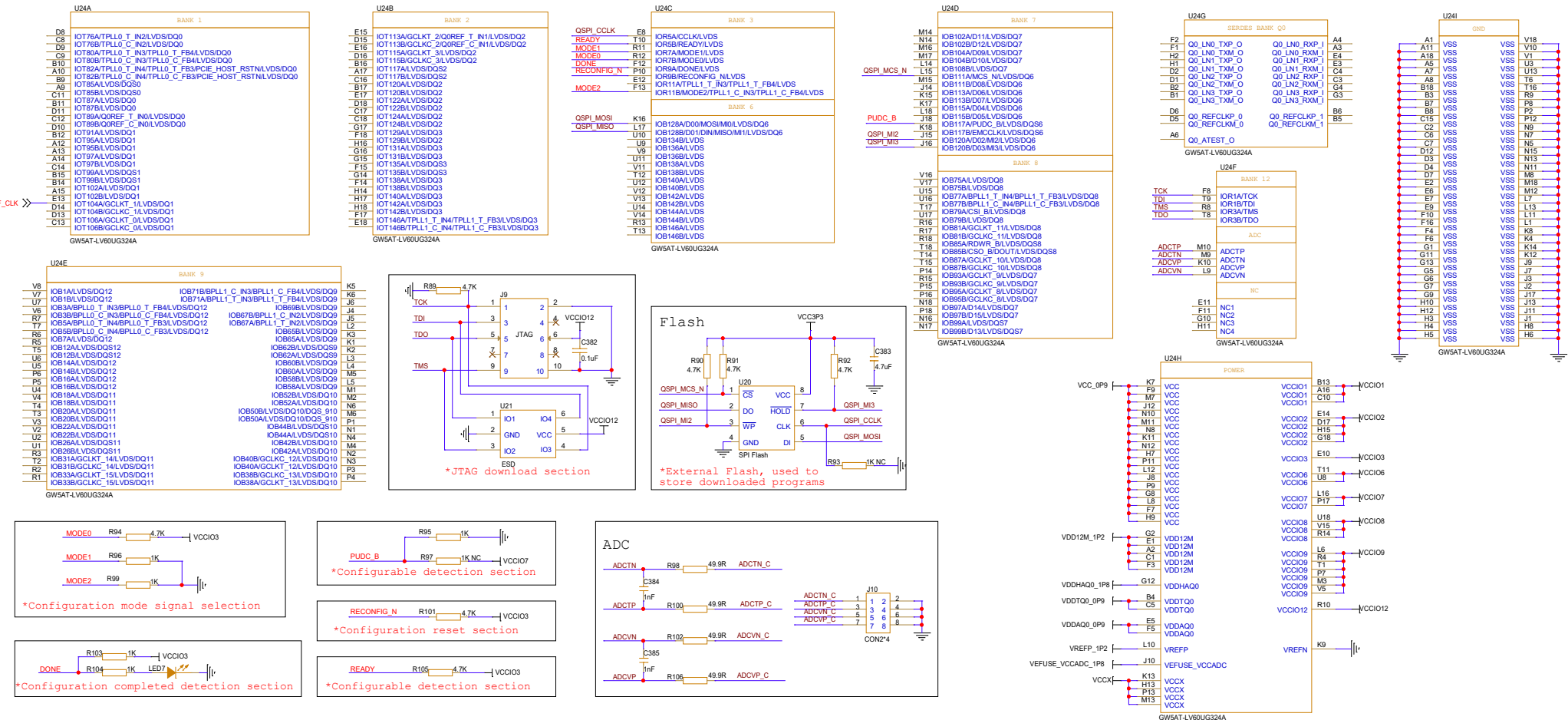


Notes:

- 1.F CLK signal is an external input clock signal.
- 1.F is recommended that F.CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
- For details about SPI Flash selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.
- If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

Title			GOWIN Minimum System Diagram
Size			Document Number
C			GW5AT-LV60UG324
Date			Wednesday, May 28, 2025
Sheet			6 of 7
Rev			1.5

GW5AT-LV60UG324A



Notes:

- 1.F CLK signal is an external input clock signal.
- It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.
- If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
V _{CCIO}	Core voltage, EV	1.14V	1.8V
V _{CCIO1}	I/O Bank voltage	1V	3.465V
V _{CCIO11}	Auxiliary voltage	1.71V	3.465V
V _{REFUSE} [2]	Voltage required for eFUSE writing	1.62V	1.98V
Gigabit Transceiver			
V _{DDHADR}	Analog high power supply voltage	1.71V	1.89V
V _{DDADR}	Analog core power supply voltage	0.87V	1.03V
V _{DDTQ}	TX power supply voltage	0.87V	1.03V
V _{DDQ}	Digital power supply voltage	0.87V	1.03V
MIPI			
V _{DDMI}	Analog core power supply voltage	0.87V	1.06V
V _{DDMI}	Analog auxiliary power supply voltage	1.71V	3.465V
V _{DDMI}	Digital power supply voltage	0.87V	1.06V
V _{CC12M}	MIPI LP power supply voltage	1.14V	1.32V
ADC			
V _{CCADC}	ADC power supply voltage	1.62V	1.98V
V _{REFN}	ADC reference voltage	0V	0V
V _{REFP}	ADC reference voltage	0V	1.25V
Note:			
[1] When internal differential termination resistors are required, V _{CC} must be greater than or equal to 3V; the I/O input-output Fmax is limited when V _{CC} >1.8V, and V _{CC} needs to be greater than or equal to 2.5V for input-output applications with Fmax greater than 600Mbps.			
[2] When V _{REFUSE} is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			