GW1N-LV1CS30

U1

IO Bank 0

Pin	Signal
B4	IOT2B/MODE0/BANK0

MODE0

IO Bank 1

Pin	Signal
A3	IOR2A/BANK1
B3	IOR2B/BANK1
A4	IOR4A/RPLL_T_FB/BANK1
B1	IOR5A/GCLKT_2/RPLL_T_IN/BANK1
B2	IOR5B/GCLKC_2/RPLL_C_IN/BANK1
E2	IOR6F/SI/D2/BANK1
D1	IOR6G/SO/D1/BANK1
D2	IOR6H/SSPI_CS_N/D0/BANK1
C1	IOR7A/GCLKT_3/BANK1
C2	IOR7B/GCLKC_3/BANK1

IO Bank 2

Pin	Signal
D3	IOB11A/GCLKT_4/BANK2
E3	IOB11B/GCLKC_4/BANK2

F_CLK

IO Bank 3

Pin	Signal
E4	IOL10A/BANK3
D4	IOL10B/BANK3
C6	IOL5A/GCLKT_7/BANK3
C5	IOL5B/GCLKC_7/BANK3
C4	IOL6A/TMS/BANK3
A5	IOL6B/TCK/BANK3
C3	IOL6C/SCLK/BANK3
B5	IOL6D/TDI/BANK3
B6	IOL6E/TDO/BANK3
D6	IOL7A/GCLKT_6/BANK3
D5	IOL7B/GCLKC_6/BANK3

TMS
TCK
TDI
TDO

Power/Gnd

Pin	Signal
E6	VCC
A6	VCCO0/VCCO3
A1	VCCO1/VCCO2
E1	VCCO1/VCCO2
E5	VSS
A2	VSS

VCC1P2
VCCO0/VCCO3
VCCO1/VCCO2
VCCO1/VCCO2

GW1N-LV1CS30

R1 1K MODE0

*Configuration mode signal selection

R2 4.7K

J1

TCK 1 / 1
TDI 3 / 3
TDO 5 / 5
7 / 7
TMS 9 / 9
2 / 2
4 / 4 VCCO0/VCCO3
6 / 6
8 / 8
10 / 10

JTAG

C1 0.1uF

R3 4.7K

VCCO0/VCCO3

U2

1	IO1	IO4	6	VCCO0/VCCO3
2	GND	VCC	5	
3	IO2	IO3	4	

ESD

*JTAG download section

VCC FB1

VCC1P2
VCCO1/VCCO2
VCCO0/VCCO3

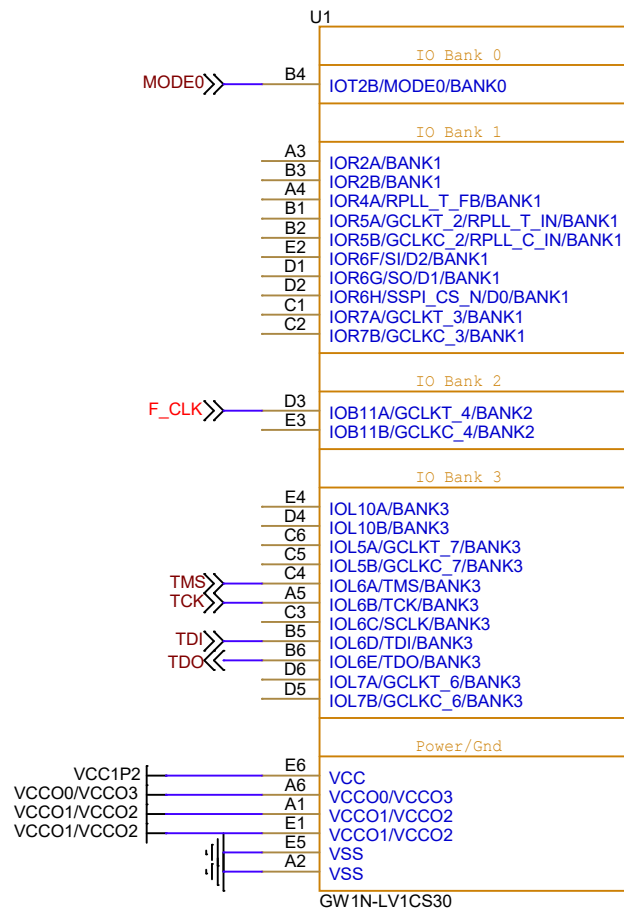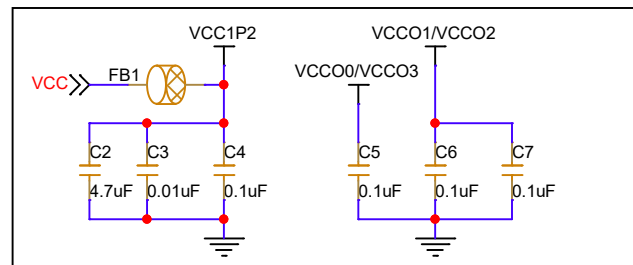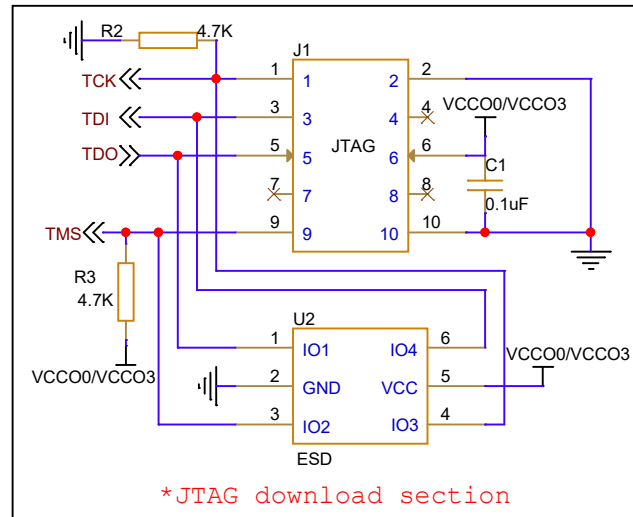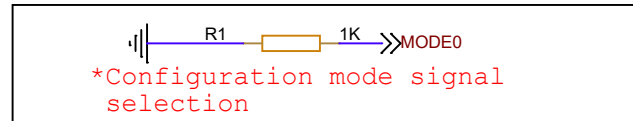| C2	C3	C4	C5	C6	C7
4.7uF	0.01uF	0.1uF	0.1uF	0.1uF	0.1uF

Notes:
1.F_CLK signal is an external input clock signal.
  It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

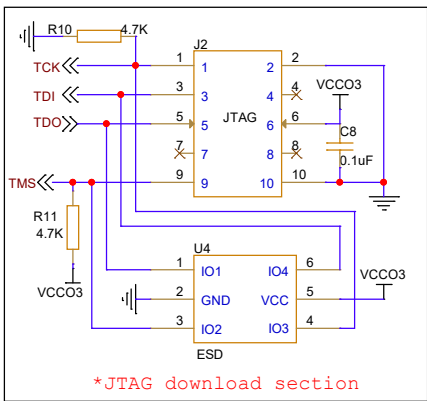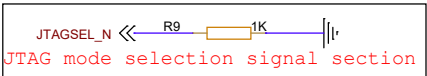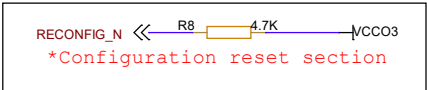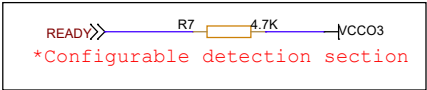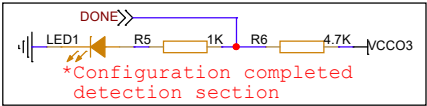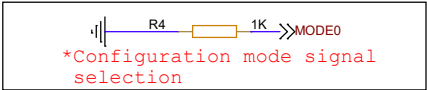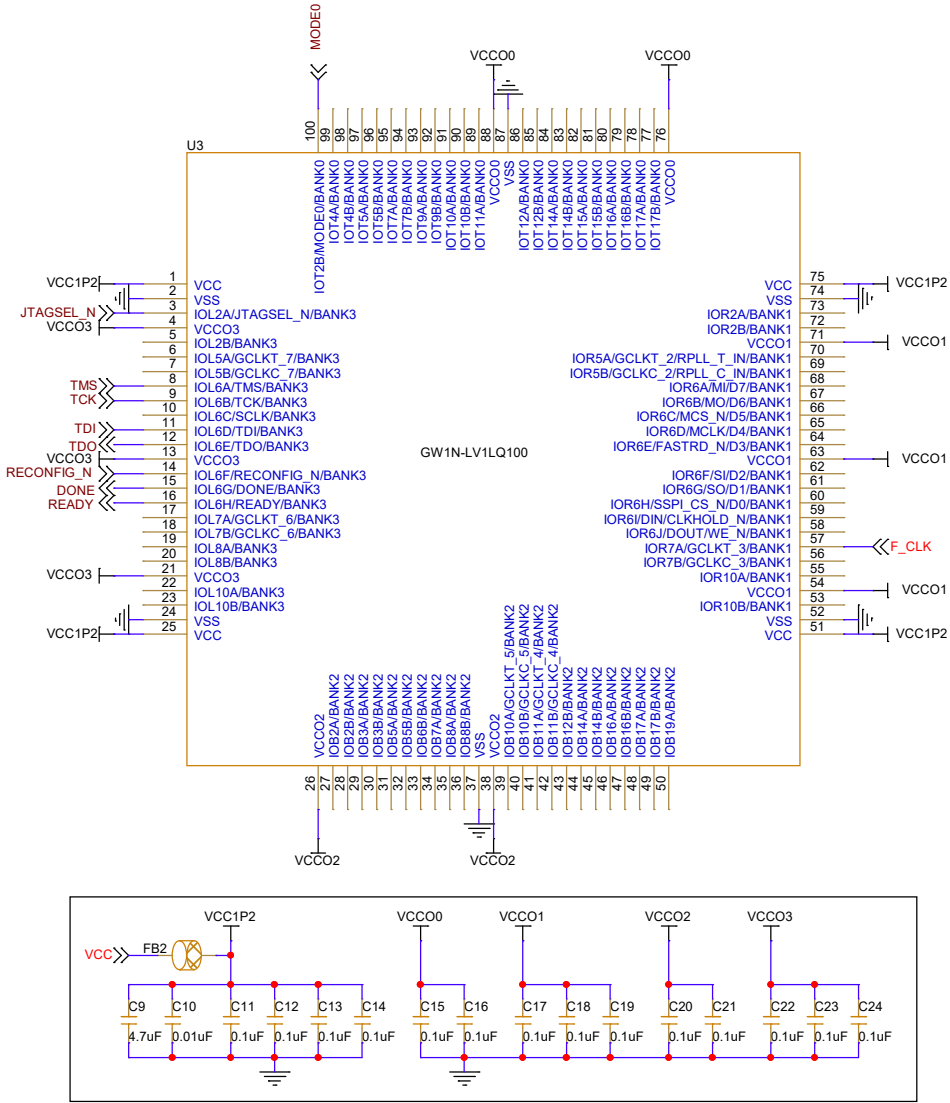| Title	GOWIN Minimum System Diagram		
Size A4	Document Number GW1N-LV1CS30		Rev 2.1
Date:	Wednesday, April 10, 2024	Sheet	1 of 5

GW1N-LV1LQ100

U3 — GW1N-LV1LQ100

MODE0

VCCO0   VCCO0

Top pins (100–76):
IOT2B/MODE0/BANK0 (100), IOT4A/BANK0 (99), IOT4B/BANK0 (98), IOT5A/BANK0 (97), IOT5B/BANK0 (96), IOT6A/BANK0 (95), IOT6B/BANK0 (94), IOT7A/BANK0 (93), IOT7B/BANK0 (92), IOT9A/BANK0 (91), IOT9B/BANK0 (90), IOT10A/BANK0 (89), IOT10B/BANK0 (88), IOT11A/BANK0 (87), VCCO0 (86), VSS (85), IOT12A/BANK0 (84), IOT12B/BANK0 (83), IOT14A/BANK0 (82), IOT14B/BANK0 (81), IOT15A/BANK0 (80), IOT15B/BANK0 (79), IOT16A/BANK0 (78), IOT16B/BANK0 (77), IOT17A/BANK0 (76), IOT17B/BANK0, VCCO0

Left pins (1–25):
1 VCC (VCC1P2), 2 VSS, 3 IOL2A/JTAGSEL_N/BANK3 (JTAGSEL_N), 4 VCCO3, 5 IOL2B/BANK3, 6 IOL5A/GCLKT_7/BANK3, 7 IOL5B/GCLKC_7/BANK3, 8 IOL6A/TMS/BANK3 (TMS), 9 IOL6B/TCK/BANK3 (TCK), 10 IOL6C/SCLK/BANK3, 11 IOL6D/TDI/BANK3 (TDI), 12 IOL6E/TDO/BANK3 (TDO), 13 VCCO3, 14 IOL6F/RECONFIG_N/BANK3 (RECONFIG_N), 15 IOL6G/DONE/BANK3 (DONE), 16 IOL6H/READY/BANK3 (READY), 17 IOL7A/GCLKT_6/BANK3, 18 IOL7B/GCLKC_6/BANK3, 19 IOL8A/BANK3, 20 IOL8B/BANK3, 21 VCCO3, 22 IOL10A/BANK3, 23 IOL10B/BANK3, 24 VSS (VCC1P2), 25 VCC

Right pins (75–51):
75 VCC (VCC1P2), 74 VSS, 73 IOR2A/BANK1, 72 IOR2B/BANK1, 71 VCCO1, 70 IOR5A/GCLKT_2/RPLL_T_IN/BANK1, 69 IOR5B/GCLKC_2/RPLL_C_IN/BANK1, 68 IOR6A/MI/D7/BANK1, 67 IOR6B/MO/D6/BANK1, 66 IOR6C/MCS_N/D5/BANK1, 65 IOR6D/MCLK/D4/BANK1, 64 IOR6E/FASTRD_N/D3/BANK1, 63 VCCO1, 62 IOR6F/SI/D2/BANK1, 61 IOR6G/SO/D1/BANK1, 60 IOR6H/SSPI_CS_N/D0/BANK1, 59 IOR6I/DIN/CLKHOLD_N/BANK1, 58 IOR6J/DOUT/WE_N/BANK1, 57 IOR7A/GCLKT_3/BANK1 (F_CLK), 56 IOR7B/GCLKC_3/BANK1, 55 IOR10A/BANK1, 54 VCCO1, 53 IOR10B/BANK1, 52 VSS, 51 VCC (VCC1P2)

Bottom pins (26–50):
VCCO2, IOB2A/BANK2 (26), IOB2B/BANK2 (27), IOB3A/BANK2 (28), IOB3B/BANK2 (29), IOB5A/BANK2 (30), IOB5B/BANK2 (31), IOB6A/BANK2 (32), IOB6B/BANK2 (33), IOB7A/BANK2 (34), IOB7B/BANK2 (35), IOB8A/BANK2 (36), IOB8B/BANK2 (37), VSS (38), VCCO2 (39), IOB10A/GCLKT_5/BANK2 (40), IOB10B/GCLKC_5/BANK2 (41), IOB11A/GCLKT_4/BANK2 (42), IOB11B/GCLKC_4/BANK2 (43), IOB12B/BANK2 (44), IOB14A/BANK2 (45), IOB14B/BANK2 (46), IOB16A/BANK2 (47), IOB16B/BANK2 (48), IOB17A/BANK2 (49), IOB17B/BANK2 (50), IOB19A/BANK2

VCCO2   VCCO2

Configuration sections

R4 — 1K — MODE0
*Configuration mode signal selection

DONE — LED1 — R5 1K — R6 4.7K — VCCO3
*Configuration completed detection section

READY — R7 4.7K — VCCO3
*Configurable detection section

RECONFIG_N — R8 4.7K — VCCO3
*Configuration reset section

JTAGSEL_N — R9 1K
JTAG mode selection signal section

JTAG download section

R10 4.7K
J2 — JTAG
TCK (1), TDI (3), TDO (5)
(7), (9)
TMS
R11 4.7K
VCCO3

Pins: 1,3,5,7,9 / 2,4,6,8,10
VCCO3   C8 0.1uF

U4 — ESD
1 IO1 — 6 IO4
2 GND — 5 VCC — VCCO3
3 IO2 — 4 IO3
VCCO3

*JTAG download section

Power decoupling

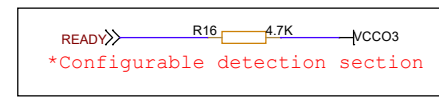VCC — FB2 — VCC1P2   VCCO0   VCCO1   VCCO2   VCCO3

C9 4.7uF, C10 0.01uF, C11 0.1uF, C12 0.1uF, C13 0.1uF, C14 0.1uF, C15 0.1uF, C16 0.1uF, C17 0.1uF, C18 0.1uF, C19 0.1uF, C20 0.1uF, C21 0.1uF, C22 0.1uF, C23 0.1uF, C24 0.1uF

Notes:
1. F_CLK signal is an external input clock signal.
   It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

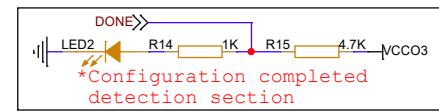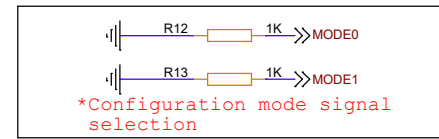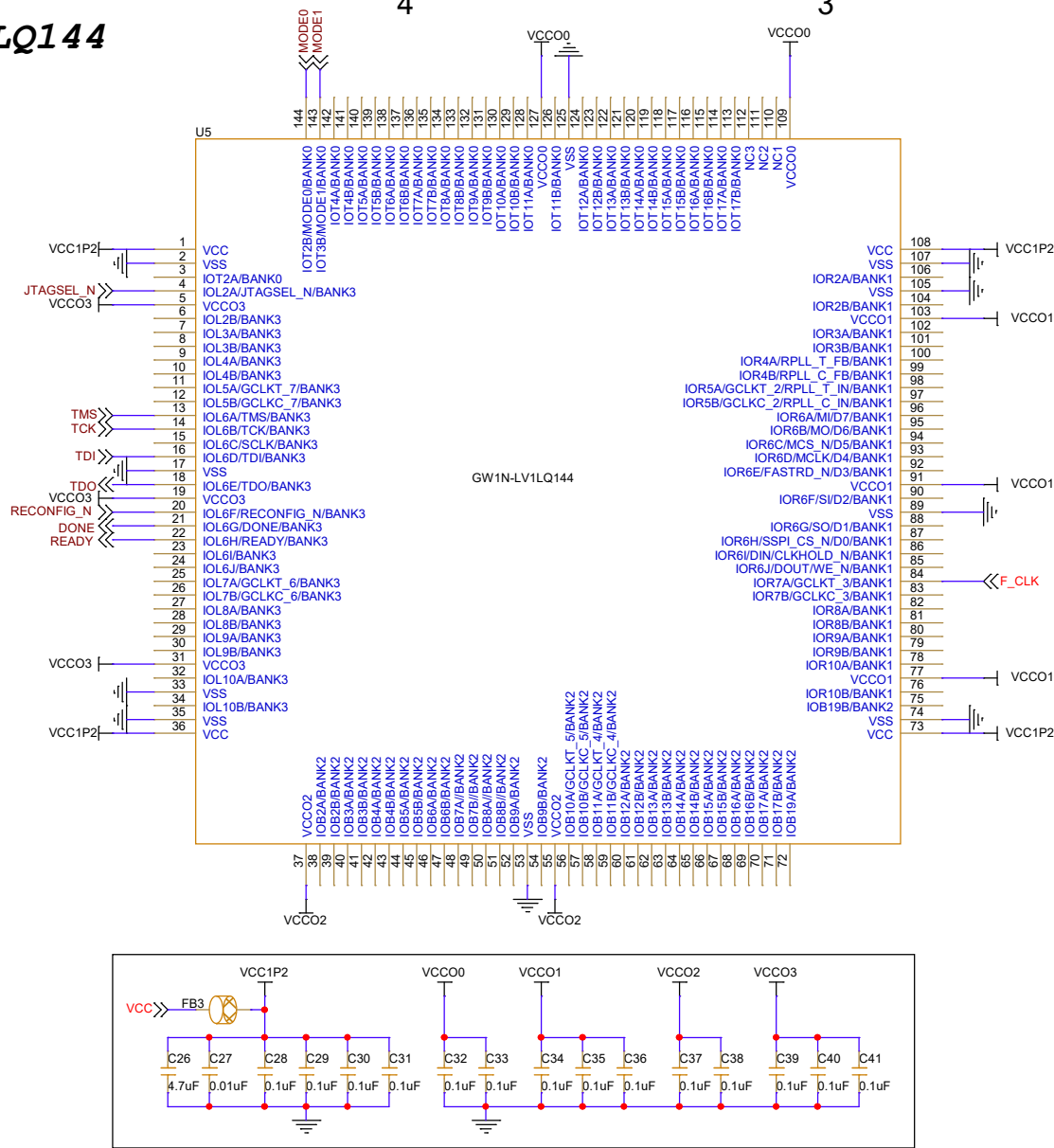| Title	GOWIN Minimum System Diagram	
Size B	Document Number GW1N-LV1LQ100	Rev 2.1
Date: Monday, April 08, 2024	Sheet 2 of 5	

GW1N-LV1LQ144

MODE0
MODE1

VCCO0   VCCO0

U5

Left side pins (1-36):
- 1 VCC — VCC1P2
- 2 VSS
- 3 IOT2A/BANK0
- 4 IOL2A/JTAGSEL_N/BANK3 — JTAGSEL_N
- 5 VCCO3
- 6 VCCO3
- 7 IOL2B/BANK3
- 8 IOL3A/BANK3
- 9 IOL3B/BANK3
- 10 IOL4A/BANK3
- 11 IOL4B/BANK3
- 12 IOL5A/GCLKT_7/BANK3
- 13 IOL5B/GCLKC_7/BANK3
- 14 IOL6A/TMS/BANK3 — TMS
- 15 IOL6B/TCK/BANK3 — TCK
- 16 IOL6C/SCLK/BANK3
- 17 IOL6D/TDI/BANK3 — TDI
- 18 VSS
- 19 IOL6E/TDO/BANK3 — TDO
- 20 VCCO3 — VCCO3
- 21 IOL6F/RECONFIG_N/BANK3 — RECONFIG_N
- 22 IOL6G/DONE/BANK3 — DONE
- 23 IOL6H/READY/BANK3 — READY
- 24 IOL6I/BANK3
- 25 IOL6J/BANK3
- 26 IOL7A/GCLKT_6/BANK3
- 27 IOL7B/GCLKC_6/BANK3
- 28 IOL8A/BANK3
- 29 IOL8B/BANK3
- 30 IOL9A/BANK3
- 31 IOL9B/BANK3
- 32 VCCO3 — VCCO3
- 33 IOL10A/BANK3
- 34 VSS
- 35 IOL10B/BANK3
- 36 VSS — VCC1P2
- VCC

Right side pins (73-108):
- 108 VCC — VCC1P2
- 107 VSS
- 106 IOR2A/BANK1
- 105 VSS
- 104 IOR2B/BANK1
- 103 IOR3A/BANK1 — VCCO1
- 102 VCCO1
- 101 IOR3A/BANK1
- 100 IOR3B/BANK1
- 99 IOR4A/RPLL_T_FB/BANK1
- 98 IOR4B/RPLL_C_FB/BANK1
- 97 IOR5A/GCLKT_2/RPLL_T_IN/BANK1
- 96 IOR5B/GCLKC_2/RPLL_C_IN/BANK1
- 95 IOR6A/MI/D7/BANK1
- 94 IOR6B/MO/D6/BANK1
- 93 IOR6C/MCS_N/D5/BANK1
- 92 IOR6D/MCLK/D4/BANK1
- 91 IOR6E/FASTRD_N/D3/BANK1 — VCCO1
- 90 VCCO1
- 89 IOR6F/SI/D2/BANK1
- 88 VSS
- 87 IOR6G/SO/D1/BANK1
- 86 IOR6H/SSPI_CS_N/D0/BANK1
- 85 IOR6I/DIN/CLKHOLD_N/BANK1
- 84 IOR6J/DOUT/WE_N/BANK1
- 83 IOR7A/GCLKT_3/BANK1 — F_CLK
- 82 IOR7B/GCLKC_3/BANK1
- 81 IOR8A/BANK1
- 80 IOR8B/BANK1
- 79 IOR9A/BANK1
- 78 IOR9B/BANK1
- 77 IOR10A/BANK1 — VCCO1
- 76 VCCO1
- 75 IOR10B/BANK1
- 74 IOB19B/BANK2
- 73 VSS — VCC1P2
- VCC

GW1N-LV1LQ144

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*Configuration mode signal selection
- R12 1K MODE0
- R13 1K MODE1

*Configuration completed detection section
- LED2 R14 1K R15 4.7K VCCO3
- DONE

*Configurable detection section
- READY R16 4.7K VCCO3

*Configuration reset section
- RECONFIG_N R17 4.7K VCCO3

JTAG mode selection signal section
- JTAGSEL_N R18 1K

*JTAG download section
- R19 4.7K
- J3 JTAG
- TCK 1 2
- TDI 3 4 VCCO3
- TDO 5 6
- 7 8 C25 0.1uF
- TMS 9 10
- R20 4.7K
- VCCO3
- U6 ESD
  - 1 IO1   6 IO4 VCCO3
  - 2 GND   5 VCC
  - 3 IO2   4 IO3

Bottom decoupling section:
- VCC FB3 VCC1P2
- C26 4.7uF C27 0.01uF C28 0.1uF C29 0.1uF C30 0.1uF C31 0.1uF
- VCCO0: C32 0.1uF C33 0.1uF
- VCCO1: C34 0.1uF C35 0.1uF C36 0.1uF
- VCCO2: C37 0.1uF C38 0.1uF
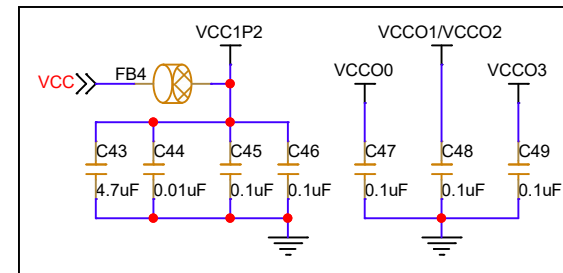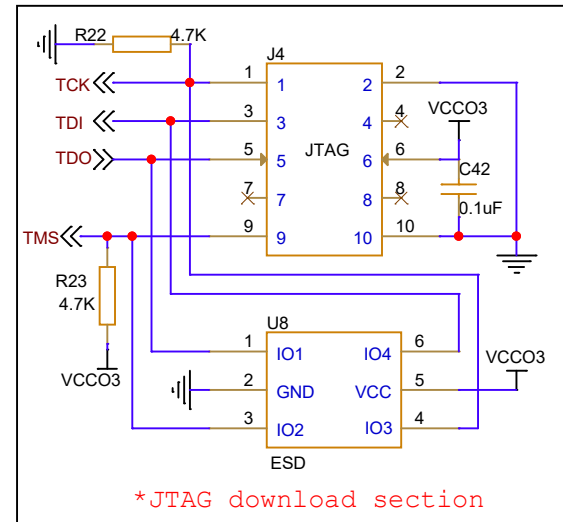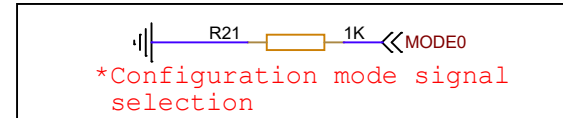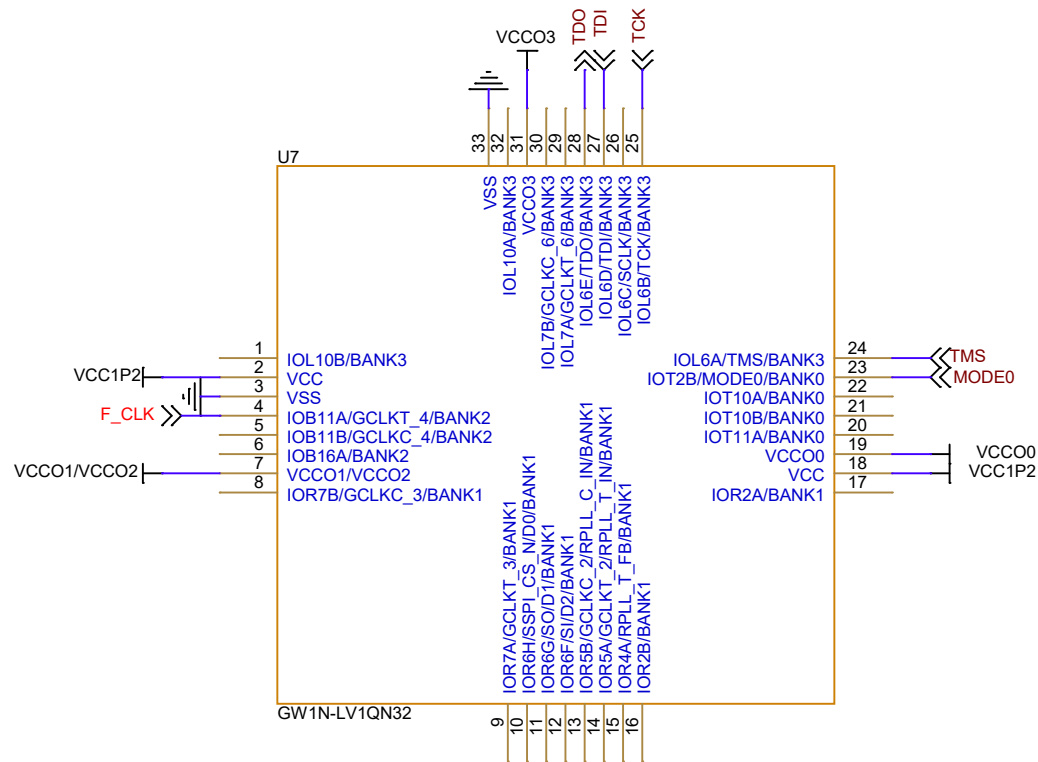- VCCO3: C39 0.1uF C40 0.1uF C41 0.1uF

VCCO2   VCCO2

Notes:
1. F_CLK signal is an external input clock signal.
   It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

GW1N-LV1QN32

U7 — GW1N-LV1QN32

Top pins:
- 33 VSS/BANK3
- 32 VCCO3
- 31 IOL10A/BANK3
- 30 IOL7B/GCLKC_6/BANK3
- 29 IOL7A/GCLKT_6/BANK3
- 28 IOL6E/TDO/BANK3
- 27 IOL6D/TDI/BANK3
- 26 IOL6C/SCLK/BANK3
- 25 IOL6B/TCK/BANK3

VCCO3, TDO, TDI, TCK

Left pins:
- 1 IOL10B/BANK3
- 2 VCC — VCC1P2
- 3 VSS
- 4 IOB11A/GCLKT_4/BANK2 — F_CLK
- 5 IOB11B/GCLKC_4/BANK2
- 6 IOB16A/BANK2
- 7 VCCO1/VCCO2 — VCCO1/VCCO2
- 8 IOR7B/GCLKC_3/BANK1

Right pins:
- 24 IOL6A/TMS/BANK3 — TMS
- 23 IOT2B/MODE0/BANK0 — MODE0
- 22 IOT10A/BANK0
- 21 IOT10B/BANK0
- 20 IOT11A/BANK0
- 19 VCCO0 — VCCO0
- 18 VCC — VCC1P2
- 17 IOR2A/BANK1

Bottom pins:
- 9 IOR7A/GCLKT_3/BANK1
- 10 IOR6H/SSPI_CS_N/D0/BANK1
- 11 IOR6G/SO/D1/BANK1
- 12 IOR6F/SI/D2/BANK1
- 13 IOR5B/GCLKC_2/RPLL_C_IN/BANK1
- 14 IOR5A/GCLKT_2/RPLL_T_IN/BANK1
- 15 IOR4A/RPLL_T_FB/BANK1
- 16 IOR2B/BANK1

*Configuration mode signal selection
R21 1K — MODE0

*JTAG download section

J4 — JTAG
- R22 4.7K — TCK — 1
- TDI — 3
- TDO — 5
- 7
- TMS — 9
- 2
- 4 VCCO3
- 6 — C42 0.1uF
- 8
- 10
- R23 4.7K
- VCCO3

U8 — ESD
- 1 IO1 — 6 IO4 — VCCO3
- 2 GND — 5 VCC
- 3 IO2 — 4 IO3
- VCCO3

Power decoupling
VCC — FB4 — VCC1P2
- C43 4.7uF
- C44 0.01uF
- C45 0.1uF
- C46 0.1uF

VCCO1/VCCO2
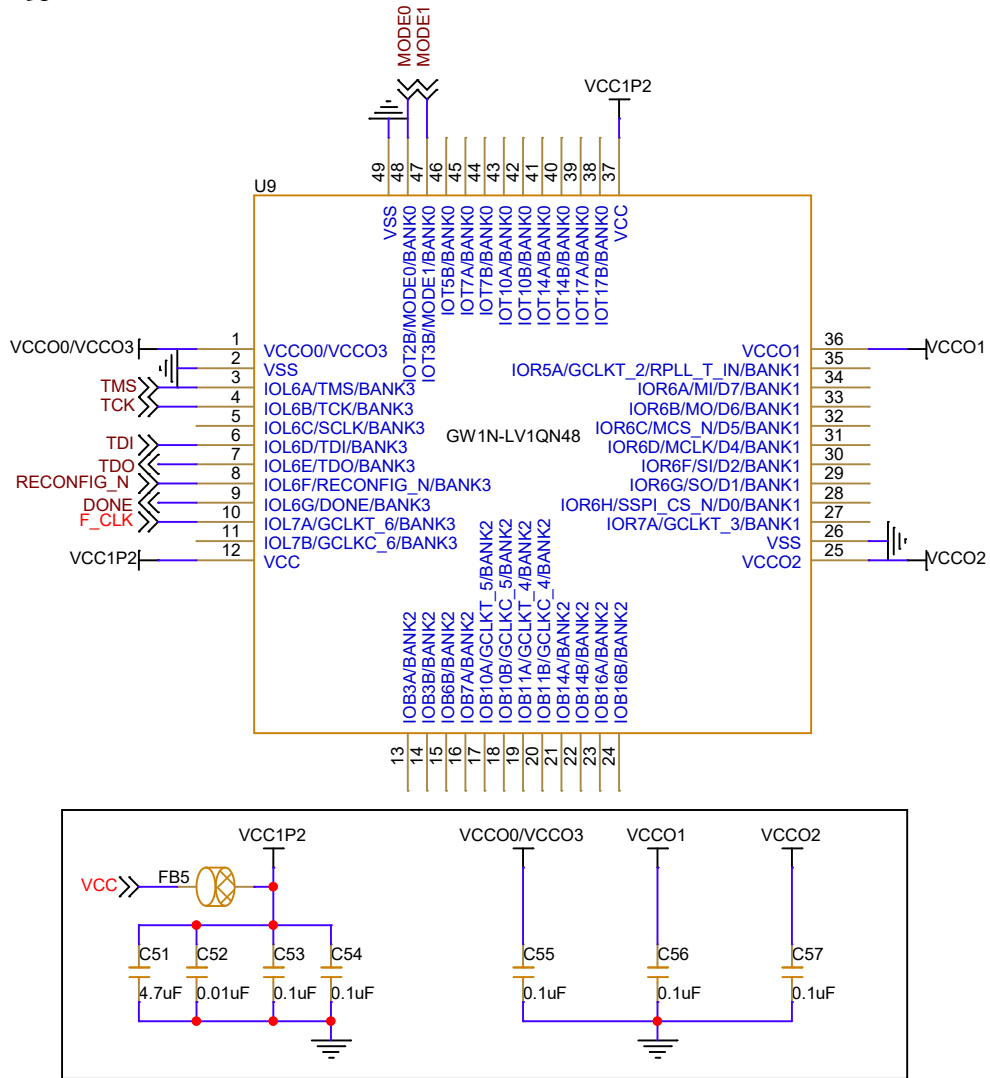- C47 0.1uF
- C48 0.1uF

VCCO0, VCCO3
- C49 0.1uF

Notes:
1. F_CLK signal is an external input clock signal.
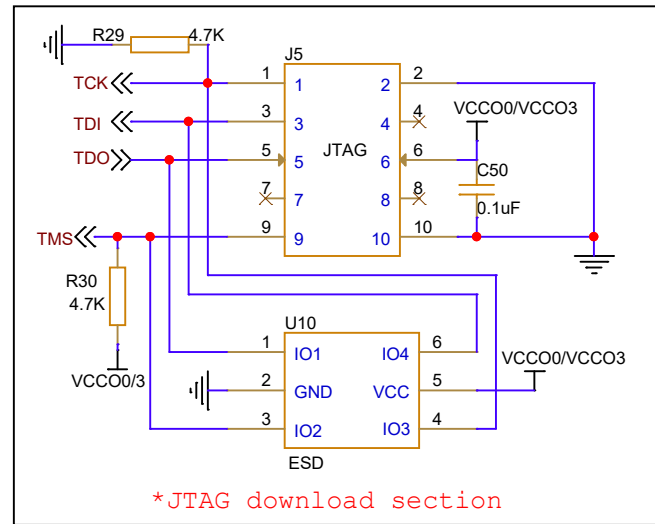   It is recommended that F_CLK signal be provided through an active oscillator crystal.
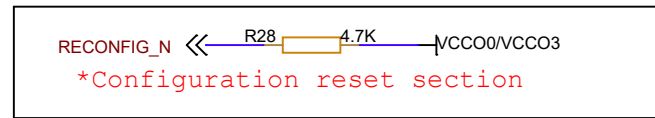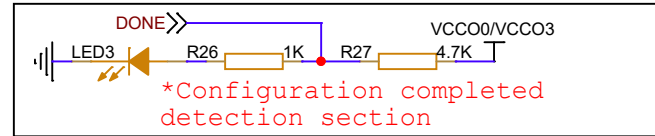2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title	GOWIN Minimum System Diagram
Size A4	Document Number GW1N-LV1QN32	Rev 2.1
Date: Monday, April 08, 2024	Sheet 4 of 5

GW1N-LV1QN48

U9 — GW1N-LV1QN48

Top pins (49, 48, 47, 46, 45, 44, 43, 42, 41, 40, 39, 38, 37):
- MODE0, MODE1
- VCC1P2
- VSS
- IOT2B/MODE0/BANK0
- IOT3B/MODE1/BANK0
- IOT5B/BANK0
- IOT7A/BANK0
- IOT7B/BANK0
- IOT10A/BANK0
- IOT10B/BANK0
- IOT14A/BANK0
- IOT14B/BANK0
- IOT17A/BANK0
- IOT17B/BANK0
- VCC

Left pins (1–12):
- 1 VCCO0/VCCO3 — VCCO0/VCCO3
- 2 VSS
- 3 IOL6A/TMS/BANK3 — TMS
- 4 IOL6B/TCK/BANK3 — TCK
- 5 IOL6C/SCLK/BANK3
- 6 IOL6D/TDI/BANK3 — TDI
- 7 IOL6E/TDO/BANK3 — TDO
- 8 IOL6F/RECONFIG_N/BANK3 — RECONFIG_N
- 9 IOL6G/DONE/BANK3 — DONE
- 10 IOL7A/GCLKT_6/BANK3 — F_CLK
- 11 IOL7B/GCLKC_6/BANK3
- 12 VCC — VCC1P2

Right pins (36–25):
- 36 VCCO1 — VCCO1
- 35 IOR5A/GCLKT_2/RPLL_T_IN/BANK1
- 34 IOR6A/MI/D7/BANK1
- 33 IOR6B/MO/D6/BANK1
- 32 IOR6C/MCS_N/D5/BANK1
- 31 IOR6D/MCLK/D4/BANK1
- 30 IOR6F/SI/D2/BANK1
- 29 IOR6G/SO/D1/BANK1
- 28 IOR6H/SSPI_CS_N/D0/BANK1
- 27 IOR7A/GCLKT_3/BANK1
- 26 VSS
- 25 VCCO2 — VCCO2

Bottom pins (13–24):
- IOB3A/BANK2
- IOB3B/BANK2
- IOB6B/BANK2
- IOB7B/BANK2
- IOB10A/GCLKT_5/BANK2
- IOB10B/GCLKC_5/BANK2
- IOB11A/GCLKT_4/BANK2
- IOB11B/GCLKC_4/BANK2
- IOB14A/BANK2
- IOB14B/BANK2
- IOB16A/BANK2
- IOB16B/BANK2

*Configuration mode signal selection

- R24 1K → MODE0
- R25 1K → MODE1

*Configuration completed detection section

- DONE
- LED3 R26 1K R27 4.7K VCCO0/VCCO3

*Configuration reset section

- RECONFIG_N R28 4.7K VCCO0/VCCO3

*JTAG download section

J5 — JTAG
- R29 4.7K
- TCK — 1
- TDI — 3
- TDO — 5
- 7
- TMS — 9
- 2
- 4 VCCO0/VCCO3
- 6
- 8 C50 0.1uF
- 10
- R30 4.7K
- VCCO0/3

U10 — ESD
- 1 IO1 — 6 IO4 — VCCO0/VCCO3
- 2 GND — 5 VCC
- 3 IO2 — 4 IO3

Power supply decoupling

- VCC — FB5 — VCC1P2
- C51 4.7uF
- C52 0.01uF
- C53 0.1uF
- C54 0.1uF
- VCCO0/VCCO3 — C55 0.1uF
- VCCO1 — C56 0.1uF
- VCCO2 — C57 0.1uF

Notes:

1. F_CLK signal is an external input clock signal.
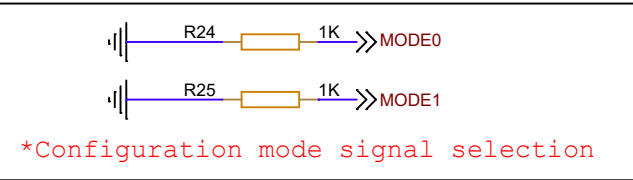   It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.