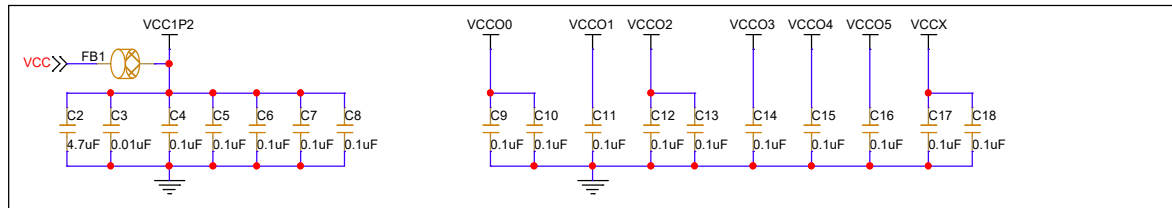
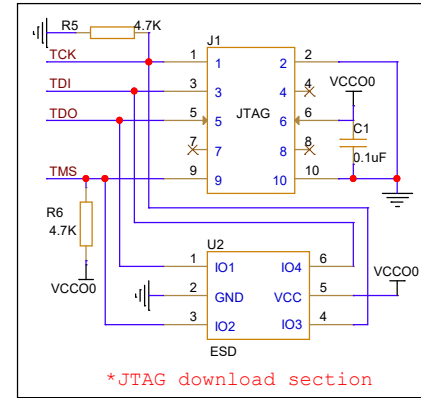
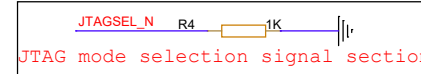
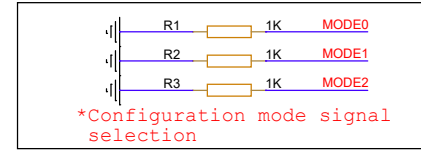
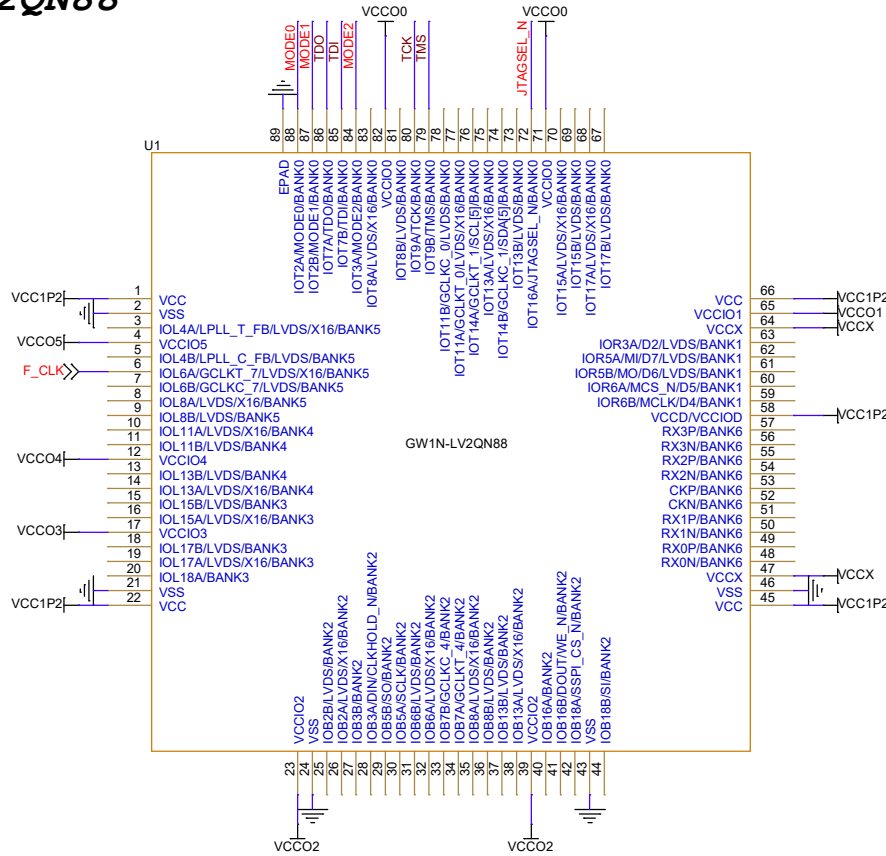


GW1N-LV2QN88

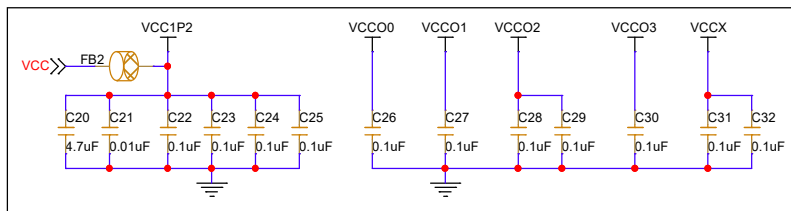
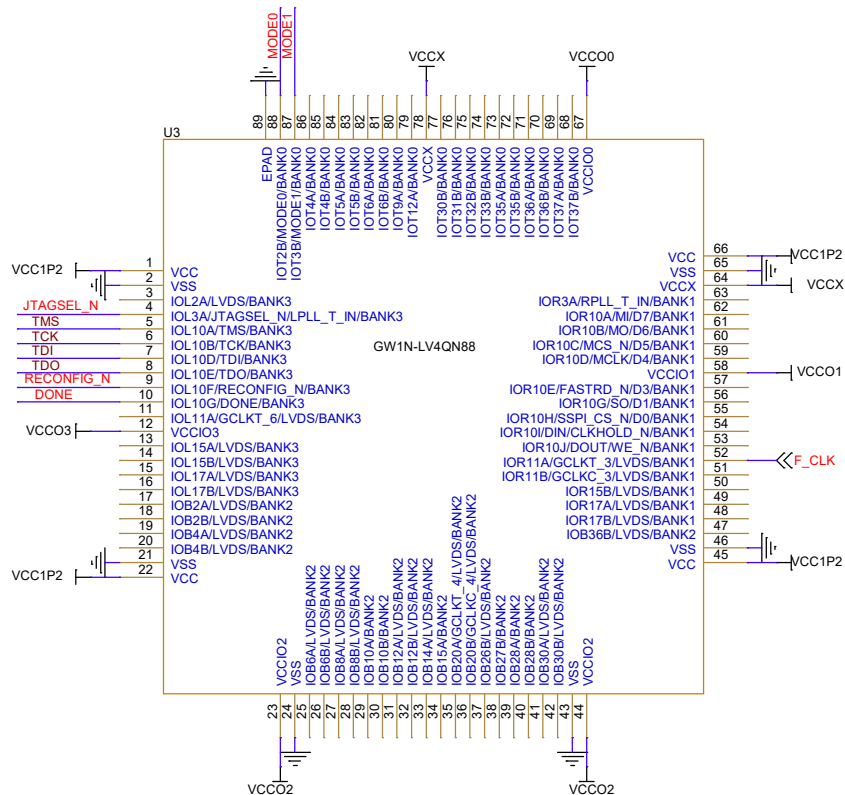


Notes:

- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

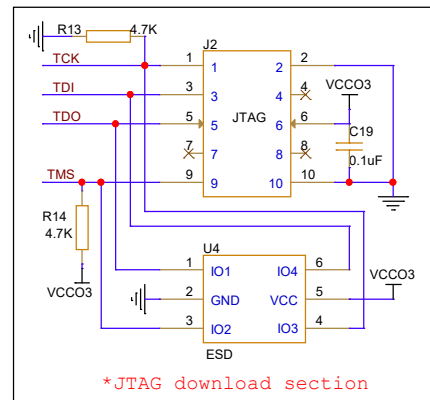
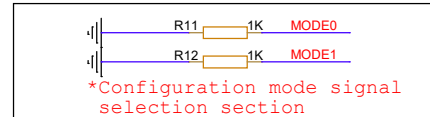
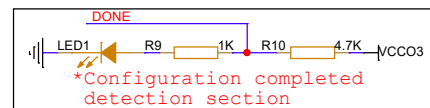
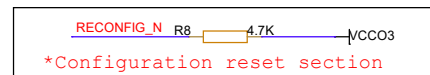
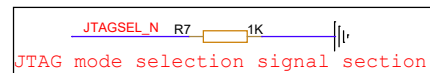
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| Title | | |
| GOWIN Minimum System Diagram | | |
| Size | Document Number | Rev |
| B | GW1N-LV2QN88 | 3.6 |
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GW1N-LV4QN88



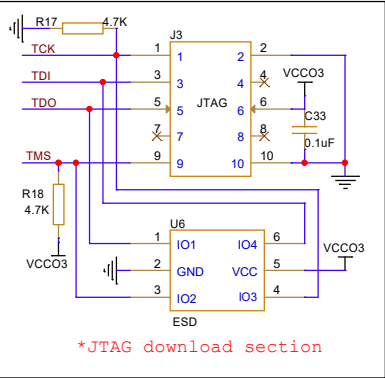
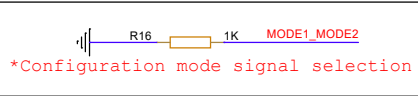
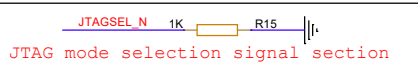
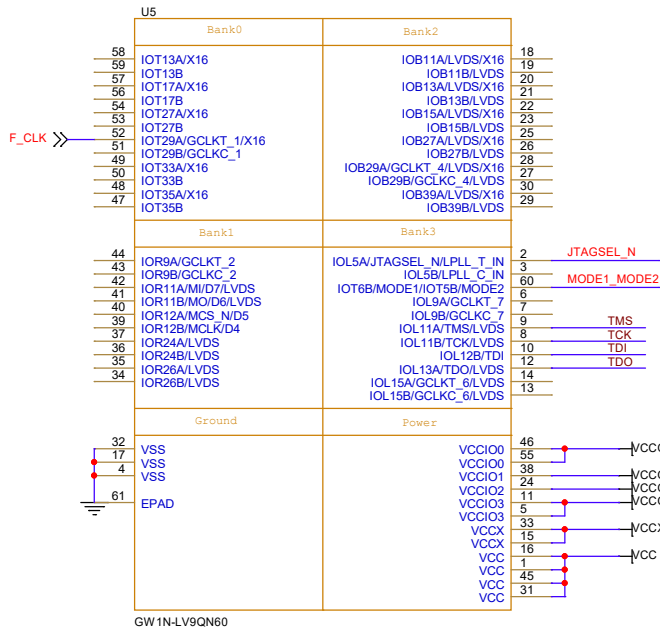
Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

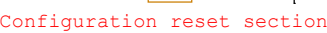
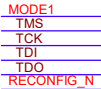


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| Gowin FPGA-AOTOMOTIVE Minimum System Diagram | | |
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| B | GW1N-LV4QN88 | 3.6 |
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GW1N-LV9QN60



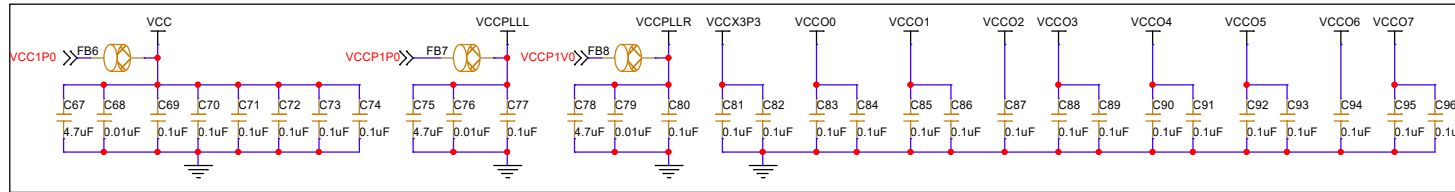
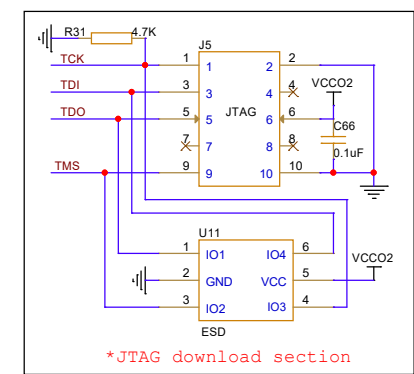
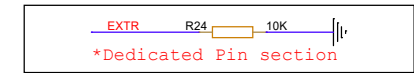
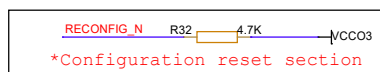
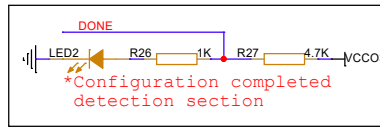
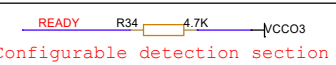
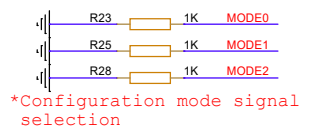
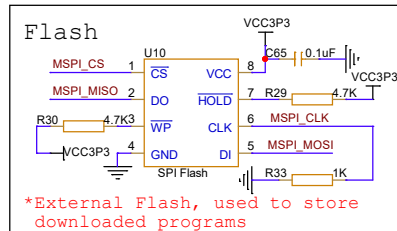
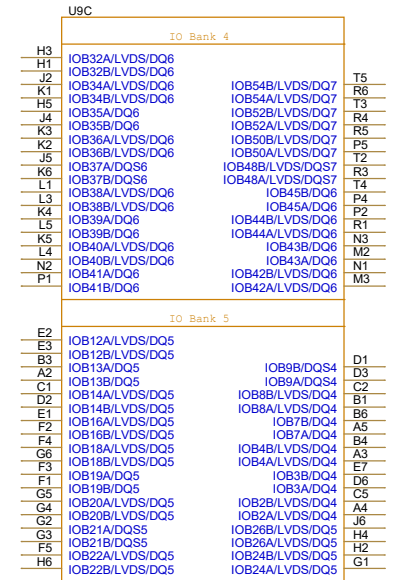
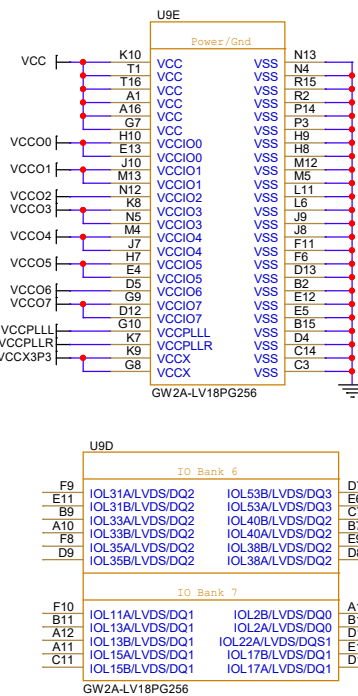
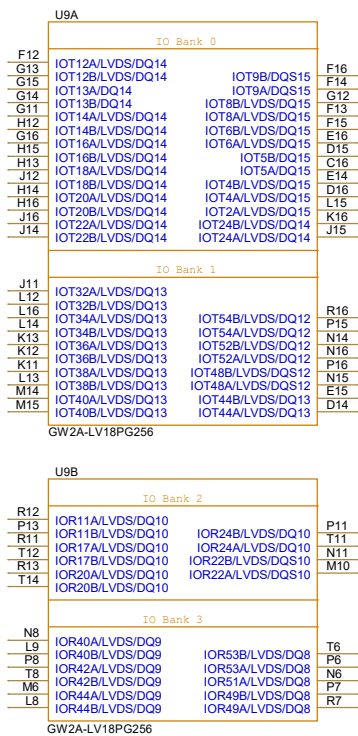
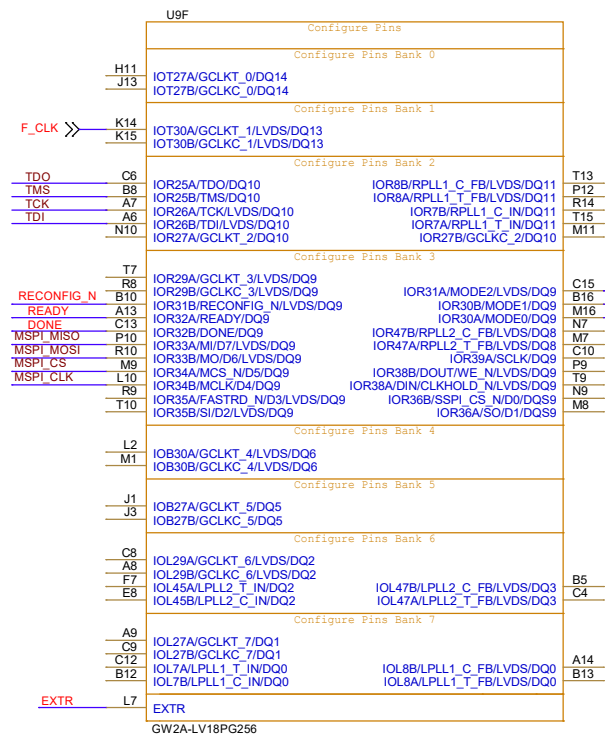
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- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

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| Title | | |
| GOWIN Minimum System Diagram | | |
| Size B | Document Number GW1N-LV9QN88F | Rev 3.6 |
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GW2A-LV18PG256

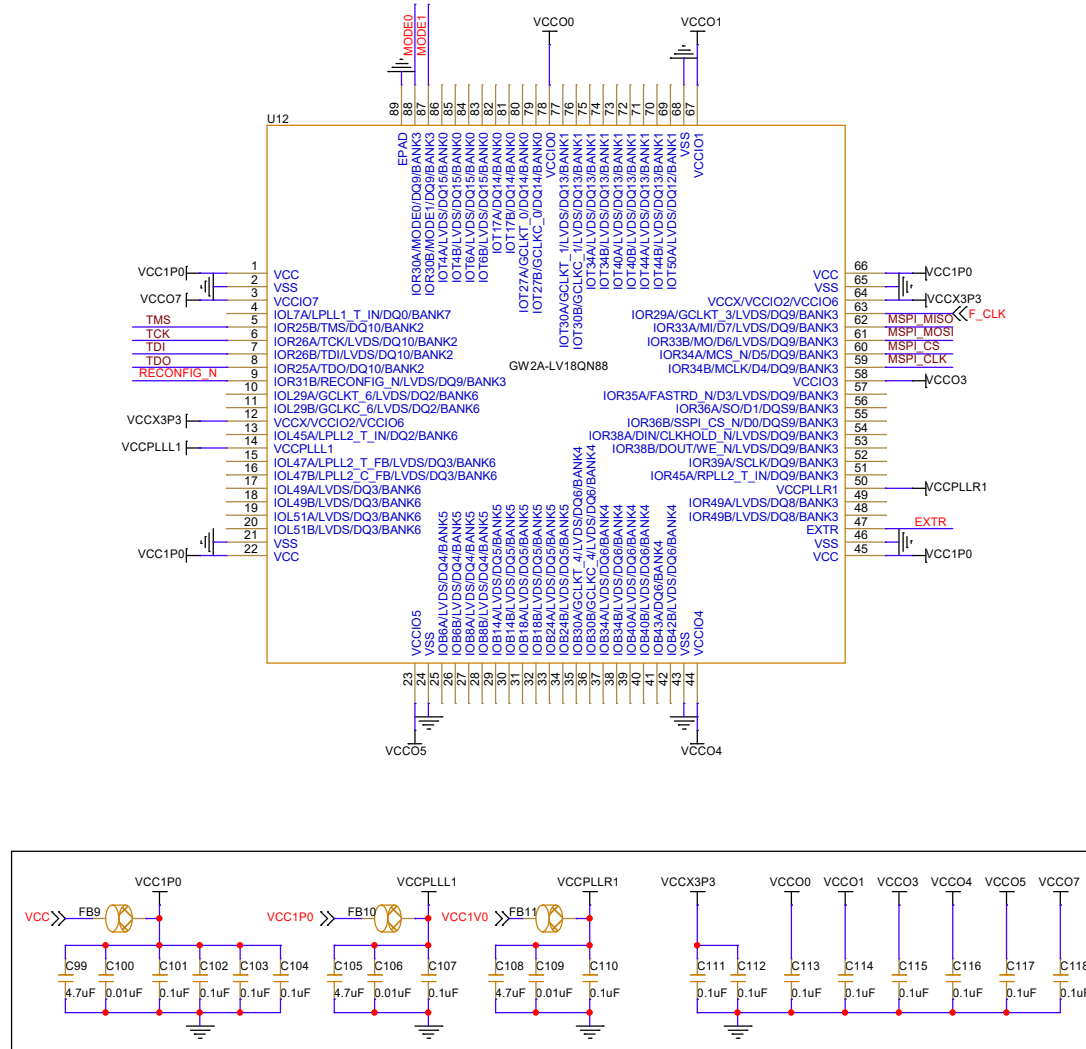


Notes:

1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage,
a level shifter is required for voltage translation.

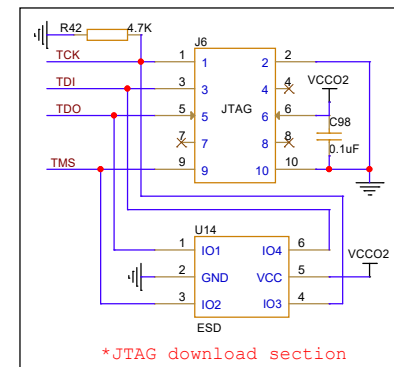
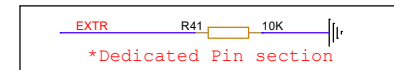
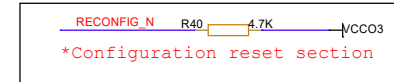
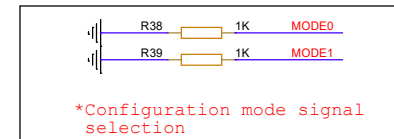
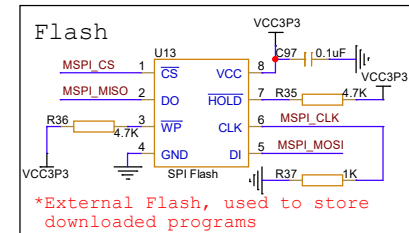
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| Size | Document Number | | Rev |
| A3 | GW2A-L V1.0PG256 | | 3.6 |
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GW2A-LV18QN88



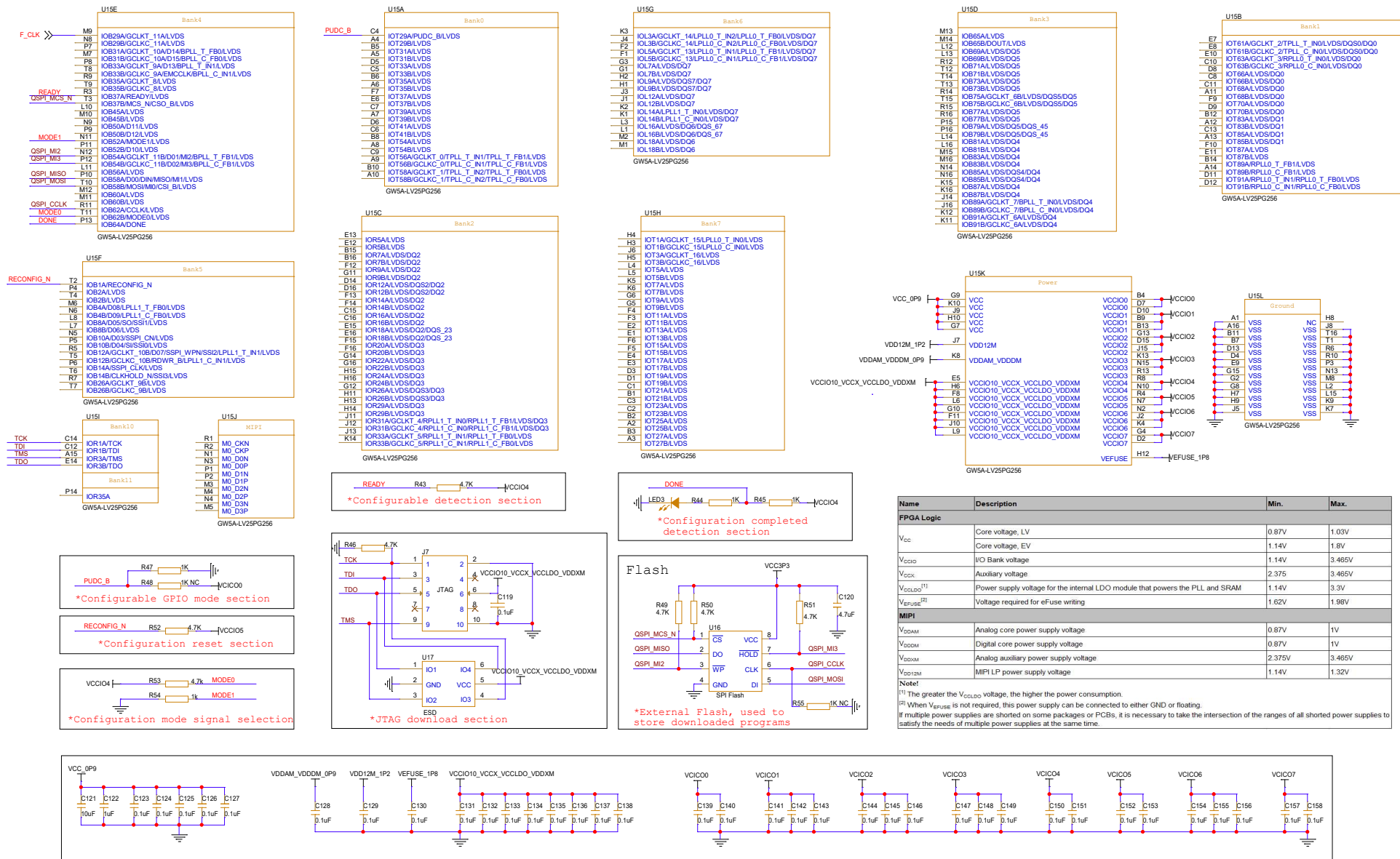
Notes:

1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage,
a level shifter is required for voltage translation



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| Gowin FPGA-AOTOMOTIVE Minimum System Diagram | | | | |
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| A3 | GW2A-LV18QN88F | | | 3.6 |
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GW5A-LV25PG256

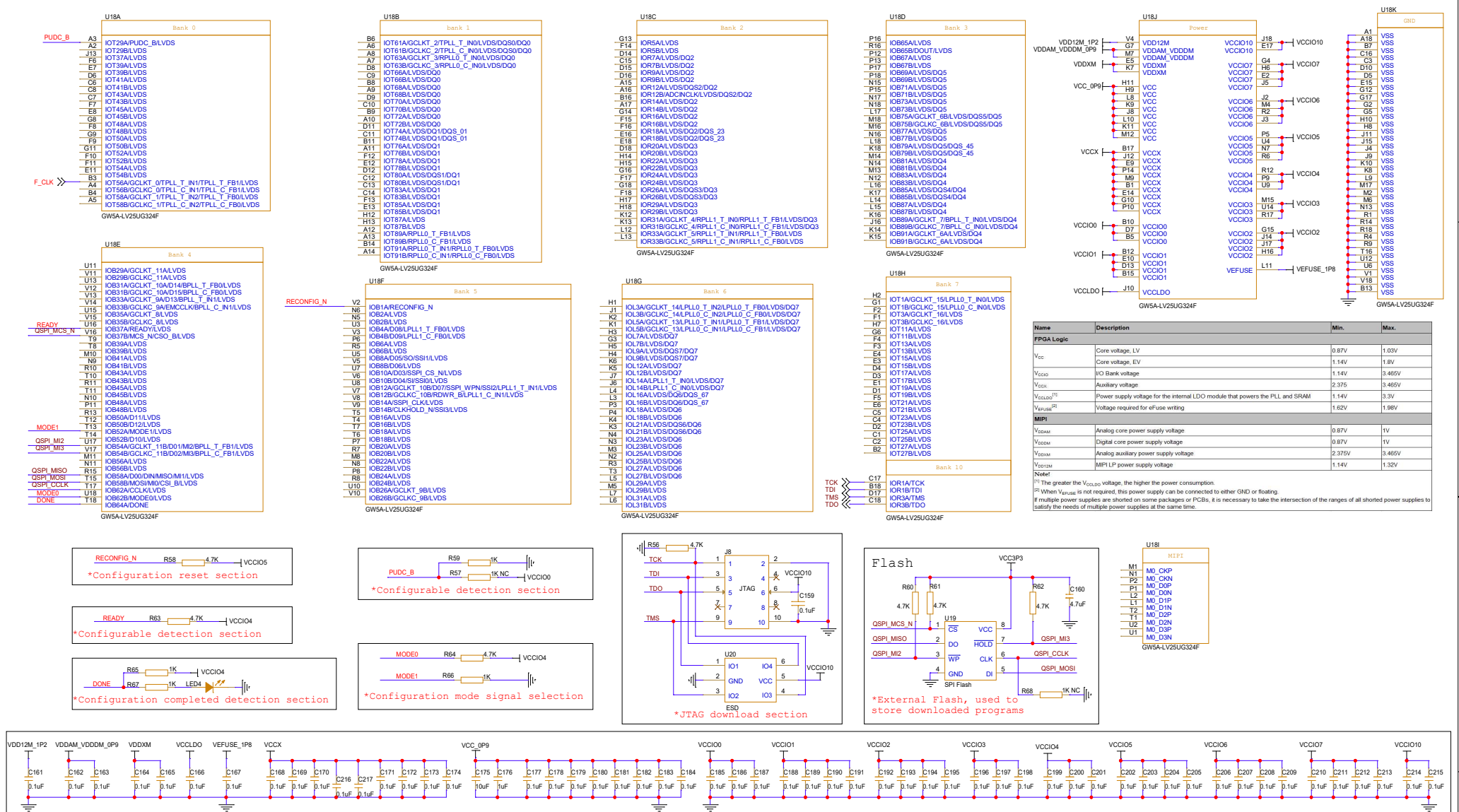


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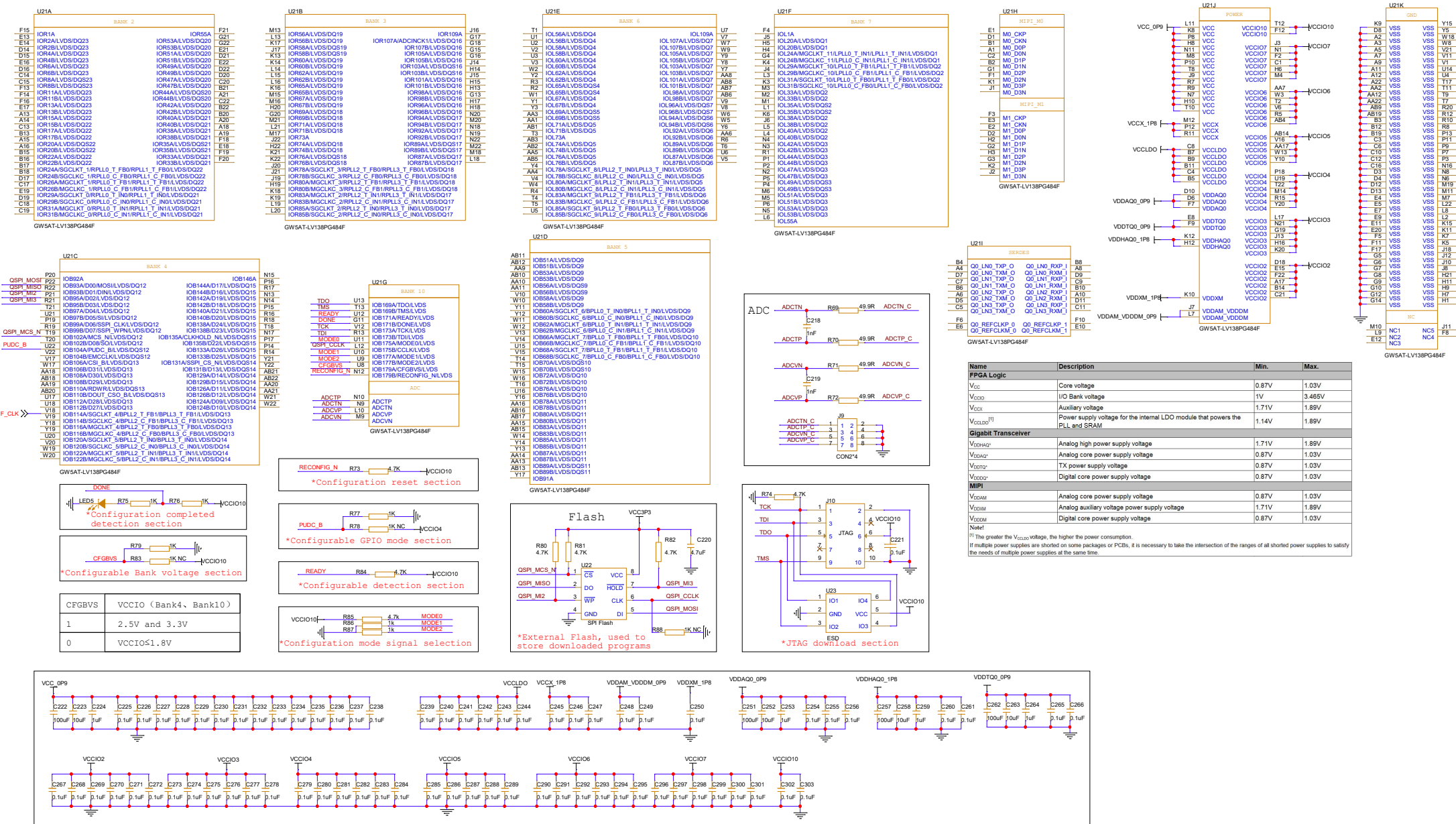
- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage,
a level shifter is required for voltage translation.

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| GOWIN Minimum System Diagram | | | | | | | | | |
| Size | Document Number | | | | | | | | Rev |
| C | GW5A-LV2SPG256 | | | | | | | | 3.6 |
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GW5A-LV25UG324F



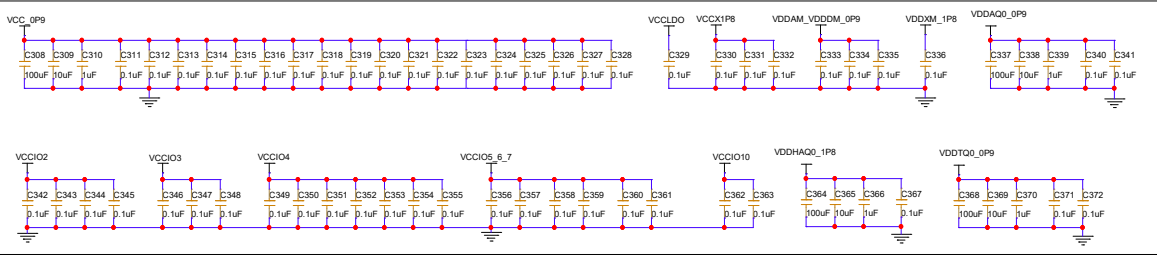
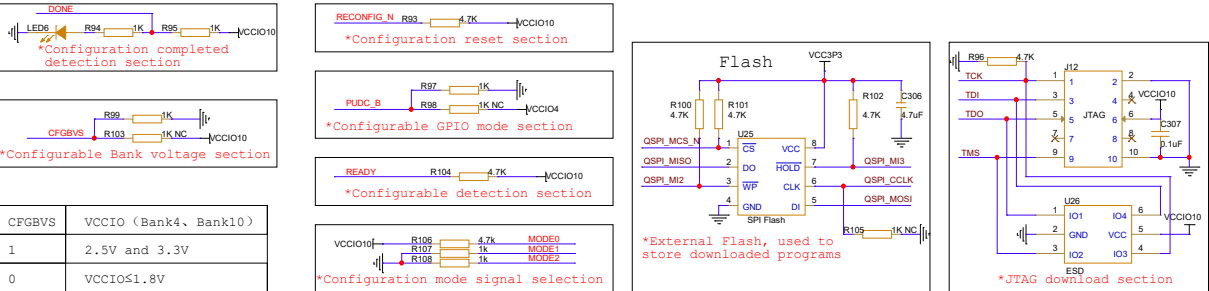
GW5AT-LV138PG484F



Notes

1. F_CLK signal is an external input clock signal.
- It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG704, Arora V FPGA Products Programming and Configuration Guide .
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. VCC core voltage requires a large current, so it is recommended to supply power separately.
5. The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, Arora V FPGA Products Programming and Configuration Guide .
6. The MSPI signal levels must match the Flash power supply voltage.
- If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

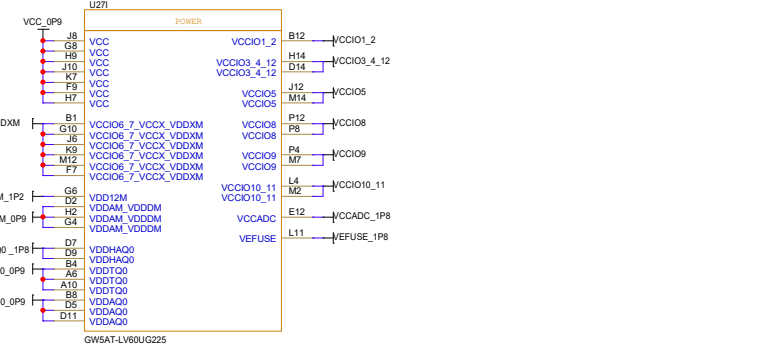
GW5AT-LV138UG324A



Notes:
1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.External Flash memory Is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG704,
Arora V FPGA Products Programming and Configuration Guide .
3.It is recommended that add an ESD protection chip to the JTAG download circuit.
4.VCC core voltage requires a large current, so it is recommended to supply power separately.
5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704,
Arora V FPGA Products Programming and Configuration Guide.
6.The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage,
a level shifter is required for voltage translation.

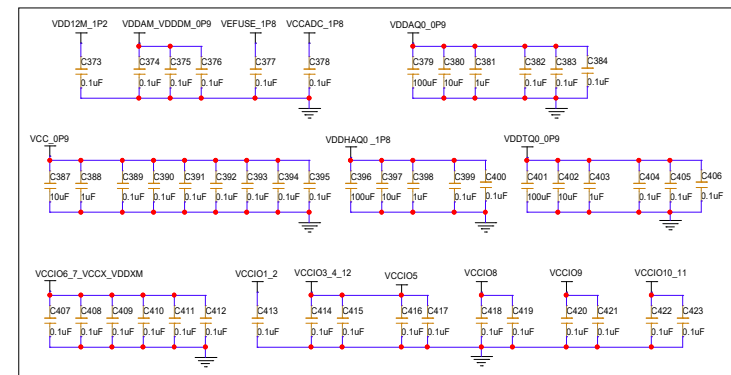
| Name | Description | Min. | Max. |
|---|---|-------|--------|
| FPGA Logic | | | |
| V _{CC} | Core voltage | 0.87V | 1.03V |
| V _{CCIO} | I/O Bank voltage | 1V | 3.465V |
| V _{CCX} | Auxiliary voltage | 1.71V | 1.89V |
| V _{CCIO0} ⁽¹⁾ | Power supply voltage for the internal LDO module that powers the PLL and SRAM | 1.14V | 1.89V |
| Gigabit Transceiver | | | |
| V _{DDHAQ0} | Analog high power supply voltage | 1.71V | 1.89V |
| V _{DDAQ0} | Analog core power supply voltage | 0.87V | 1.03V |
| V _{DDTQ0} | TX power supply voltage | 0.87V | 1.03V |
| V _{DDQ0} | Digital core power supply voltage | 0.87V | 1.03V |
| MIPI | | | |
| V _{DDAM} | Analog core power supply voltage | 0.87V | 1.03V |
| V _{DDDM} | Analog auxiliary voltage power supply voltage | 1.71V | 1.89V |
| V _{DDOM} | Digital core power supply voltage | 0.87V | 1.03V |
| Note! | | | |
| ⁽¹⁾ The greater the V _{CCIO0} voltage, the higher the power consumption. | | | |
| If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time. | | | |

GW5AT-LV60UG225



| Name | Description | Min. | Max. |
|----------------------------------|---------------------------------------|-------|--------|
| FPGA Logic | | | |
| V _{CC} | Core voltage, LV | 0.87V | 1.03V |
| V _{CC} | Core voltage, EV | 1.14V | 1.8V |
| V _{CCIO} | I/O Bank voltage | 1V | 3.465V |
| V _{CCX} ⁽¹⁾ | Auxiliary voltage | 1.71V | 3.465V |
| V _{FUSE} ⁽²⁾ | Voltage required for eFuse writing | 1.62V | 1.98V |
| Gigabit Transceiver | | | |
| V _{DDHAIQ} | Analog high power supply voltage | 1.71V | 1.89V |
| V _{DDAQ} | Analog core power supply voltage | 0.87V | 1.03V |
| V _{DDIO} | TX power supply voltage | 0.87V | 1.03V |
| V _{DDO} | Digital power supply voltage | 0.87V | 1.03V |
| MIPI | | | |
| V _{DDAI} | Analog core power supply voltage | 0.87V | 1.08V |
| V _{DDAI} | Analog auxiliary power supply voltage | 1.71V | 3.465V |
| V _{DDO} | Digital power supply voltage | 0.87V | 1.08V |
| V _{DDIM} | MIPI LP power supply voltage | 1.14V | 1.32V |
| ADC | | | |
| V _{CCADC} | ADC power supply voltage | 1.62V | 1.98V |
| V _{REFN} | ADC reference voltage | 0V | 0V |
| V _{REFP} | ADC reference voltage | 0V | 1.25V |

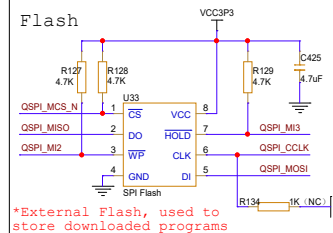
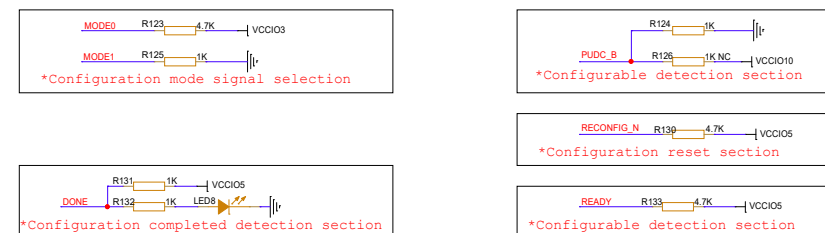
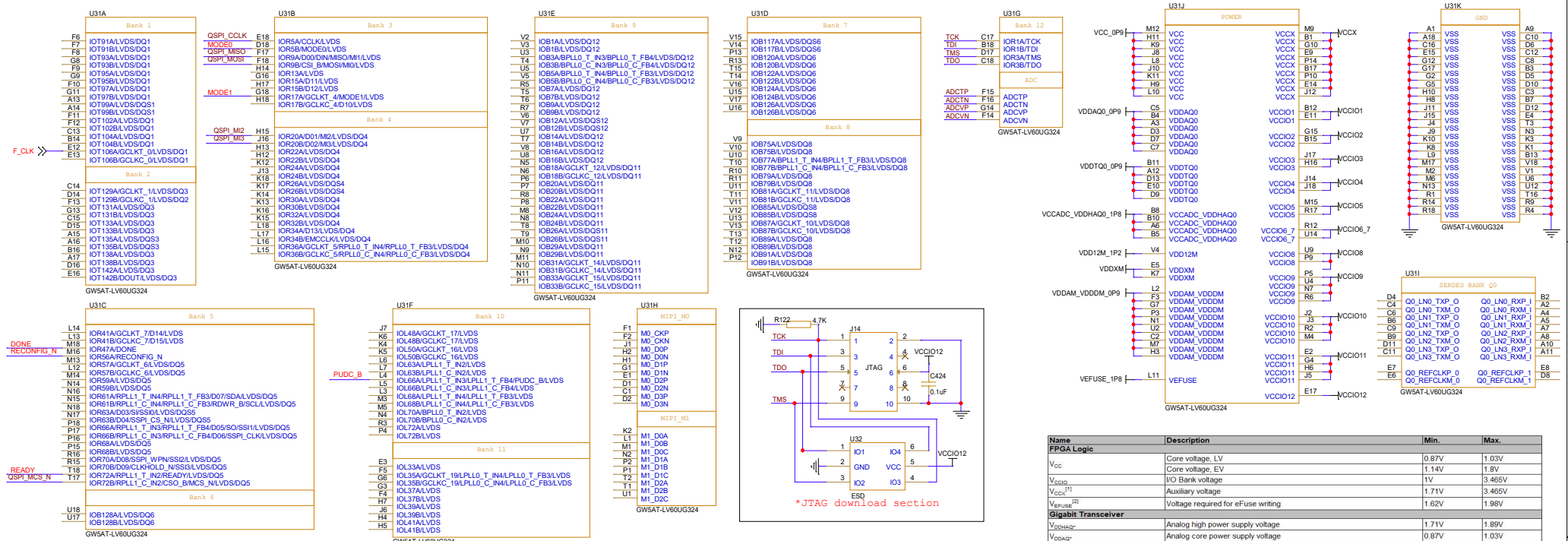
[2] When V_{FUSE} is not required, this power supply can be connected to either GND or floating.



Notes:

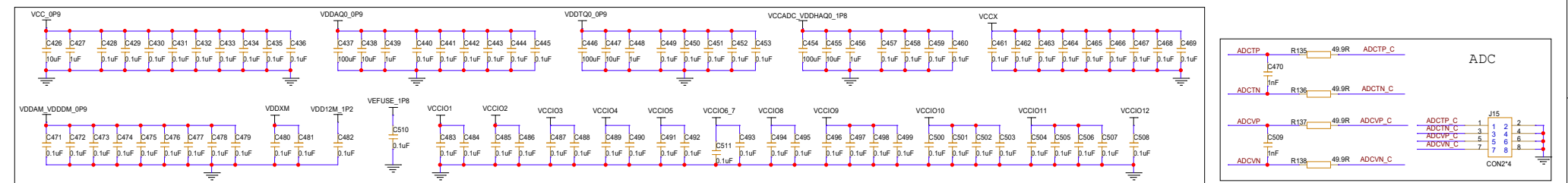
- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Arara V 60K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arara V 60K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

GW5AT-LV60UG324



| Pin Name | Description | Min. | Max. |
|------------------------------------|---|-------|----------------------|
| PPGA Logic | | | |
| V _{CC} | Core voltage, LV | 0.87V | 1.03V ^[1] |
| V _{CCIO} | Core voltage, HV | 1.14V | 1.18V |
| V _{CCIO} ^[11] | I/O Bank voltage | 0.87V | 3.465V |
| V _{CCIO} ^[12] | Auxiliary voltage | 1.71V | 3.465V |
| V _{PEUSER} ^[2] | Voltage required for eFUSE writing | 1.62V | 1.98V |
| Gigabit Transceiver | | | |
| V _{DDH4G+} | Analogue high power supply voltage | 1.71V | 1.89V |
| V _{DDH4G+} ^[2] | Analogue core power supply voltage | 0.87V | 1.03V |
| V _{DDIO12+} | TX power supply voltage | 0.87V | 1.03V |
| V _{DDIO2+} | Digital power supply voltage | 0.87V | 1.03V |
| MIPI | | | |
| V _{DDAM} | Analogue core power supply voltage | 0.87V | 1.08V |
| V _{DDOM1} | Analogue auxiliary power supply voltage | 1.71V | 3.465V |
| V _{DDOM} | Digital power supply voltage | 0.87V | 1.08V |
| V _{DDIO2M} | MIPI LP power supply voltage | 1.14V | 1.32V |
| ADC | | | |
| V _{REFADP} | ADC power supply voltage | 1.62V | 1.98V |
| V _{REFINL} | ADC reference voltage | 0V | 0V |
| V _{REFFP} | ADC reference voltage | 0V | 1.25V |

Note:
^[1] When internal differential termination resistors are required, V_{CCIO} must be greater than or equal to 3V; the IO input-output F_{max} is limited when V_{CCIO}=1.8V, and V_{CCIO} needs to be greater than or equal to 2.5V for input-output applications with F_{max} greater than 600Mbps.
^[2] When V_{PEUSER} is not required, this power supply can be connected to either GND or floating.
^[3] If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies.



Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F.CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage,
a level shifter is required for voltage translation.

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| Title | | | |
| GOWIN Minimum System Diagram | | | |
| Size | Document Number | | Rev |
| C | GW5AT-LV80UG324 | | 3.6 |
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