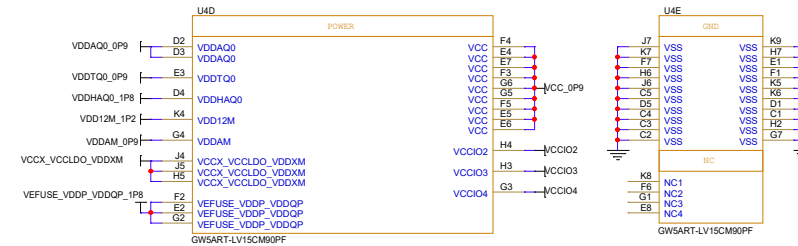
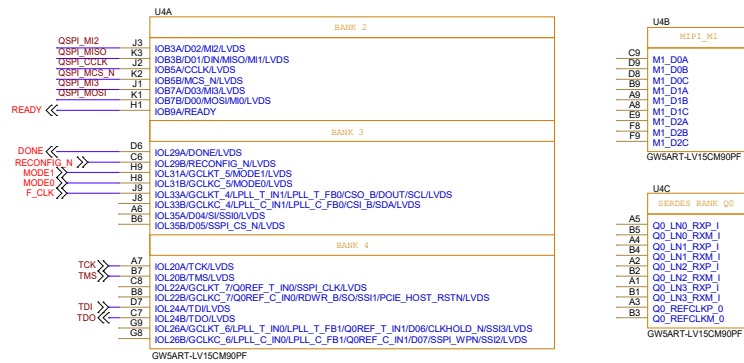


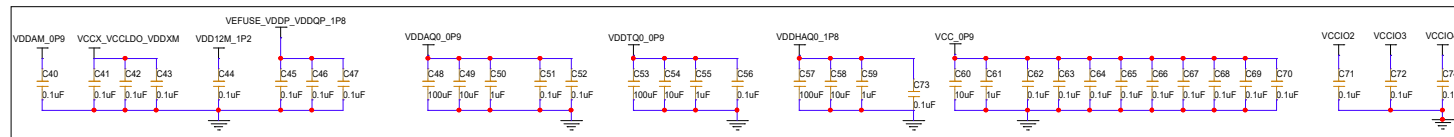
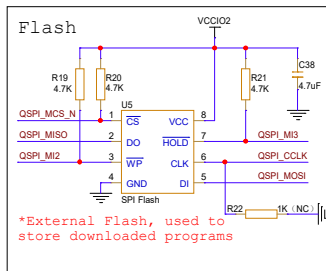
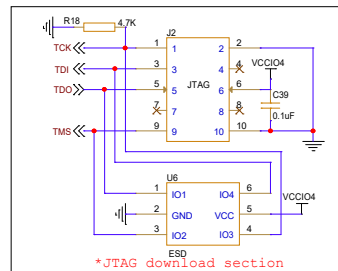
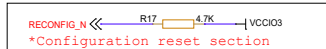
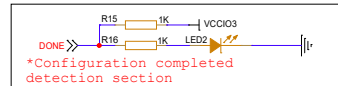
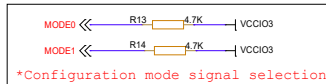
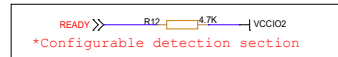
GW5ART-LV15CM90PF



Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCX} ^[1]	Auxiliary voltage	1.71V	3.465V
V _{CCLDO}	Power supply voltage of internal LDO module that powers PLL and SRAM	1.14V	2.75V
V _{EFUSE} ^[2]	Voltage required for eFuse writing	1.62V	1.98V
Gigabit Transceiver			
V _{DDHAQ*}	Analog high power supply voltage	1.71V	1.89V
V _{DDAQ*}	Analog core power supply voltage	0.87V	1.03V
V _{DDTG*}	Serdes transmitter power supply voltage	0.87V	1.03V
MIPI			
V _{DDAM}	Analog core power supply voltage	0.855V	1.08V
V _{DDXM}	Analog auxiliary power supply voltage	1.71V	3.465V
V _{DDDM}	Digital core power supply voltage	0.87V	1.08V
V _{DD12M}	MIPI LP power supply voltage	1.14V	1.32V
PSRAM			
V _{DDP}	PSRAM power supply voltage	1.71V	1.89V
V _{DDDP}	PSRAM data bus power supply voltage	1.71V	1.89V

[1] When internal differential termination resistors are required, Vccx must be greater than or equal to 3V; the IO input-output Fmax is limited when Vccx=1.8V, and Vccx needs to be greater than or equal to 2.5V for input-output applications with Fmax greater than 600Mbps.

If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.

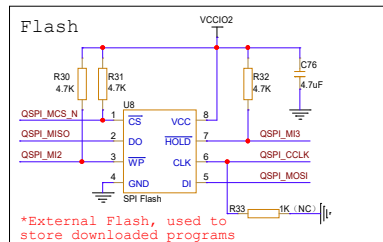
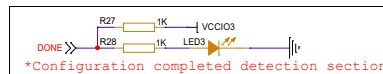
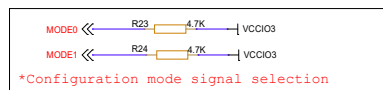
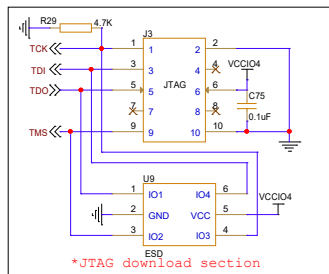
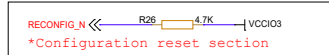
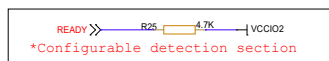
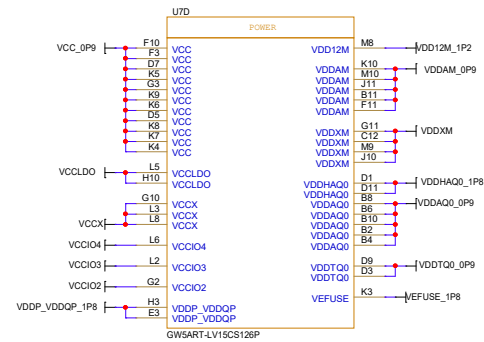
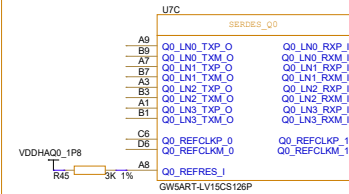
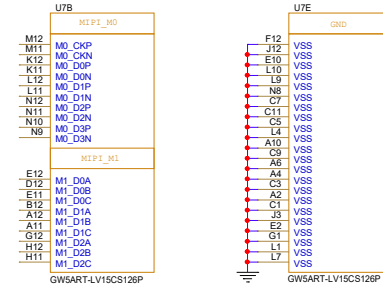
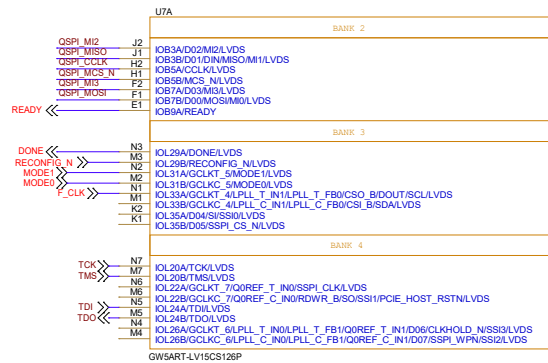


Notes:

1. F_CLK signal is an external input clock signal.
- It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG720, Arora 15K FPGA Products Programming and Configuration V Guide.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. VCC core voltage requires a large current, so it is recommended to supply power separately.
5. The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG720, Arora V 15K FPGA Products Programming and Configuration Guide.

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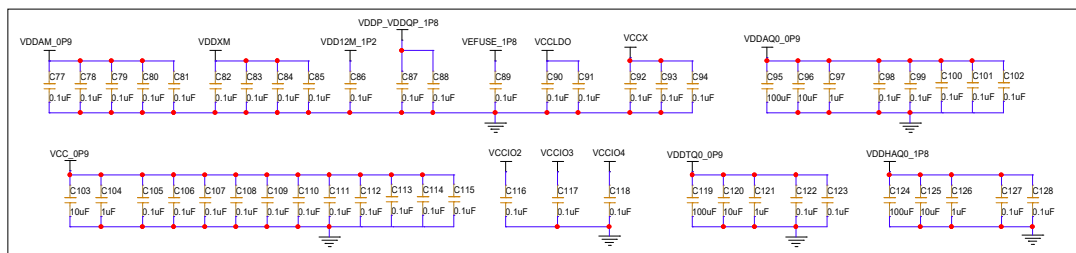


Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCX} ^[1]	Auxiliary voltage	1.71V	3.465V
V _{CC_LDO}	Power supply voltage of internal LDO module that powers PLL and SRAM	1.14V	2.75V
V _{FUSE} ^[2]	Voltage required for eFuse writing	1.62V	1.98V
Gigabit Transceiver			
V _{DDHAQ*}	Analog high power supply voltage	1.71V	1.89V
V _{DDAQ*}	Analog core power supply voltage	0.87V	1.03V
V _{DDTG*}	Serdes transmitter power supply voltage	0.87V	1.03V
MIPI			
V _{DDAM}	Analog core power supply voltage	0.855V	1.08V
V _{DDXM}	Analog auxiliary power supply voltage	1.71V	3.465V
V _{DDDM}	Digital core power supply voltage	0.87V	1.08V
V _{DD12M}	MIPI LP power supply voltage	1.14V	1.32V
PSRAM			
V _{DDP}	PSRAM power supply voltage	1.71V	1.89V
V _{DDQP}	PSRAM data bus power supply voltage	1.71V	1.89V

[1] When internal differential termination resistors are required, Vccx must be greater than or equal to 3V; the IO input-output Fmax is limited when Vccx=1.8V, and Vccx needs to be greater than or equal to 2.5V for input-output applications with Fmax greater than 600Mbps.

[2] When V_{EFUSE} is not required, this power supply can be connected to either GND or floating.

If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.

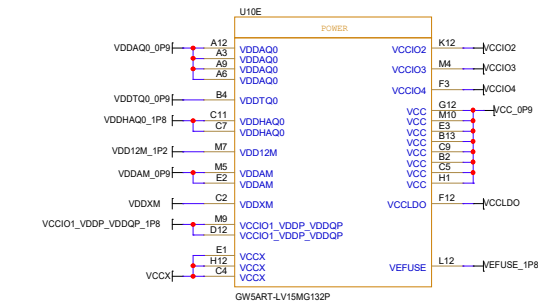
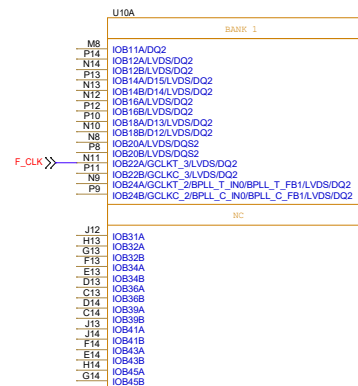
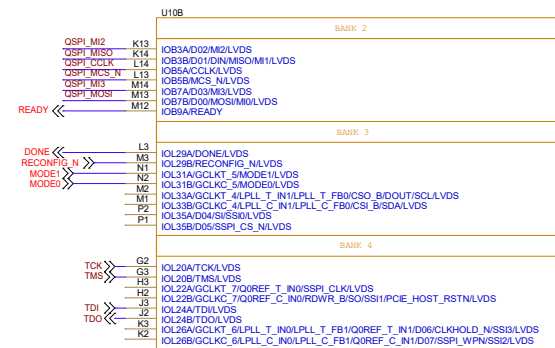


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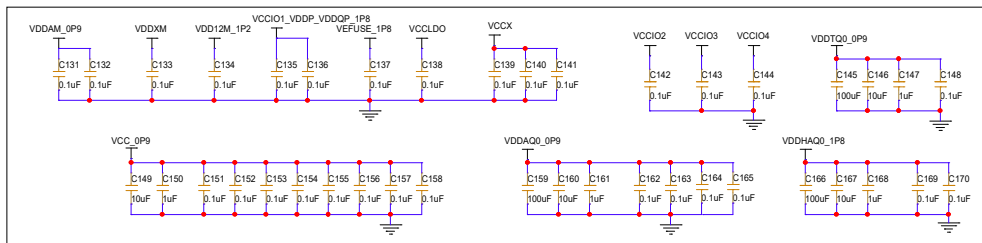
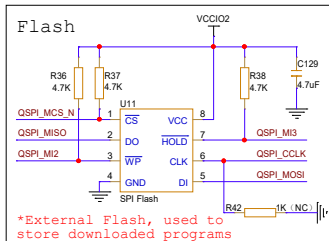
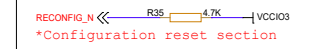
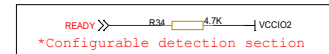
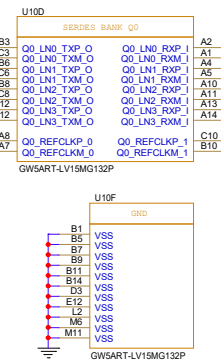
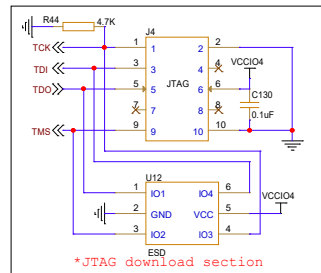
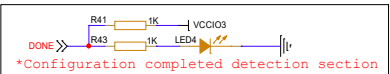
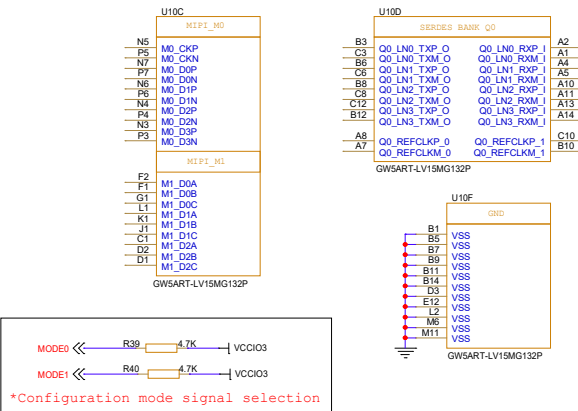
1. FL CLK signal is an external input clock signal.
It is recommended that FL CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG720, Arora 15K FPGA Products Programming and Configuration V Guide.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. VCC core voltage requires a large current, so it is recommended to supply power separately.
5. The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG720, Arora V 15K FPGA Products Programming and Configuration Guide.

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Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{COX} ^[1]	Auxiliary voltage	1.71V	3.465V
V _{CC} LDO	Power supply voltage of internal LDO module that powers PLL and SRAM	1.14V	2.75V
V _{EFUSE} ^[2]	Voltage required for eFuse writing	1.62V	1.98V
Gigabit Transceiver			
V _{DD} HAQ*	Analog high power supply voltage	1.71V	1.89V
V _{DD} AG*	Analog core power supply voltage	0.87V	1.03V
V _{DD} TO*	Serdes transmitter power supply voltage	0.87V	1.03V
MIPI			
V _{DD} AM	Analog core power supply voltage	0.855V	1.08V
V _{DD} XM	Analog auxiliary power supply voltage	1.71V	3.465V
V _{DD} DM	Digital core power supply voltage	0.87V	1.08V
V _{DD} I2M	MIPI LP power supply voltage	1.14V	1.32V
PSRAM			
V _{DD} P	PSRAM power supply voltage	1.71V	1.89V
V _{DD} QP	PSRAM data bus power supply voltage	1.71V	1.89V
Note!			
^[1] When internal differential termination resistors are required, V _{CC} x must be greater than or equal to 3V; the IO input-output F _{max} is limited when V _{CC} x=1.8V, and V _{CC} x needs to be greater than or equal to 2.5V for input-output applications with F _{max} greater than 600Mbps. ^[2] When V _{EFUSE} is not required, this power supply can be connected to either GND or floating. If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			



Notes:

- 1.F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG720, Arora 15K FPGA Products Programming and Configuration V Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG720, Arora V 15K FPGA Products Programming and Configuration Guide.