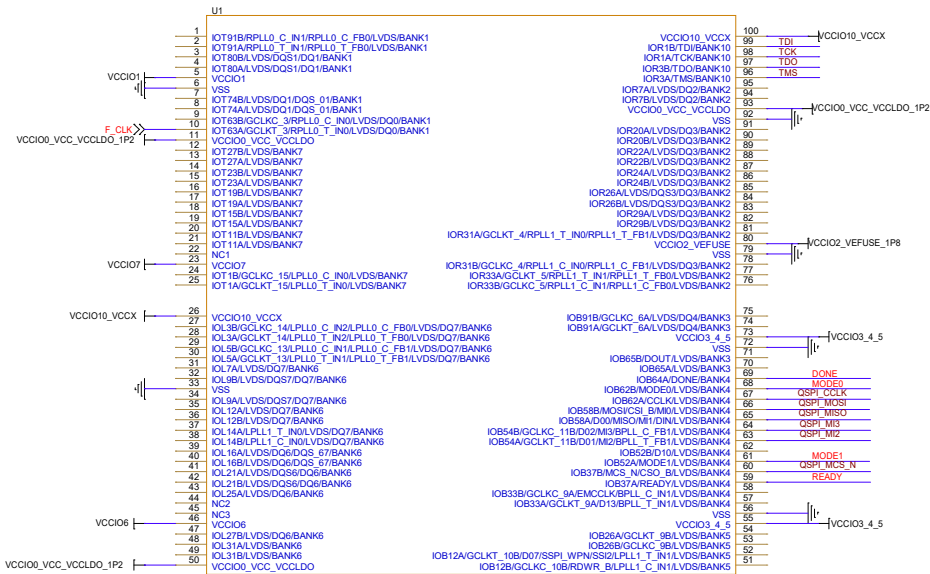
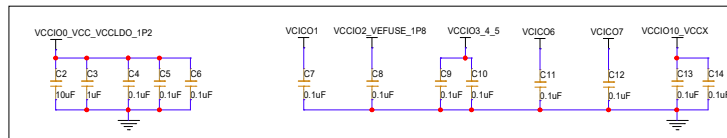


***GW5A-EV25LQ100***



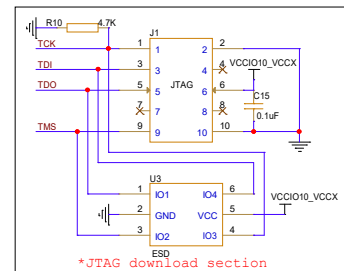
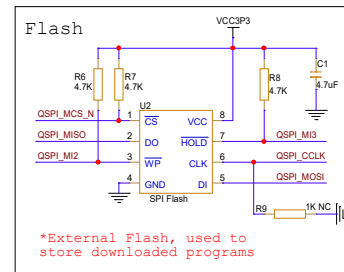
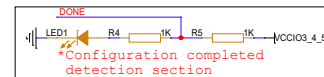
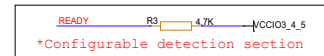
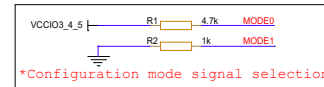
GW5A-EV25LQ100



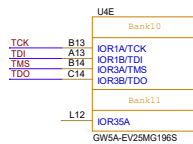
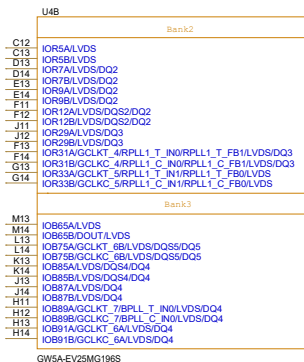
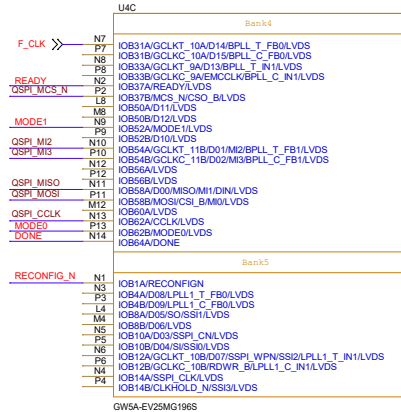
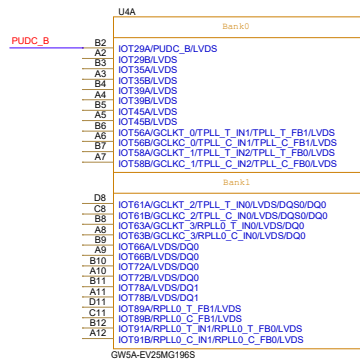
Name	Description	Min.	Max.
<b>FPGA Logic</b>			
V <sub>CC</sub>	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V <sub>COG</sub>	I/O Bank voltage	1.14V	3.465V
V <sub>CDK</sub>	Auxiliary voltage	2.375	3.465V
V <sub>CCDDO</sub> <sup>(1)</sup>	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V <sub>EFUSE</sub> <sup>(2)</sup>	Voltage required for eFuse writing	1.62V	1.98V
<b>MIPI</b>			
V <sub>DDAM</sub>	Analog core power supply voltage	0.87V	1V
V <sub>DDCM</sub>	Digital core power supply voltage	0.87V	1V
V <sub>DDIM</sub>	Analog auxiliary power supply voltage	2.375V	3.465V
V <sub>DD12M</sub>	MIPI LP power supply voltage	1.14V	1.32V
<b>Notes:</b>			
<sup>(1)</sup> The greater the V <sub>CCDDO</sub> voltage, the higher the power consumption.			
<sup>(2)</sup> When V <sub>EFUSE</sub> is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of all shorted power supplies as the minimum voltage to ensure the needs of multiple power supplies at the same time.			

Notes:

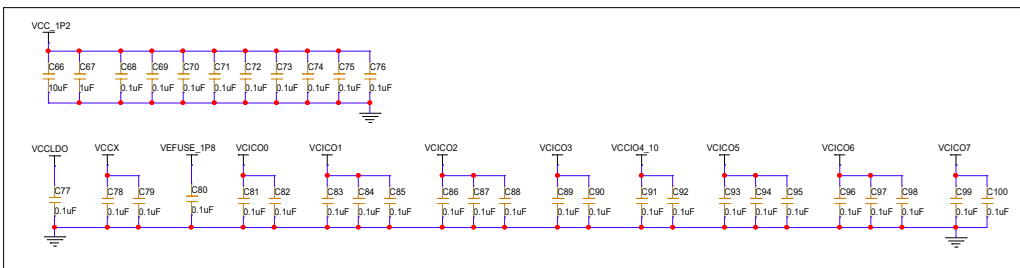
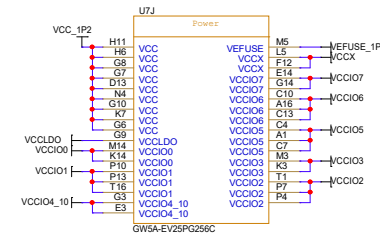
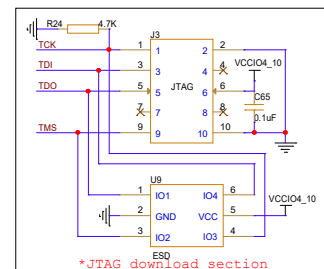
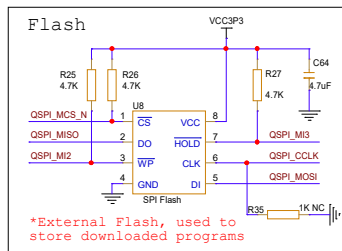
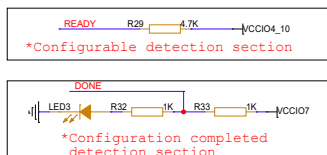
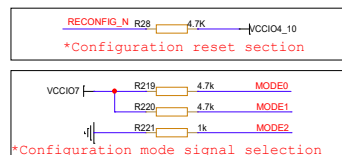
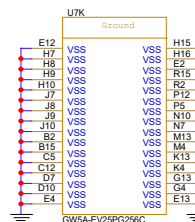
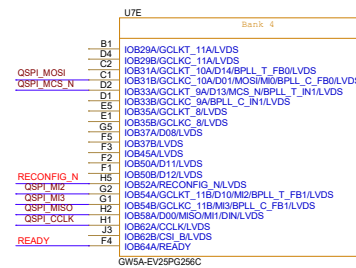
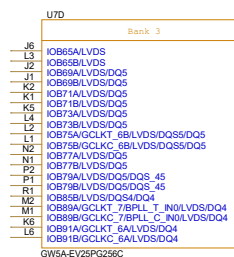
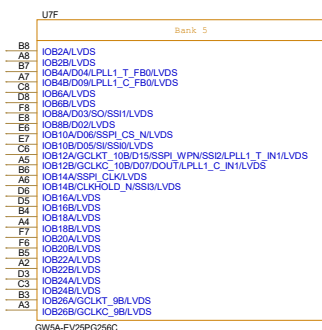
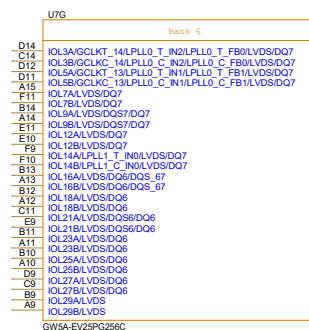
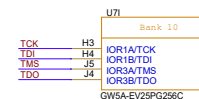
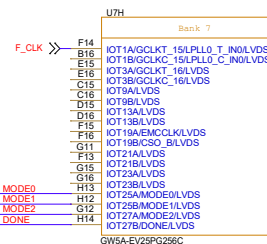
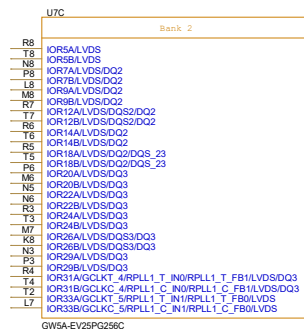
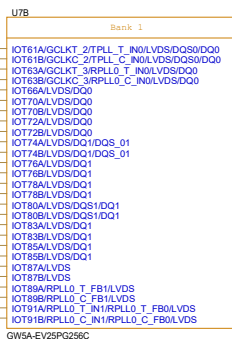
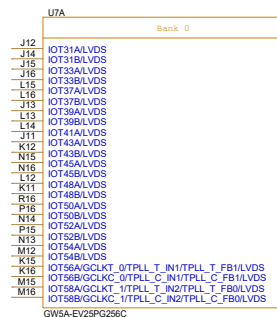
- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.  
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.  
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.  
If the voltage of the MSPI BANK does not match the Flash power supply voltage,  
a level shifter is required for voltage translation.



# GW5A-EV25MG196S



***GW5A-EV25PG256C***



Notes:

- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.  
For details about SPI Flash Model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.  
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.  
If the voltage of the MSPI BANK does not match the Flash power supply voltage,  
a level shifter is required for voltage translation.

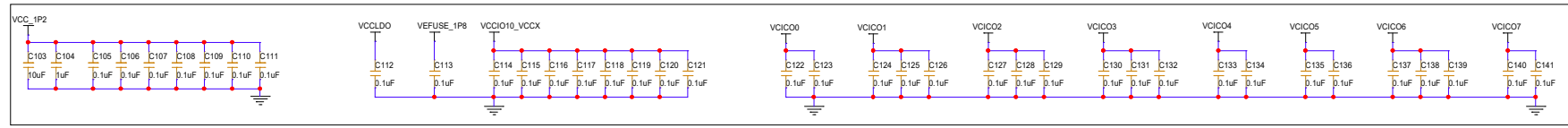
Name	Description	Min.	Max.
<b>FPGA Logic</b>			
V <sub>CC</sub>	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V <sub>CCIO</sub>	I/O Bank voltage	1.14V	3.465V
V <sub>CCX</sub>	Auxiliary voltage	2.375	3.465V
V <sub>CCDDO</sub> <sup>[1]</sup>	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V <sub>EFUSE</sub> <sup>[2]</sup>	Voltage required for eFuse writing	1.62V	1.98V
<b>MIPI</b>			
V <sub>DDAM</sub>	Analog core power supply voltage	0.87V	1V
V <sub>DDDM</sub>	Digital core power supply voltage	0.87V	1V
V <sub>DDXM</sub>	Analog auxiliary power supply voltage	2.375V	3.465V
V <sub>DD12M</sub>	MIPI LP power supply voltage	1.14V	1.32V
<b>Note!</b>			
<sup>[1]</sup> The greater the V <sub>CCDDO</sub> voltage, the higher the power consumption.			
<sup>[2]</sup> When V <sub>EFUSE</sub> is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies.			

Title				
GOWIN Minimum System Diagram				
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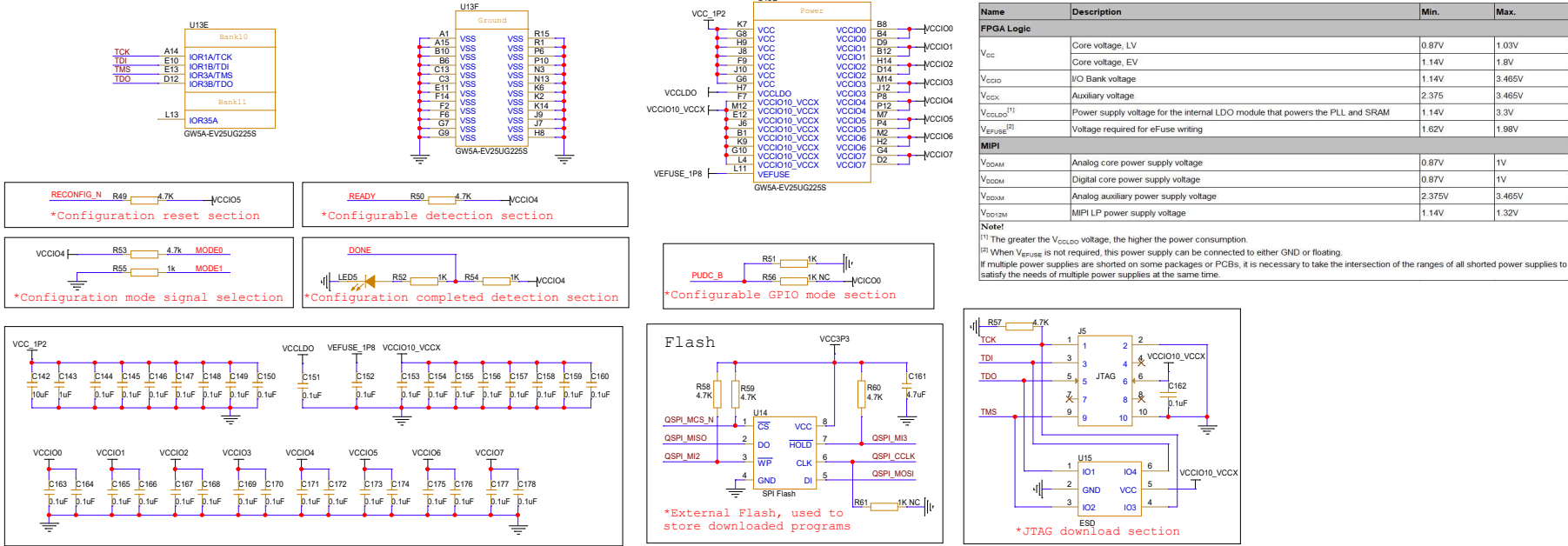
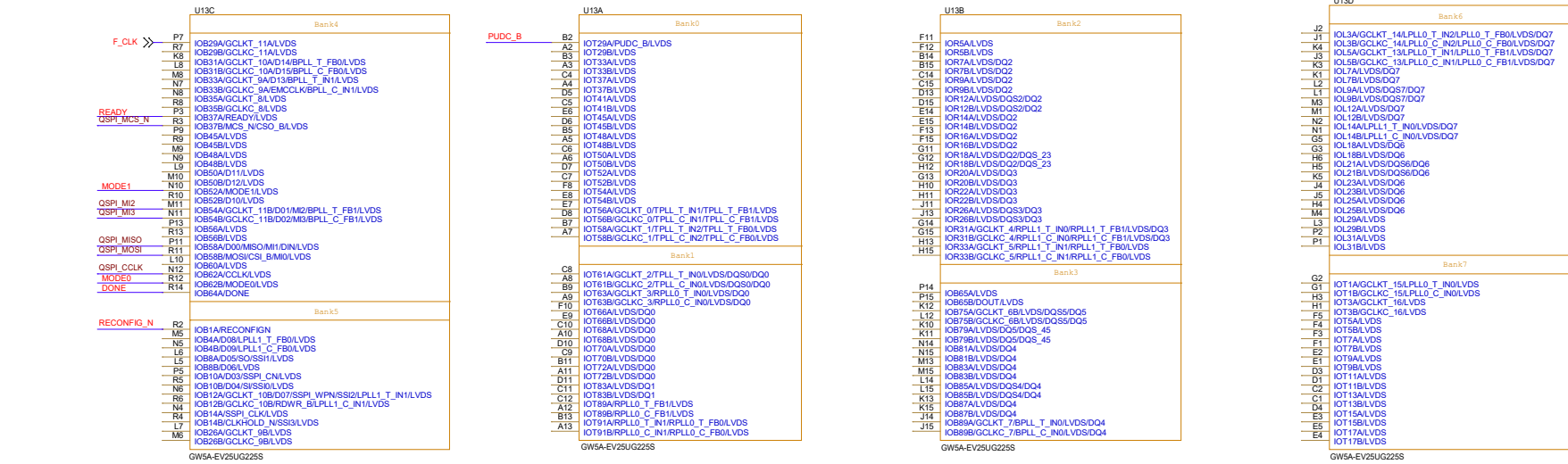
Name	Description	Min.	Max.
<b>FPGA Logic</b>			
V <sub>CC</sub>	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V <sub>CCIO</sub>	I/O Bank voltage	1.14V	3.465V
V <sub>CCX</sub>	Auxiliary voltage	2.375	3.465V
V <sub>CCDDO</sub> <sup>[1]</sup>	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V <sub>EFUSE</sub> <sup>[2]</sup>	Voltage required for eFuse writing	1.62V	1.98V
<b>MIPI</b>			
V <sub>DDMM</sub>	Analog core power supply voltage	0.87V	1V
V <sub>DDDM</sub>	Digital core power supply voltage	0.87V	1V
V <sub>DDMM</sub>	Analog auxiliary power supply voltage	2.375V	3.465V
V <sub>DD12M</sub>	MIPI LP power supply voltage	1.14V	1.32V
<b>Note!</b>			
[1] The greater the V <sub>CCDDO</sub> voltage, the higher the power consumption.			
[2] When V <sub>EFUSE</sub> is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of all shorted power supplies to			



Notes:

- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.  
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.  
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 6.The MSPI signal levels must match the Flash power supply voltage.  
If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

Title			
GOWIN Minimum System Diagram			
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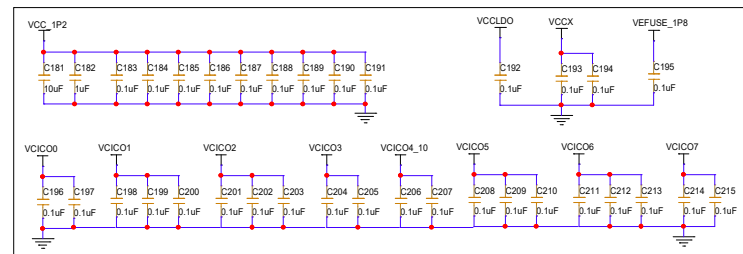
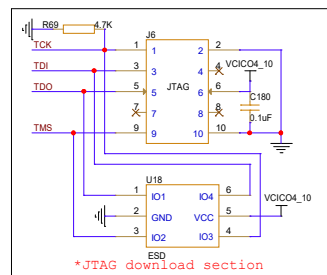
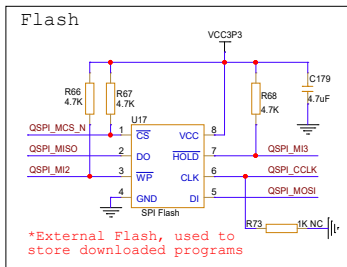
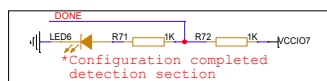
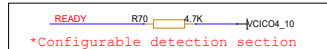
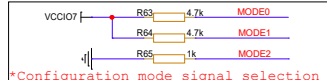
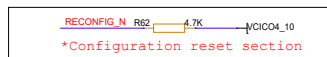
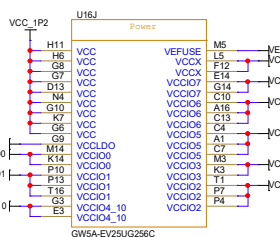
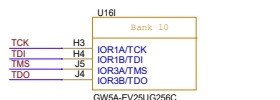
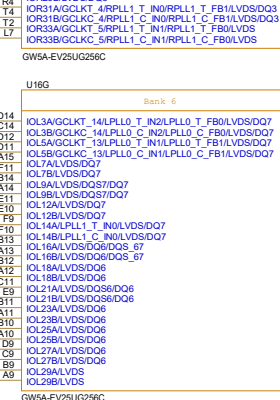
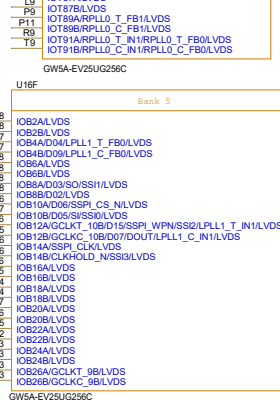
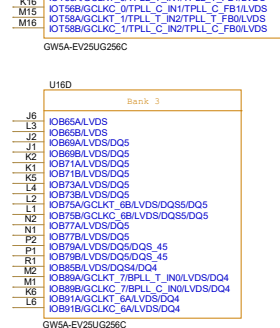
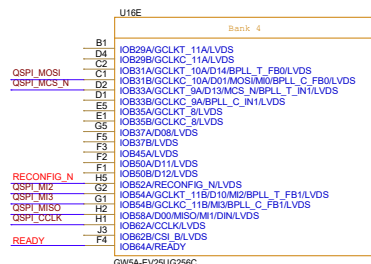
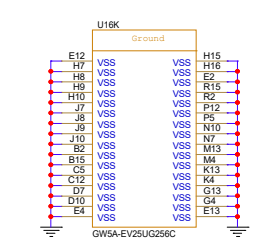
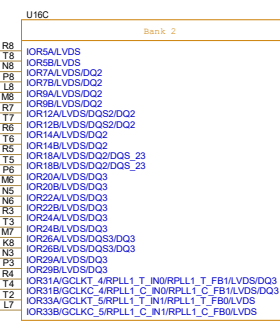
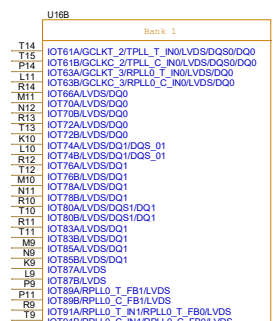
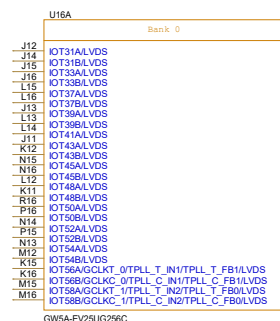
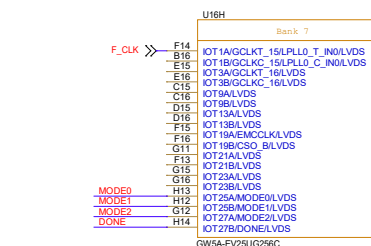


Notes:

- 1.F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage. If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.



***GW5A-EV25UG256C***



Name	Description	Min.	Max.
<b>FPGA Logic</b>			
V <sub>CC</sub>	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V <sub>CCIO</sub>	I/O Bank voltage	1.14V	3.465V
V <sub>CCAUX</sub>	Auxiliary voltage	2.375	3.465V
V <sub>CCDDO</sub> <sup>[1]</sup>	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V <sub>EPUSE</sub> <sup>[2]</sup>	Voltage required for eFuse writing	1.62V	1.98V
<b>MIPI</b>			
V <sub>DDAM</sub>	Analog core power supply voltage	0.87V	1V
V <sub>DDDM</sub>	Digital core power supply voltage	0.87V	1V
V <sub>DDOIM</sub>	Analog auxiliary power supply voltage	2.375V	3.465V
V <sub>DDI2M</sub>	MIPI LP power supply voltage	1.14V	1.32V

<sup>[1]</sup> The greater the  $V_{CC,DO}$  voltage, the higher the power consumption.

<sup>[2]</sup> When  $V_{EFUSE}$  is not required, this power supply can be connected to either GND or floating.

If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.

Notes:

1.F CLK signal is an external input clock signal.

It is recommended that F CLK signal be provided through an active oscillator crystal.

2.External Flash memory is used to store downloaded programs

For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714,

Arora V 25K FPGA Products Programming and Configuration Guide .

3.It is recommended that add an ESD protection chip to the JTAG downlo

4.VCC core voltage requires a large current, so it is recommended to supply power separately.

5. The MODE pin is the GowinCONFIG configuration mode selection signal.

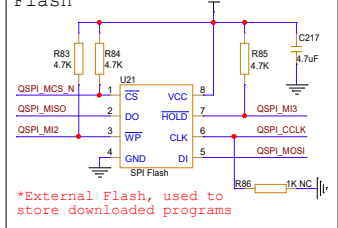
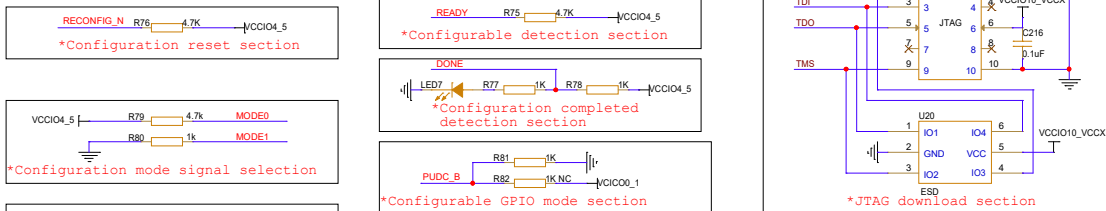
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714.

Arora V 25K FPGA Products Programming and Configuration Guide.

6. The MSPI signal levels must match the Flash power supply voltage.

If the voltage of the MSPI BANK does not match the Flash power supply

***GW5A-EV25UG324S***



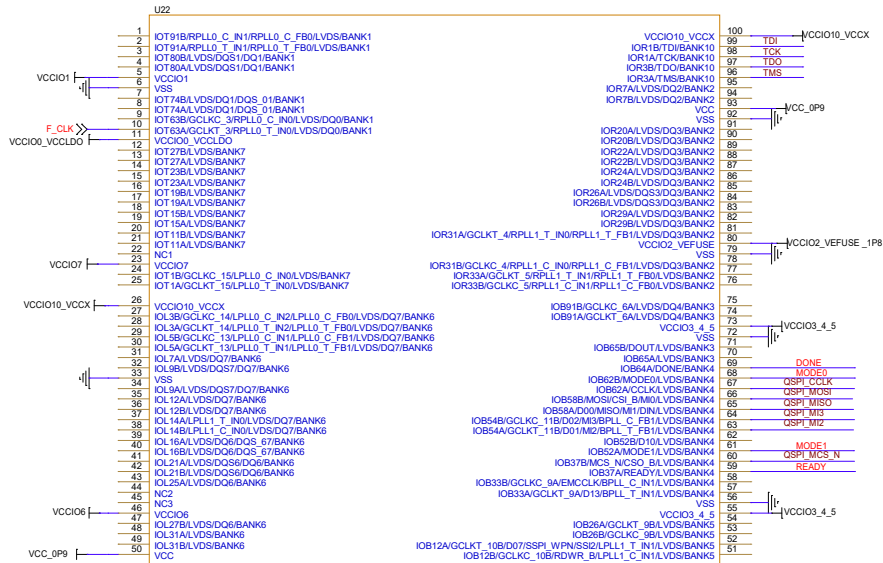
Notes:

- 1.F CLK signal is an external input clock signal.
- It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory Is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.
- If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

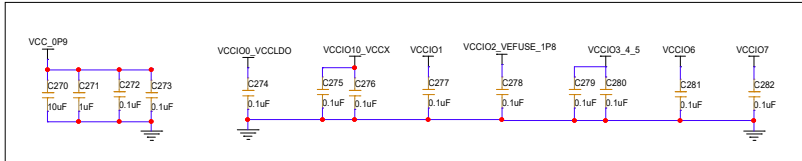
Name	Description	Min.	Max.
<b>PPGA Logic</b>			
V <sub>CC</sub>	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V <sub>COO</sub>	I/O Bank voltage	1.14V	3.465V
V <sub>GCK</sub>	Auxiliary voltage	2.375	3.465V
V <sub>CCDDO</sub> <sup>[1]</sup>	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V <sub>EFUSE</sub> <sup>[2]</sup>	Voltage required for eFuse writing	1.62V	1.98V
<b>MIPI</b>			
V <sub>DDAM</sub>	Analog core power supply voltage	0.87V	1V
V <sub>DDCM</sub>	Digital core power supply voltage	0.87V	1V
V <sub>DDCM</sub>	Analog auxiliary power supply voltage	2.375V	3.465V
V <sub>DD12M</sub>	MIPI LP power supply voltage	1.14V	1.32V
<b>Note:</b>			
<sup>[1]</sup> The greater the V <sub>CCDDO</sub> voltage, the higher the power consumption.			
<sup>[2]</sup> When V <sub>EFUSE</sub> is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shared on some packages or PCBs, it is necessary to take the intersection of the ranges of all shared power supplies to satisfy the needs of multiple power supplies at the same time.			

Title			
GOWIN Minimum System Diagram			
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***GW5A-LV25LQ100***



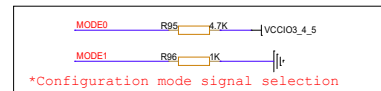
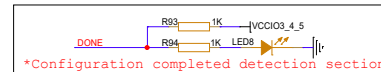
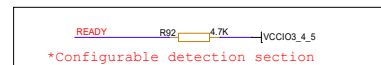
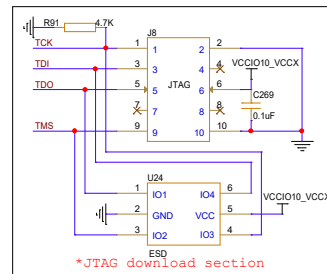
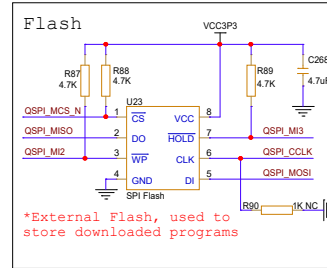
GW5A-LV25LQ100



Name	Description	Min.	Max.
<b>FPGA Logic</b>			
V <sub>CC</sub>	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V <sub>CGO</sub>	I/O Bank voltage	1.14V	3.465V
V <sub>GCK</sub>	Auxiliary voltage	2.375	3.465V
V <sub>CDDO</sub> <sup>[1]</sup>	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V <sub>EFUSE</sub> <sup>[2]</sup>	Voltage required for eFuse writing	1.62V	1.98V
<b>MIPI</b>			
V <sub>DDAM</sub>	Analog core power supply voltage	0.87V	1V
V <sub>DDCM</sub>	Digital core power supply voltage	0.87V	1V
V <sub>DDIM</sub>	Analog auxiliary power supply voltage	2.375V	3.465V
V <sub>DD12M</sub>	MIPI LP power supply voltage	1.14V	1.32V
<b>Note:</b>			
[1] The greater the V <sub>CDDO</sub> voltage, the higher the power consumption.			
[2] When V <sub>EFUSE</sub> is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to ensure the correct voltage.			

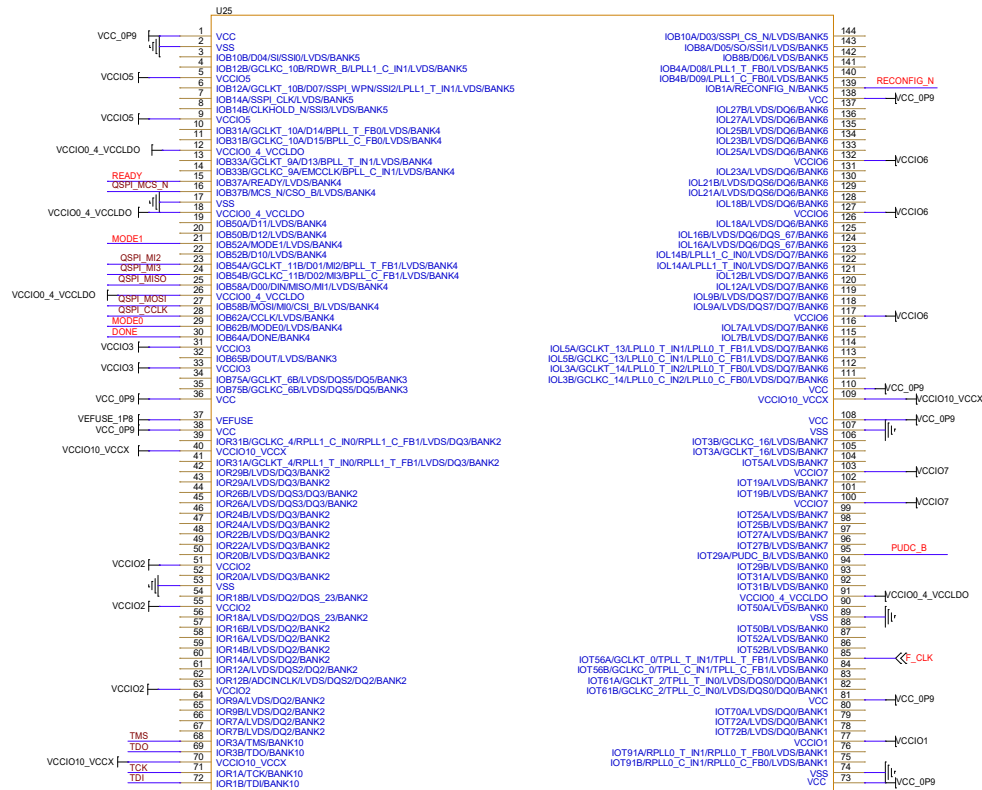
Notes:

- 1.F CLK signal is an external input clock signal.
- It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.
- If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.





***GW5A-LV25LQ144***

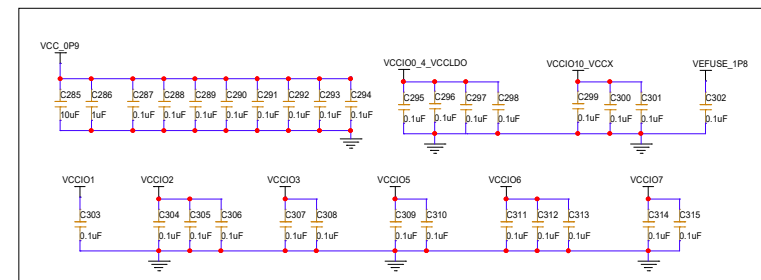
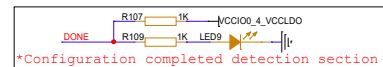
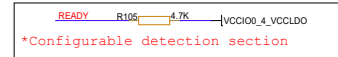
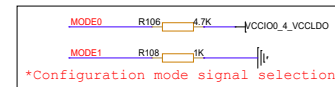
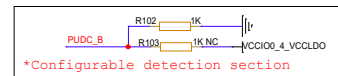
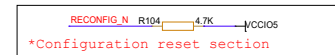
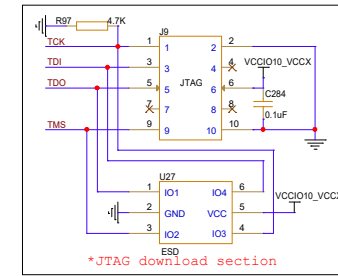
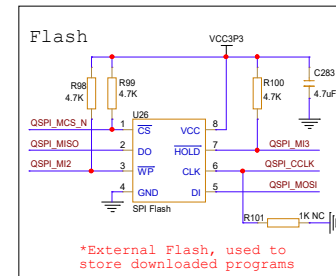


GW5A-LV25LQ144

Name	Description	Min.	Max.
<b>PPGA Logic</b>			
V <sub>CC</sub>	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V <sub>CGO</sub>	I/O Bank voltage	1.14V	3.465V
V <sub>GCK</sub>	Auxiliary voltage	2.375	3.465V
V <sub>CCLD0</sub> <sup>[1]</sup>	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V <sub>EUFUSE</sub> <sup>[2]</sup>	Voltage required for eFuse writing	1.62V	1.98V
<b>MIPI</b>			
V <sub>DDAM</sub>	Analog core power supply voltage	0.87V	1V
V <sub>DDCM</sub>	Digital core power supply voltage	0.87V	1V
V <sub>DDCM</sub>	Analog auxiliary power supply voltage	2.375V	3.465V
V <sub>DD12M</sub>	MIPI LP power supply voltage	1.14V	1.32V
<b>Note:</b>			
<sup>[1]</sup> The greater the V <sub>CCLD0</sub> voltage, the higher the power consumption.			
<sup>[2]</sup> When V <sub>EUFUSE</sub> is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			

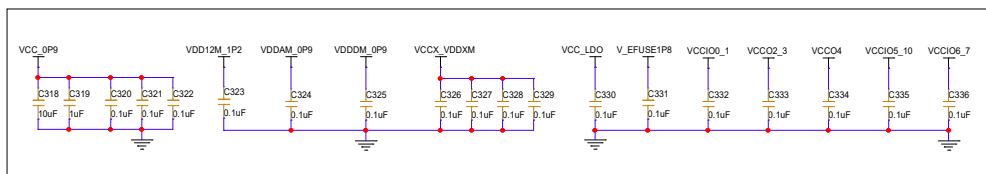
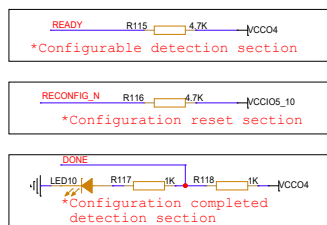
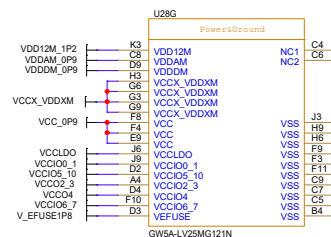
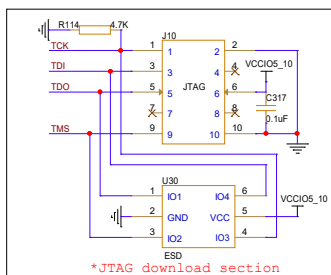
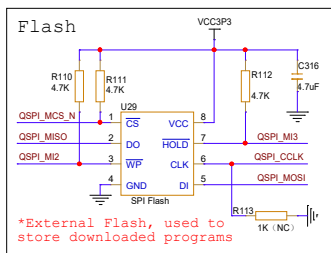
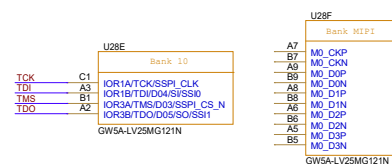
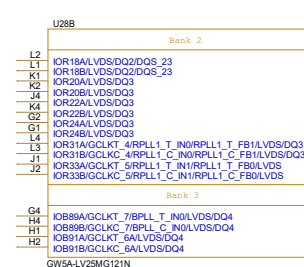
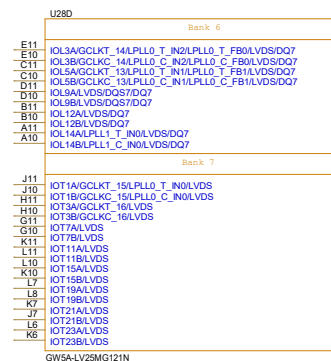
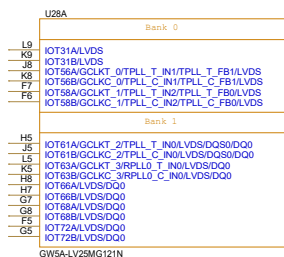
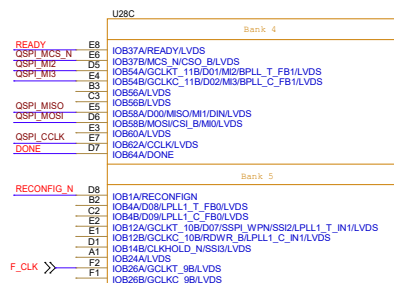
Notes:

1. F CLK signal is an external input clock signal.
- It is recommended that F CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
- For details about SPI Flash mode selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. VCC core voltage requires a large current, so it is recommended to supply power separately.
5. The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode pin, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
6. The MSPI signal levels must match the Flash power supply voltage.
- If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.



Title			
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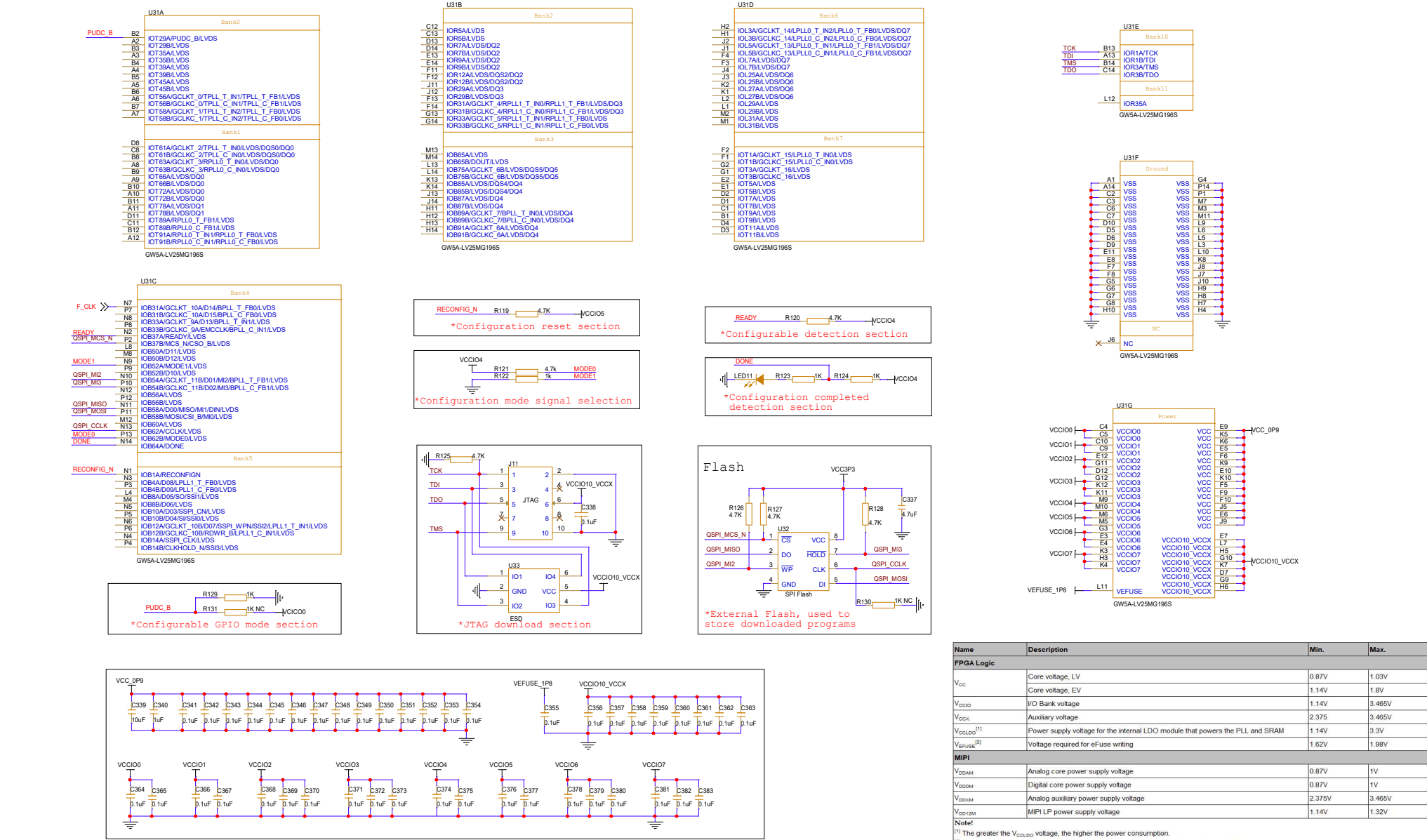
Notes:

- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.  
For details about SPI Flash mode selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.  
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.  
If the voltage of the MSPI BANK does not match the Flash power supply voltage,  
a level shifter is required for voltage translation.

Name	Description	Min.	Max.
<b>FPGA Logic</b>			
V <sub>CC</sub>	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V <sub>CCIO</sub>	I/O Bank voltage	1.14V	3.465V
V <sub>CCX</sub>	Auxiliary voltage	2.375	3.465V
V <sub>CCDDO</sub> <sup>[1]</sup>	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V <sub>EFUSE</sub> <sup>[2]</sup>	Voltage required for eFuse writing	1.62V	1.98V
<b>MIPI</b>			
V <sub>DDMM</sub>	Analog core power supply voltage	0.87V	1V
V <sub>DDDM</sub>	Digital core power supply voltage	0.87V	1V
V <sub>DDXMM</sub>	Analog auxiliary power supply voltage	2.375V	3.465V
V <sub>DD12M</sub>	MIPI LP power supply voltage	1.14V	1.32V
<b>Note!</b>			
[1] The greater the V <sub>CCDDO</sub> voltage, the higher the power consumption.			
[2] When V <sub>EFUSE</sub> is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies as the range of the power supply voltage, and then connect the power supply pins to the power supply at the same time.			

Title GOWIN Minimum System Diagram			
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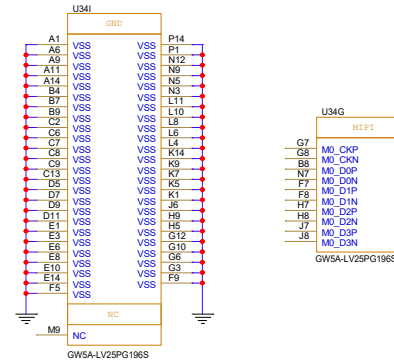
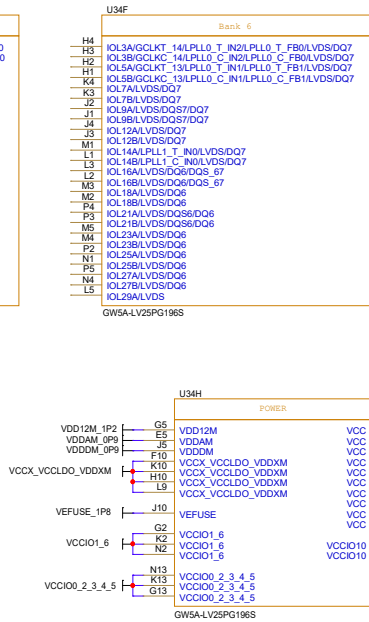
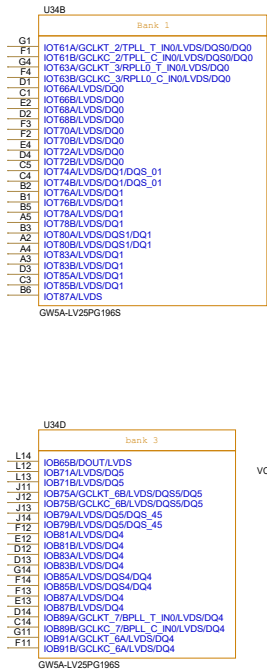
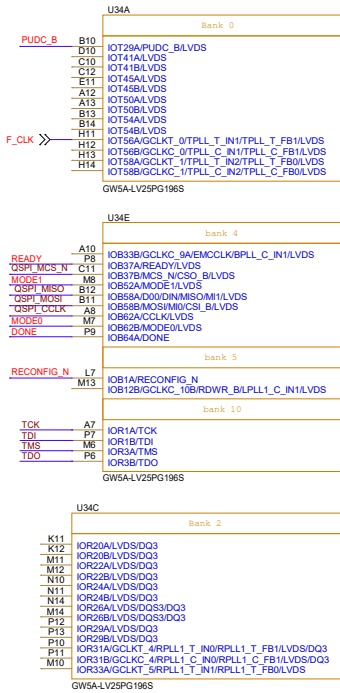


Notes:  
1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.  
2.External Flash memory is used to store downloaded programs.  
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .  
3.It is recommended that add an ESD protection chip to the JTAG download circuit.  
4.VCC core voltage requires a large current, so it is recommended to supply power separately.  
5.The MODE pin is the GowinCONFIG configuration mode selection signal.  
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.  
6.The MSPI signal levels must match the Flash power supply voltage.  
If the voltage of the MSPI Flash does not match the Flash power supply voltage, a level shifter is required for voltage translation.

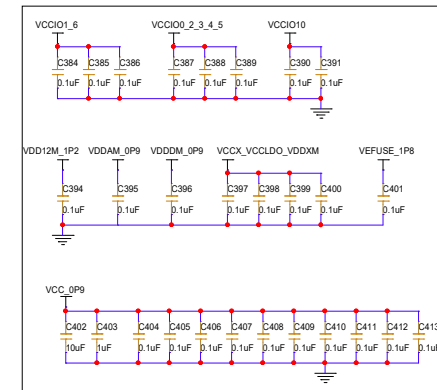
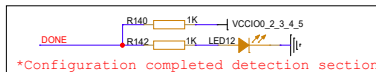
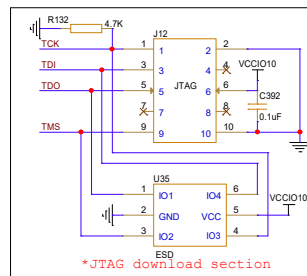
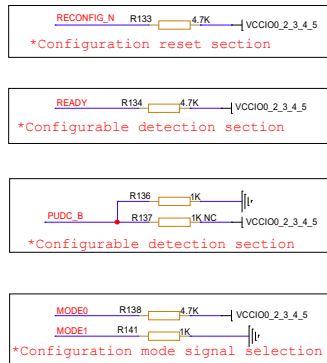
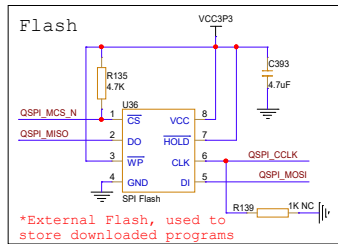
Name	Description	Min.	Max.
FPGA Logic			
V <sub>CC</sub>	Core voltage, LV	0.87V	1.03V
V <sub>CCIO</sub>	Core voltage, EV	1.14V	1.8V
V <sub>CCIO</sub>	I/O Bank voltage	1.14V	3.465V
V <sub>CCX</sub>	Auxiliary voltage	2.375	3.465V
V <sub>CCIO</sub> <sup>[1]</sup>	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V <sub>EFUSE</sub> <sup>[2]</sup>	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V <sub>DDAM</sub>	Analog core power supply voltage	0.87V	1V
V <sub>DDDM</sub>	Digital core power supply voltage	0.87V	1V
V <sub>DDDM</sub>	Analog auxiliary power supply voltage	2.375V	3.465V
V <sub>DD12M</sub>	MIPI LP power supply voltage	1.14V	1.32V
Note!			
[1] The greater the V <sub>CCIO</sub> voltage, the higher the power consumption.			
[2] When V <sub>EFUSE</sub> is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			

File			
GOWIN Minimum System Diagram			
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***GW5A-LV25PG196S***



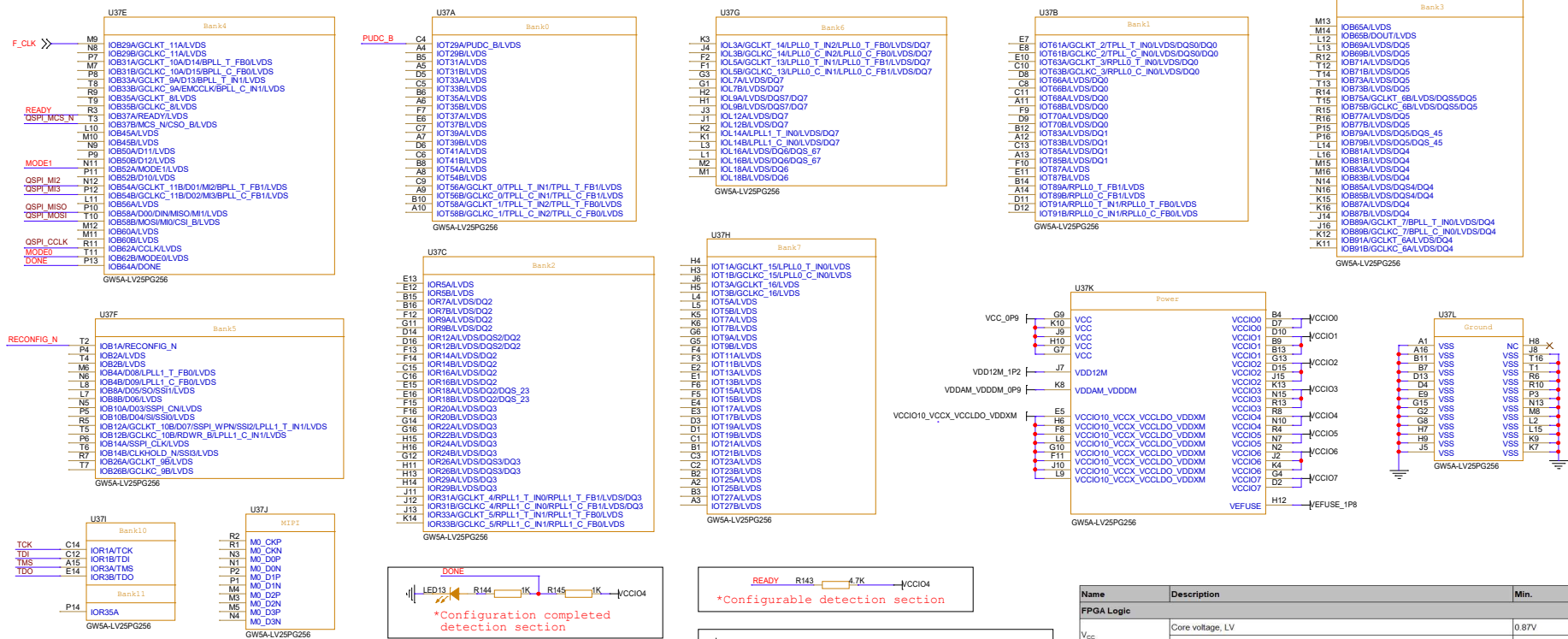
Name	Description	Min.	Max.
<b>FPGA Logic</b>			
V <sub>CC</sub>	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V <sub>CCIO</sub>	I/O Bank voltage	1.14V	3.465V
V <sub>CDK</sub>	Auxiliary voltage	2.375	3.465V
V <sub>CCDDO</sub> <sup>[1]</sup>	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V <sub>EFUSE</sub> <sup>[2]</sup>	Voltage required for eFuse writing	1.62V	1.98V
<b>MIP1</b>			
V <sub>DDM1</sub>	Analog core power supply voltage	0.87V	1V
V <sub>DDCM1</sub>	Digital core power supply voltage	0.87V	1V
V <sub>DDM1A</sub>	Analog auxiliary power supply voltage	2.375V	3.465V
V <sub>DD12M1</sub>	MIP1 LP power supply voltage	1.14V	1.32V
<b>Note:</b>			
[1] The greater the V <sub>CCDDO</sub> voltage, the higher the power consumption.			
[2] When V <sub>EFUSE</sub> is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			



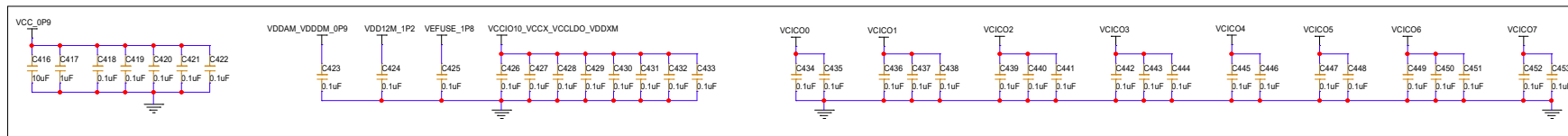
Notes:

- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.  
For details about SPI Flash Model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.  
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.  
If the voltage of the MSPI BANK does not match the Flash power supply voltage,  
a level shifter is required for voltage translation.

***GW5A-LV25PG256***



Name	Description	Min.	Max.
<b>FGPA Logic</b>			
V <sub>CC</sub>	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V <sub>CCIO</sub>	I/O Bank voltage	1.14V	3.465V
V <sub>CCA</sub>	Auxiliary voltage	2.375	3.465V
V <sub>CCDDO</sub> <sup>[1]</sup>	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V <sub>EFUSE</sub> <sup>[2]</sup>	Voltage required for eFuse writing	1.62V	1.98V
<b>MIPI</b>			
V <sub>CCDM1</sub>	Analog core power supply voltage	0.87V	1V
V <sub>CCDM</sub>	Digital core power supply voltage	0.87V	1V
V <sub>CCDM1</sub>	Analog auxiliary power supply voltage	2.375V	3.465V
V <sub>DDI2M1</sub>	MIPI LP power supply voltage	1.14V	1.32V
<b>Note!</b>			
[1] The greater the V <sub>CCDDO</sub> voltage, the higher the power consumption.			
[2] When V <sub>EFUSE</sub> is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			



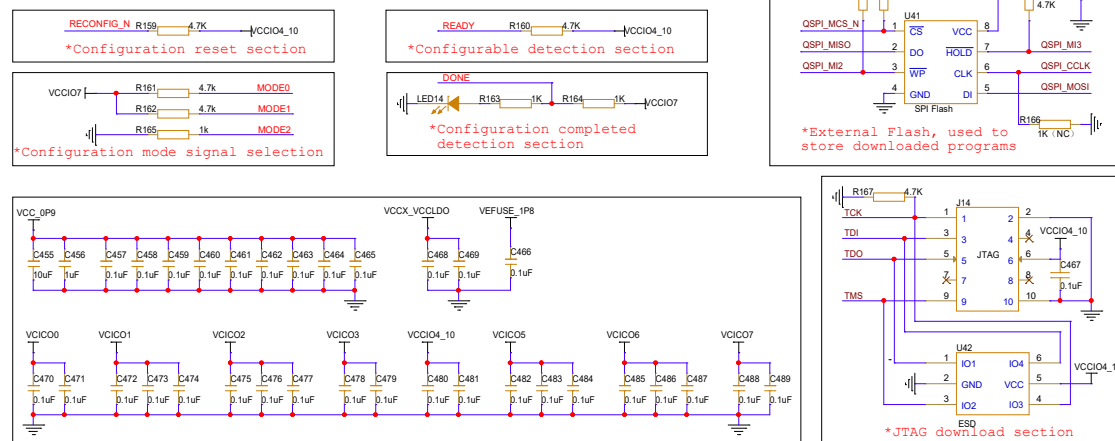
Notes:

- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.  
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.  
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.  
If the voltage of the MSPI BANK does not match the Flash power supply voltage,  
a level shifter is required for voltage translation.

Title				
GOWIN Minimum System Diagram				
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***GW5A-LV25PG256C***

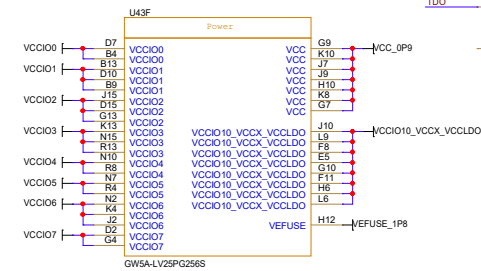
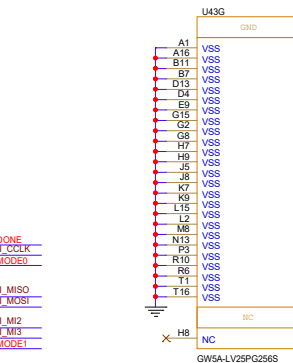
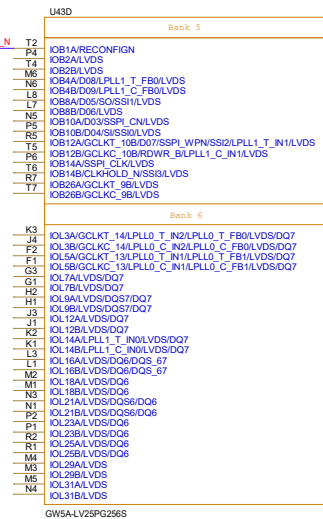
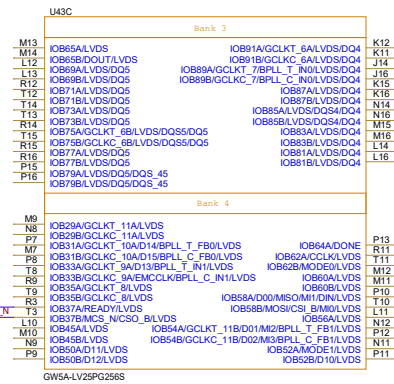
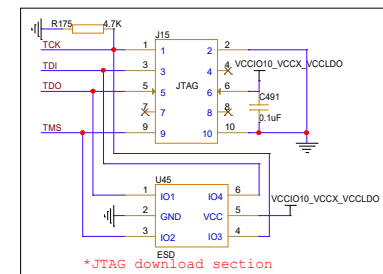
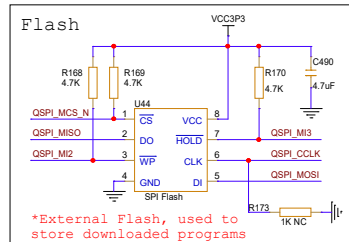
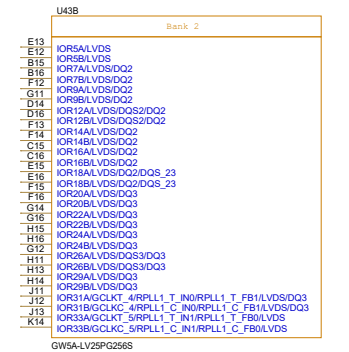
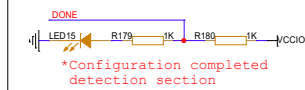
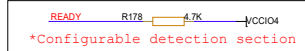
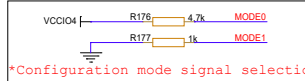
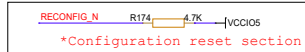
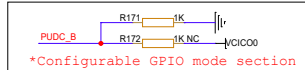


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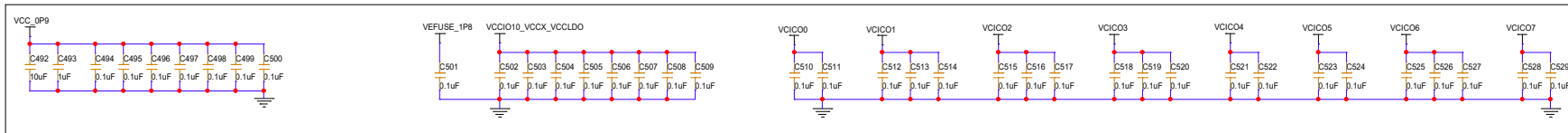
- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.  
For details about SPI Flash Model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.  
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.  
If the voltage of the MSPI BANK does not match the Flash power supply voltage,  
a level shifter is required for voltage translation.

Name	Description	Min.	Max.
<b>FPGA Logic</b>			
$V_{CC}$	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
$V_{CCIO}$	I/O Bank voltage	1.14V	3.465V
$V_{CCX}$	Auxiliary voltage	2.375	3.465V
$V_{CCDDO}^{(1)}$	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
$V_{EFUSE}^{(2)}$	Voltage required for eFuse writing	1.62V	1.96V
<b>MIPI</b>			
$V_{DDAM}$	Analog core power supply voltage	0.87V	1V
$V_{DDDM}$	Digital core power supply voltage	0.87V	1V
$V_{DDXM}$	Analog auxiliary power supply voltage	2.375V	3.465V
$V_{DD12M}$	MIPI LP power supply voltage	1.14V	1.32V
<b>Note!</b>			
<sup>(1)</sup> The greater the $V_{CCDDO}$ voltage, the higher the power consumption.			
<sup>(2)</sup> When $V_{EFUSE}$ is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			

***GW5A-LV25PG256S***



Name	Description	Min.	Max.
<b>FPGA Logic</b>			
$V_{CC}$	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
$V_{CCIO}$	I/O Bank voltage	1.14V	3.465V
$V_{DDK}$	Auxiliary voltage	2.375	3.465V
$V_{CCDDO}^{(1)}$	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
$V_{FUSE}^{(2)}$	Voltage required for eFuse writing	1.62V	1.98V
<b>MIPI</b>			
$V_{DDMI}$	Analog core power supply voltage	0.87V	1V
$V_{DDDM}$	Digital core power supply voltage	0.87V	1V
$V_{DDDM}$	Analog auxiliary power supply voltage	2.375V	3.465V
$V_{DD12M}$	MIPI LP power supply voltage	1.14V	1.32V
<b>Note!</b>			
<sup>(1)</sup> The greater the $V_{CCDDO}$ voltage, the higher the power consumption.			
<sup>(2)</sup> When $V_{FUSE}$ is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			

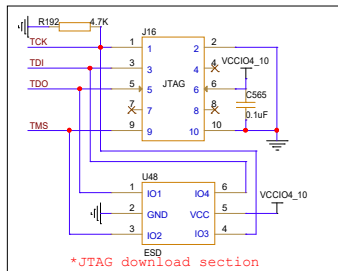
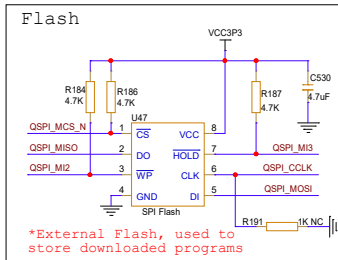
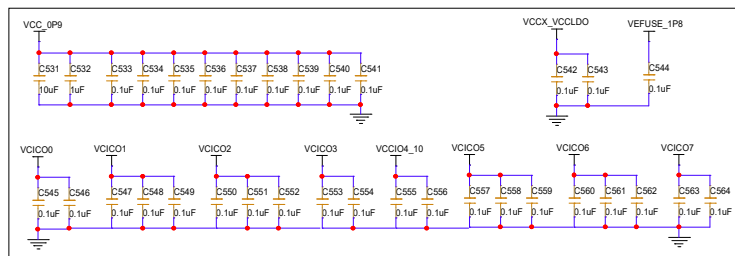
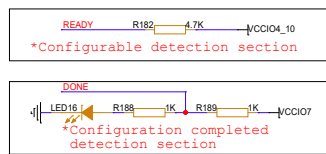
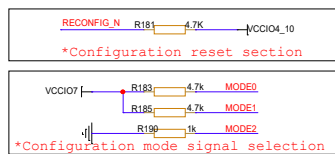
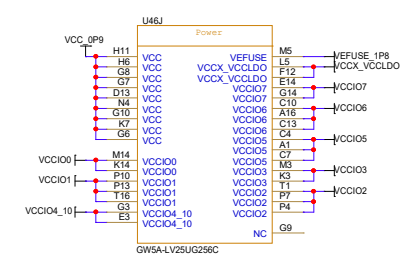
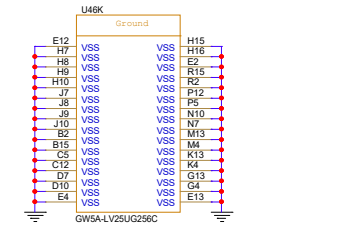
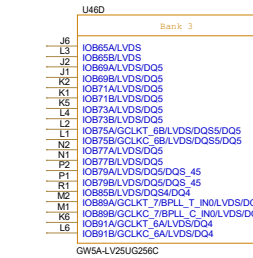
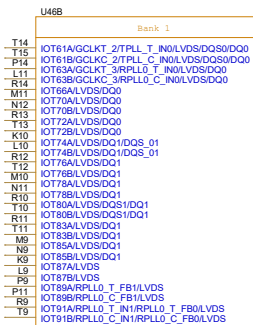
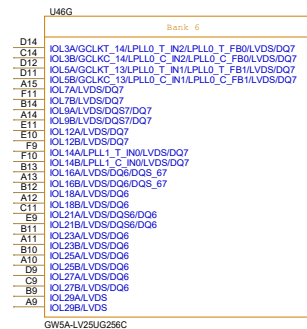
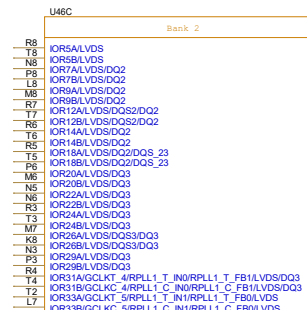
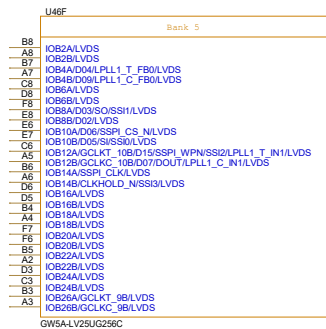
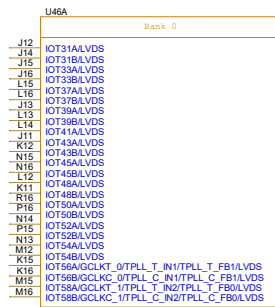
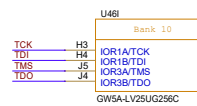
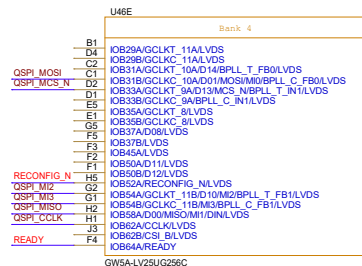
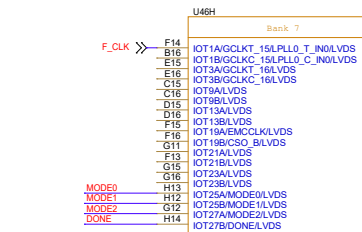


Notes:

- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.  
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.  
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 6.The MSPI signal levels must match the Flash power supply voltage.  
If the voltage of the MSPI BANK does not match the Flash power supply voltage,  
a level shifter is required for voltage translation.

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***GW5A-LV25UG256C***



Name	Description	Min.	Max.
<b>FPGA Logic</b>			
V <sub>CC</sub>	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V <sub>CCIO</sub>	I/O Bank voltage	1.14V	3.465V
V <sub>CCX</sub>	Auxiliary voltage	2.375	3.465V
V <sub>CC_LDO</sub> <sup>(1)</sup>	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V <sub>EFUSE</sub> <sup>(2)</sup>	Voltage required for eFUSE writing	1.62V	1.98V
<b>MIPI</b>			
V <sub>DDAM</sub>	Analog core power supply voltage	0.87V	1V
V <sub>DDCM</sub>	Digital core power supply voltage	0.87V	1V
V <sub>DDCMX</sub>	Analog auxiliary power supply voltage	2.375V	3.465V
V <sub>DD12M</sub>	MIPI LP power supply voltage	1.14V	1.32V

<sup>[1]</sup> The greater the  $V_{CCLDO}$  voltage, the higher the power consumption.

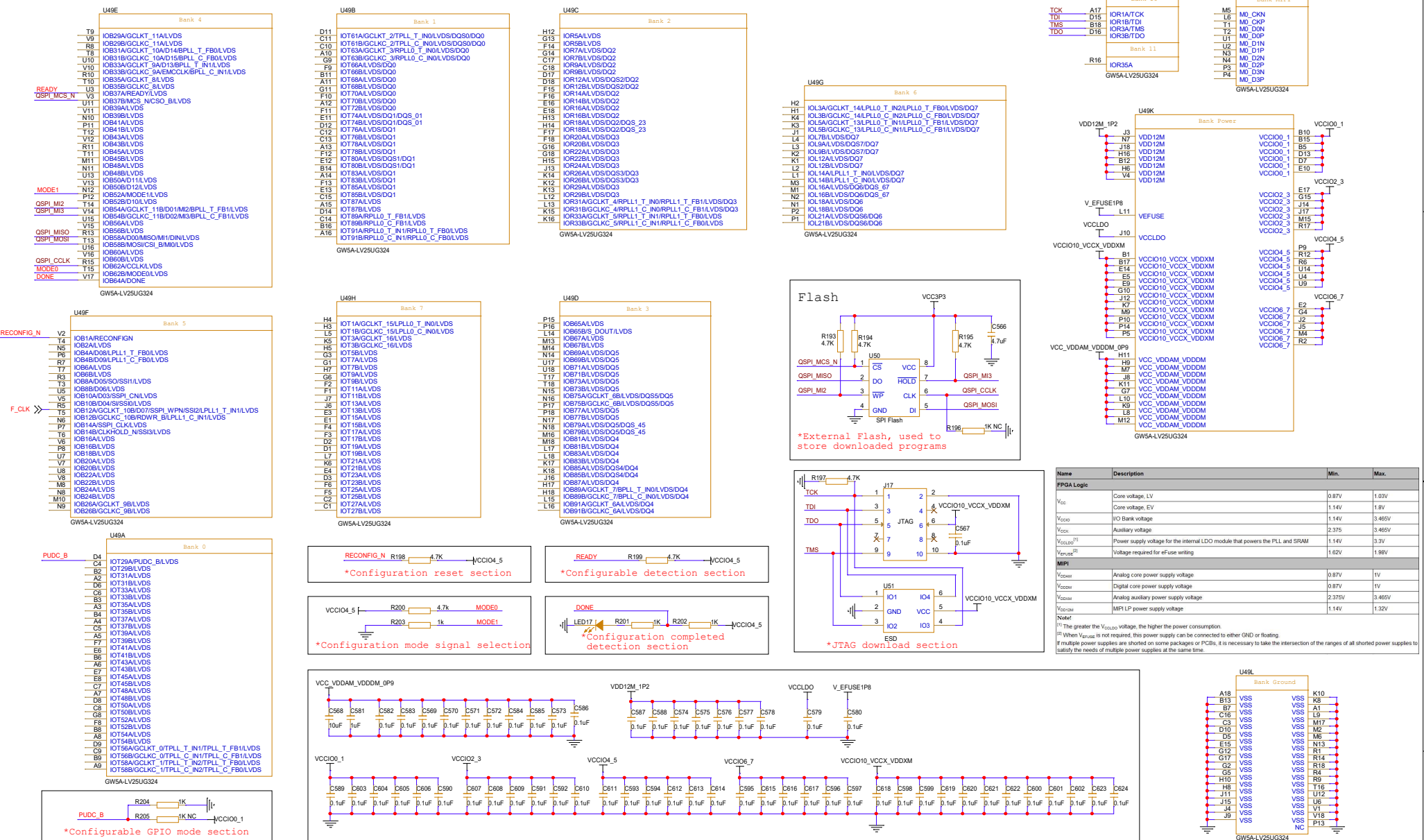
<sup>[2]</sup> When  $V_{EFUSE}$  is not required, this power supply can be connected to either GND or floating.

If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.

Notes:

- 1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.  
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit .
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.  
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 6.The MSPI signal levels must match the Flash power supply voltage.  
If the voltage of the MSPI BANK does not match the Flash power supply voltage,  
a level shifter is required for voltage translation.

***GW5A-LV25UG324***



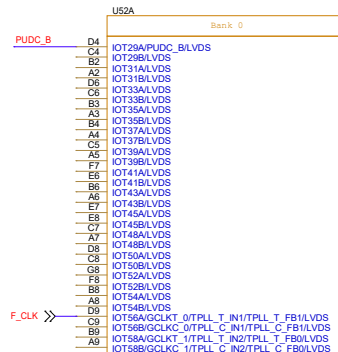
Notes:

1. F\_CLK signal is an external input clock signal.
- It is recommended that F\_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. VCC core voltage requires a large current, so it is recommended to supply power separately.
5. The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
6. The MSPI signal levels must match the Flash power supply voltage.
- If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

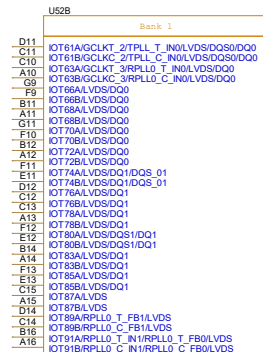
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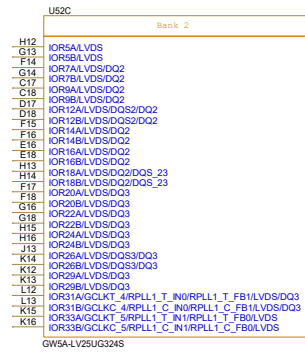
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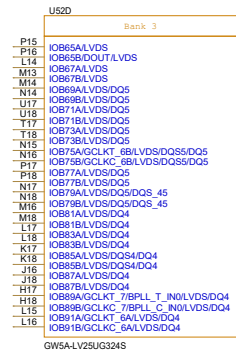
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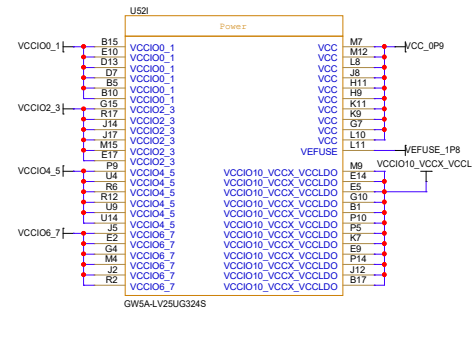
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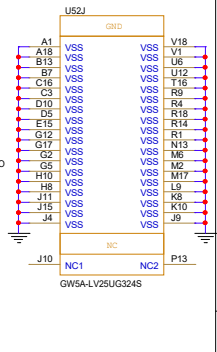
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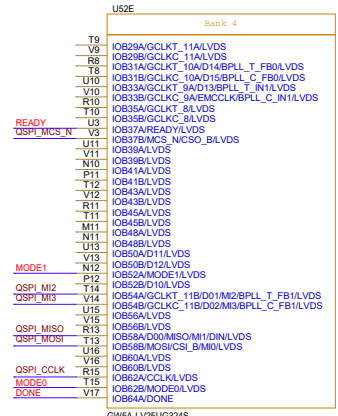
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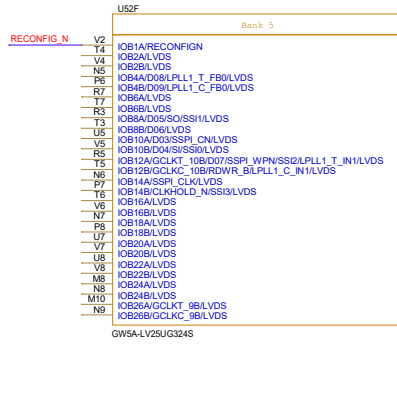
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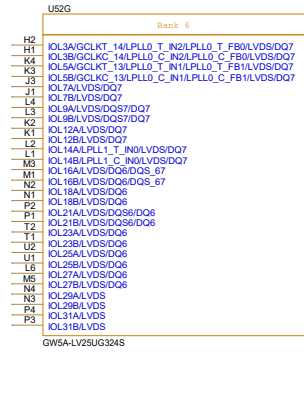
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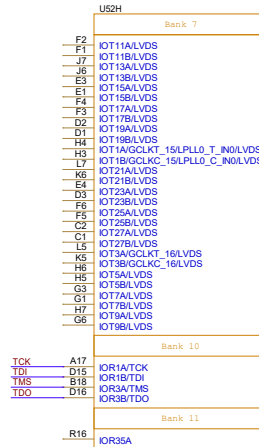
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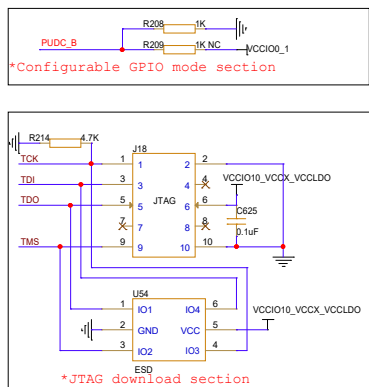
GW5A-LV25UG324S

Name	Description	Min.	Max.
<b>FPGA Logic</b>			
$V_{CC}$	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
$V_{CCIO}$	I/O Bank voltage	1.14V	3.465V
$V_{CCAUX}$	Auxiliary voltage	2.375	3.465V
$V_{CCLODIO}^{(1)}$	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
$V_{PUSE}^{(2)}$	Voltage required for eFuse writing	1.62V	1.98V
<b>MIPI</b>			
$V_{DDMI}$	Analog core power supply voltage	0.87V	1V
$V_{DDDM}$	Digital core power supply voltage	0.87V	1V
$V_{DDMI}$	Analog auxiliary power supply voltage	2.375V	3.465V
$V_{DD12MI}$	MIPI LP power supply voltage	1.14V	1.32V
<b>Note:</b>			
<sup>(1)</sup> The greater the $V_{CCLODIO}$ voltage, the higher the power consumption.			
<sup>(2)</sup> When $V_{PUSE}$ is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are needed on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			

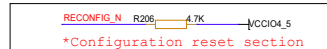
<sup>(1)</sup> The greater the  $V_{CCLOO}$  voltage, the higher the power consumption

[2] When  $V_{\text{REFUSE}}$  is not required, this power supply can be connected to either GND or floating.

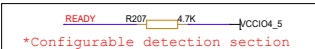
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.



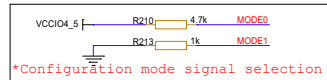
\*Configurable GPIO mode section



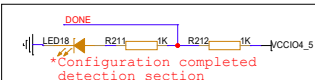
\*Configuration reset section



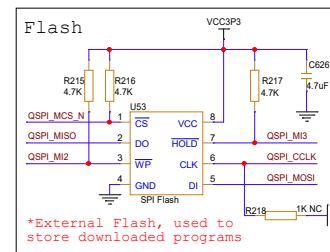
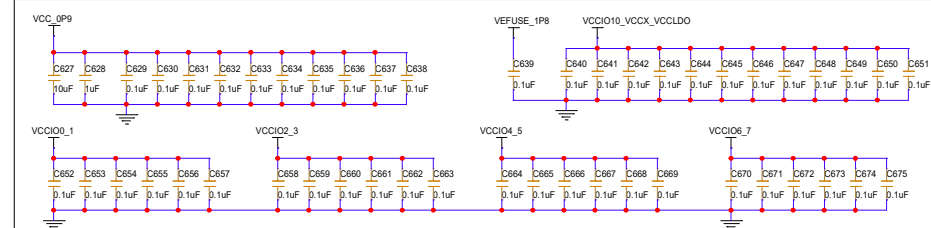
\*Configurable detection section



\*Configuration mode signal selection



\*Configuration completed  
detection section



\*External Flash, used to store downloaded programs

Notes:

- 1.F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.

For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in Arora V 25K FPGA Products Programming and Configuration Guide .

- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.

For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in Arora V 25K FPGA Products Programming and Configuration Guide.

- 6.The MSPI signal levels must match the Flash power supply voltage.

If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

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