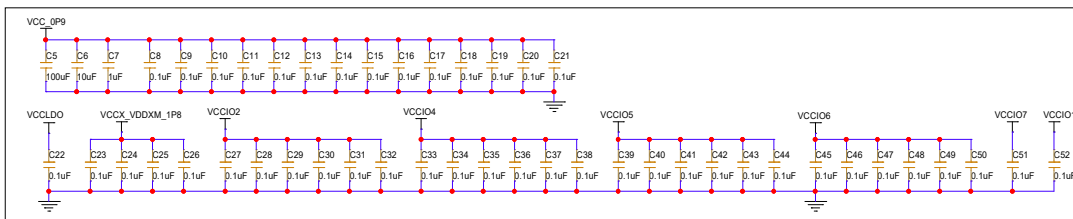
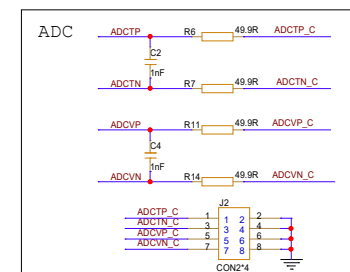
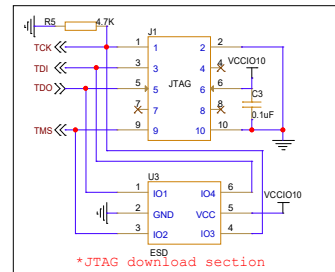
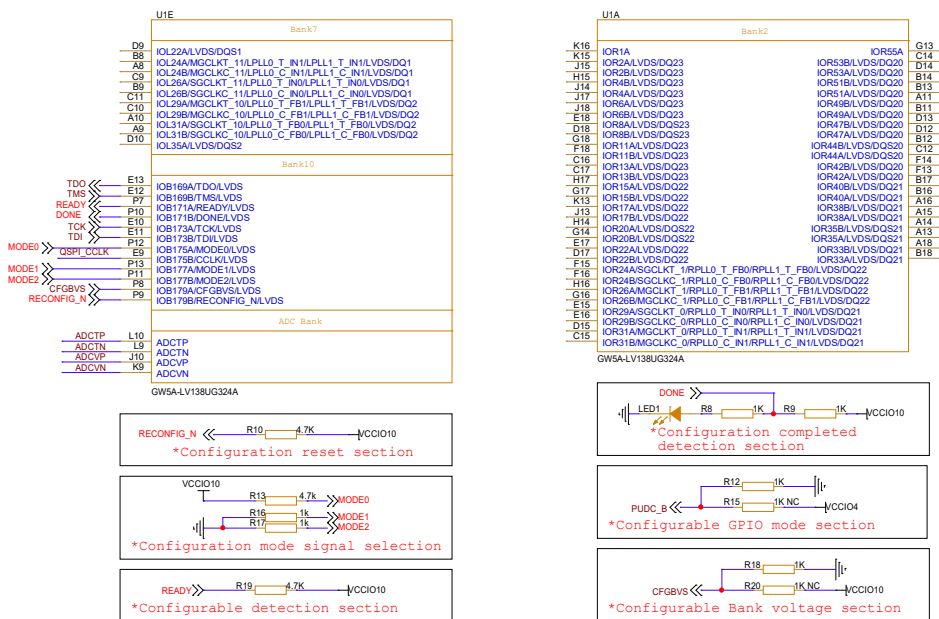
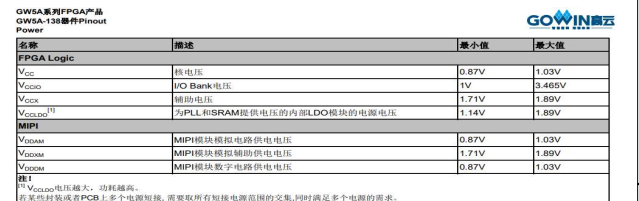
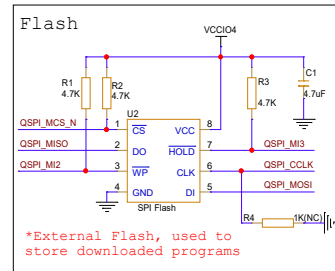
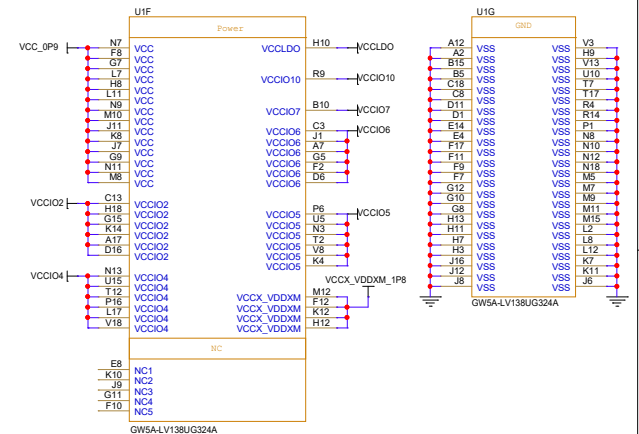
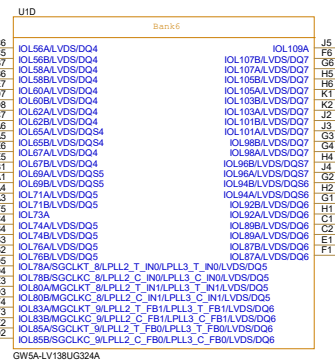
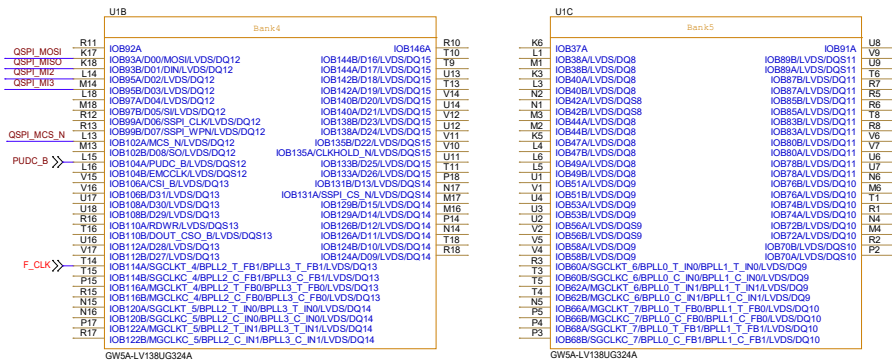


GW5A-LV138UG324A



CFGBVS	VCCIO (Bank4、Bank10)
1	2.5V and 3.3V
0	VCCIO≤1.8V

Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG704, Arora V FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, Arora V FPGA Products Programming and Configuration Guide.