



Gowin 10G Serial Ethernet IP

User Guide

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Revision History

| Date | Version | Description |
|------------|---------|--|
| 12/14/2023 | 1.0E | Initial version published. |
| 12/13/2024 | 1.1E | GW5AT-60 devices supported and related descriptions added. |
| 05/23/2025 | 1.2E | GW5AT-15 devices added. |

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1 About This Guide

1.1 Purpose

The purpose of Gowin 10G Serial Ethernet IP User Guide is to help you learn the features and usage of Gowin 10G Serial Ethernet IP by providing the descriptions of functions, GUI, and reference design, etc. The software screenshots and the supported products listed in this manual are based on Gowin Software V1.9.9. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI website. You can find the related documents at www.gowinsemi.com:

- [SUG100, Gowin Software User Guide](#)
- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1103, GW5A series of FPGA Products Data Sheet](#)
- [DS1239, GW5AST series of FPGA Products Data Sheet](#)
- [DS1105, GW5AS series of FPGA Products Data Sheet](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

| Terminology and Abbreviations | Meaning |
|-------------------------------|-------------------------------|
| AFE | Analog Front End |
| BER | Bit Error Rate |
| FFE | Feed-Forward Equalization |
| FPGA | Field Programmable Gate Array |
| IP | Intellectual Property |
| LUT | Look-up Table |
| MAC | Media Access Control |

| Terminology and Abbreviations | Meaning |
|-------------------------------|--|
| PCS | Physical Coding Sublayer |
| PMA | Physical Medium Attachment |
| SFP+ | Small Form-factor Pluggable Plus |
| XGMII | 10-Gigabit Media Independent Interface |

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

Gowin 10G Serial Ethernet IP implements the functions described in IEEE 802.3 standard Clause 49 for 10GBASE-R, providing the functions of the Physical Medium Attachment (PMA) and Physical Coding Sublayer (PCS). It offers users an XGMII (10-Gigabit Media Independent Interface) in accordance with IEEE 802.3 Clause 46 definition. This IP can be integrated into devices that comply with 10GBASE-R serial Ethernet, commonly used in communication applications.

Table 2-1 Gowin 10G Serial Ethernet IP

| Gowin 10G Serial Ethernet IP | |
|------------------------------|-----------------------------------|
| Logic Resource | See Table 2-2. |
| Delivered Doc. | |
| Design Files | Verilog (encryption) |
| Reference Design | Verilog |
| TestBench | Verilog |
| Test and Design Flow | |
| Synthesis Software | GowinSynthesis |
| Application Software | Gowin Software (V1.9.9 and above) |

Note!

For the devices supported, you can click [here](#) to get the information.

2.1 Features

- Supports IEEE802.3 Clause 49
- Supports 10GBASE-R PMA/PCS layer protocols
- Supports 10.3125Gbps
- Supports 64/66B decoding error block statistics (Only GW5AT-138/75 support this feature)
- Supports decoding error block statistics for 64/66B
- Supports serial data scrambling and descrambling
- Supports BER monitor (Only GW5AT-138/75 support this feature)
- Supports a user-side XGMII as defined by IEEE 802.3 Clause 46

- Supports RX clock elastic buffer

2.2 Operating Frequency

Gowin 10G Serial Ethernet IP operates internally at 161.2 MHz and 156.25 MHz, and the XGMII operates at 156.25 MHz.

2.3 Resource Utilization

Gowin 10G Serial Ethernet IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades. Taking Gowin GW5AT series of FPGA as an instance, the resource utilization is as shown in Table 2-2. GW5AT-60/GW5AT-15 devices directly use SerDes hardcore-related functions, consuming almost no logic resources. For the resource utilization of other devices, please refer to later release information.

Table 2-2 Resource Utilization

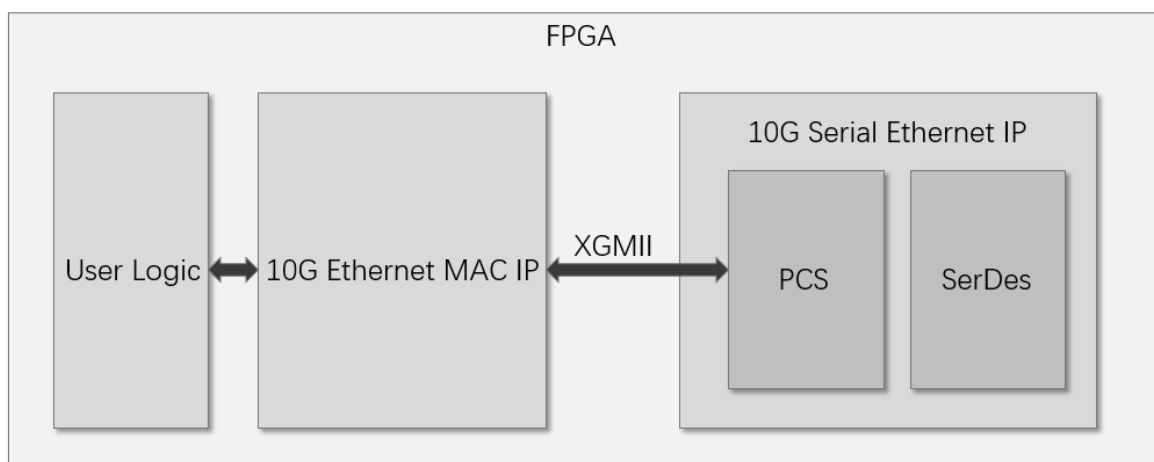
| Device | Resource Utilization | | Speed Grade |
|-----------------------|----------------------|------|-------------|
| GW5AT-138/75 | LUT | 4322 | C2/I1 |
| | REG | 3621 | |
| | BSRAM | 4 | |
| GW5AT-60/ GW5AT-15 | LUT | 3 | C2/I1 |
| | REG | 0 | |
| | BSRAM | 0 | |

3 Functional Description

3.1 Structure

The basic structure of Gowin 10G Serial Ethernet IP is shown in Figure 3-1, mainly including SerDes and PCS modules. 10G Serial Ethernet IP calls SerDes hardcore as the PMA of the protocol. Simultaneously, the IP implements the 10GBASE-R PCS protocol, providing users with an XGMII. Users can call Gowin 10G Ethernet MAC IP to interface with XGMII to implement a 10G Ethernet solution. Alternatively, they can independently design a 10G Ethernet MAC and interface it with the XGMII. The User Logic in the figure refers to the User Design in the FPGA. Externally, the FPGA can communicate with other devices using an SFP+ module.

Figure 3-1 Block Diagram of Gowin 10G Serial Ethernet IP



3.2 User Interface

3.2.1 Reset

GW5AT-138/75

The IP supports separate resets for RX and TX. rx_rstn_i is the asynchronous reset input for the RX, and tx_rstn_i is the asynchronous reset input for the TX. Both of these asynchronous reset signals are active low. The descriptions of reset signals are shown in Table 4-1.

GW5AT-60/15

No reset input control.

3.2.2 Clock

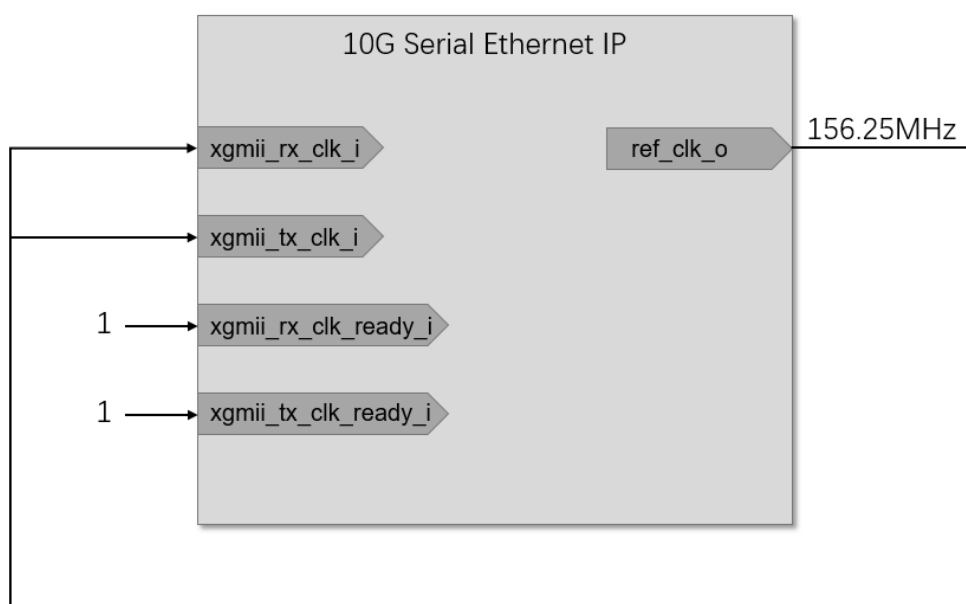
Users need to provide clocks and indicator signals that meet the requirements for the IP to ensure the correct operation of the IP. The descriptions of clock signals are shown in Table 4-1.

The clock is a crucial condition for the normal operation of the IP. The recommended clock connection is as follows:

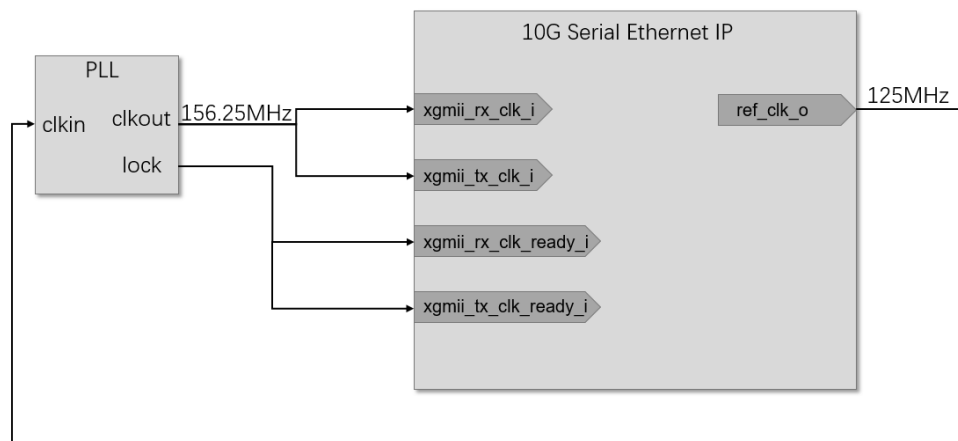
GW5AT-138/75**SerDes input reference clock with 156.25 MHz**

As shown in Figure 3-2, the ref_clk_o clock is the SerDes input reference clock with 156.25MHz. This output clock can be directly connected to xgmii_rx_clk_i and xgmii_tx_clk_i. xgmii_rx_clk_ready_i and xgmii_tx_clk_ready_i should be assigned constant value of 1.

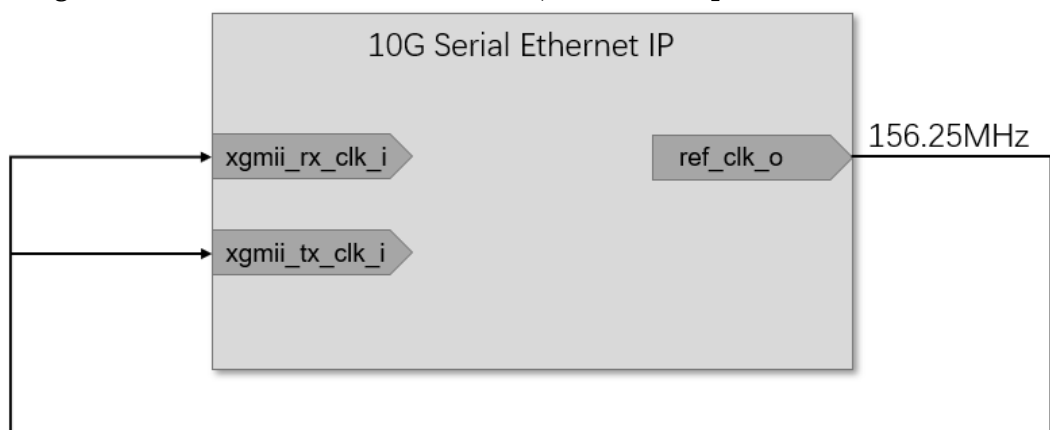
Figure 3-2 Clock Connection Reference (ref_clk_o outputs a clock with 156.25MHz)

**SerDes input reference clock is non-156.25 MHz, and take 125MHz as an example.**

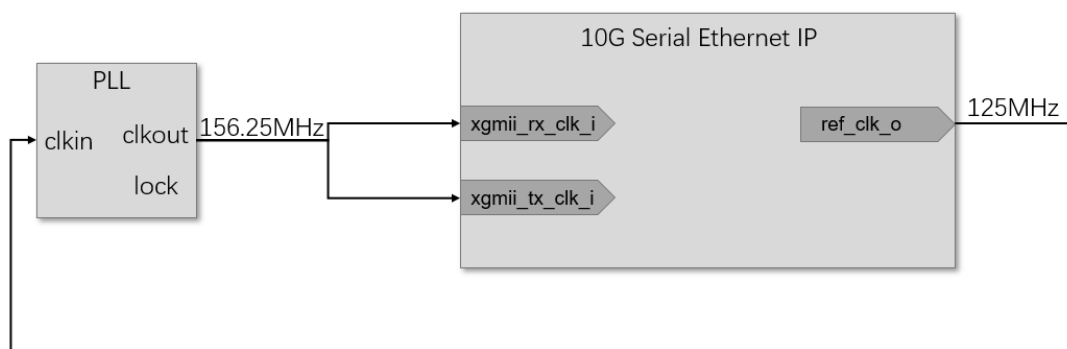
As shown in Figure 3-3, the ref_clk_o clock is SerDes input reference clock with 125 MHz. This output clock can generate a 156.25 MHz clock through a PLL, which is then used as the input for xgmii_rx_clk_i and xgmii_tx_clk_i. Both xgmii_rx_clk_ready_i and xgmii_tx_clk_ready_i should be connected to the PLL LOCK signal.

Figure 3-3 Clock Connection Reference (ref_clk_o outputs a clock with 125MHz)**GW5AT-60/15****SerDes input reference clock with 156.25 MHz**

As shown Figure 3-4, the ref_clk_o output clock is the SerDes input reference clock with 156.25 MHz. This output clock can be directly connected to xgmii_rx_clk_i and xgmii_tx_clk_i.

Figure 3-4 Clock Connection Reference (ref_clk_o outputs a clock with 156.25MHz)**SerDes input reference clock is non-156.25 MHz, and take 125MHz as an example.**

As shown in Figure 3-5, the ref_clk_o output clock is the SerDes input reference clock with 125 MHz. This output clock needs to be passed through a PLL to generate a 156.25 MHz clock, which serves as the input for xgmii_rx_clk_i and xgmii_tx_clk_i

Figure 3-5 Clock Connection Reference (ref_clk_o outputs a clock with 125MHz)

3.2.3 XGMII

The IP provides users XGMII as defined by IEEE 802.3 Clause 46. The descriptions of the XGMII signals are as shown in Table 4-1. The XGMII encoding format can be found in IEEE 802.3 Clause 46.

The IP provides a 64-bit XGMII for the user, sampled at the rising edge of its synchronous clock. In contrast, the XGMII defined by IEEE 802.3 Clause 46 is 32-bit and sampled at the dual edges of the clock. The correspondence between the two is shown in Table 3-1.

Table 3-1 Correspondence between IEEE802.3 XGMII and the IP

| IEEE802.3 XGMII | | IP XGMII |
|-------------------------|-------------------|------------------------------------|
| Samples at rising edge | TXC[0]/TXD[7:0] | xgmii_txc_i[0]/ xgmii_txd_i[7:0] |
| Samples at rising edge | TXC[1]/TXD[15:8] | xgmii_txc_i[1]/ xgmii_txd_i[15:8] |
| Samples at rising edge | TXC[2]/TXD[23:16] | xgmii_txc_i[2]/ xgmii_txd_i[23:16] |
| Samples at rising edge | TXC[3]/TXD[31:24] | xgmii_txc_i[3]/ xgmii_txd_i[31:24] |
| Samples at rising edge | TXC[0]/TXD[7:0] | xgmii_txc_i[4]/ xgmii_txd_i[39:32] |
| Samples at falling edge | TXC[1]/TXD[15:8] | xgmii_txc_i[5]/ xgmii_txd_i[47:40] |
| Samples at falling edge | TXC[2]/TXD[23:16] | xgmii_txc_i[6]/ xgmii_txd_i[55:48] |
| Samples at falling edge | TXC[3]/TXD[31:24] | xgmii_txc_i[7]/ xgmii_txd_i[63:56] |
| Samples at rising edge | RXC[0]/RXD[7:0] | xgmii_rxc_o[0]/ xgmii_rxd_o[7:0] |
| Samples at rising edge | RXC[1]/RXD[15:8] | xgmii_rxc_o[1]/ xgmii_rxd_o[15:8] |
| Samples at rising edge | RXC[2]/RXD[23:16] | xgmii_rxc_o[2]/ xgmii_rxd_o[23:16] |
| Samples at rising edge | RXC[3]/RXD[31:24] | xgmii_rxc_o[3]/ xgmii_rxd_o[31:24] |
| Samples at falling edge | RXC[0]/RXD[7:0] | xgmii_rxc_o[4]/ xgmii_rxd_o[39:32] |
| Samples at falling edge | RXC[1]/RXD[15:8] | xgmii_rxc_o[5]/ xgmii_rxd_o[47:40] |
| Samples at falling edge | RXC[2]/RXD[23:16] | xgmii_rxc_o[6]/ xgmii_rxd_o[55:48] |
| Samples at falling edge | RXC[3]/RXD[31:24] | xgmii_rxc_o[7]/ xgmii_rxd_o[63:56] |

3.2.4 Status Interface

Table 4-1 lists the IP status output interface. Users can utilize such interfaces to monitor the internal and link status of the IP.

3.2.5 Debug Interface

The IP provides a set of Debug interfaces for users, as shown in Table

4-1.

3.3 AFE (Analog Front End)

AFE means the analog front-end, and the operating speed of Gowin 10G Serial Ethernet IP is 10.3125Gbps. Users can configure the analog parameters of the IP through the interface to ensure signal integrity.

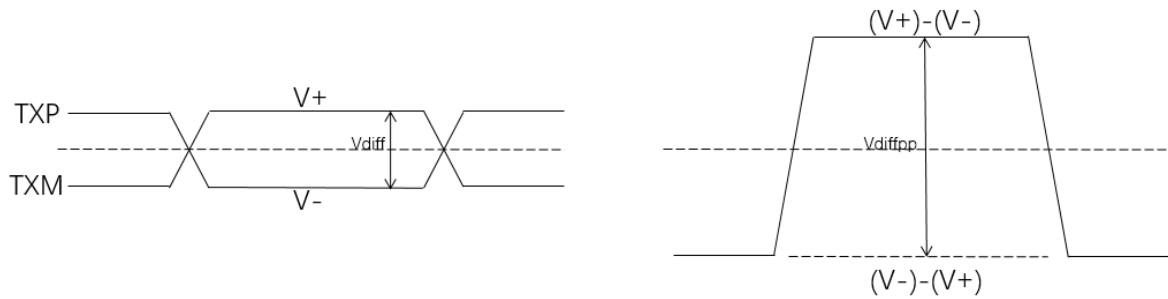
3.3.1 Transmit

On the transmit side, users can configure the differential swing and FFE (Feed-Forward Equalization) parameters of the IP.

Transmit Differential Swing

As shown in Figure 3-6, the differential voltage of the TX signal is $V_{diff} = (V+) - (V-)$, and the differential signal swing is $V_{diffpp} = 2 \times V_{diff}$. Users can configure V_{diffpp} through the interface, with a range of 180mV to 900mV.

Figure 3-6 Transmit Differential Signal Swing V_{diffpp}



TX FFE

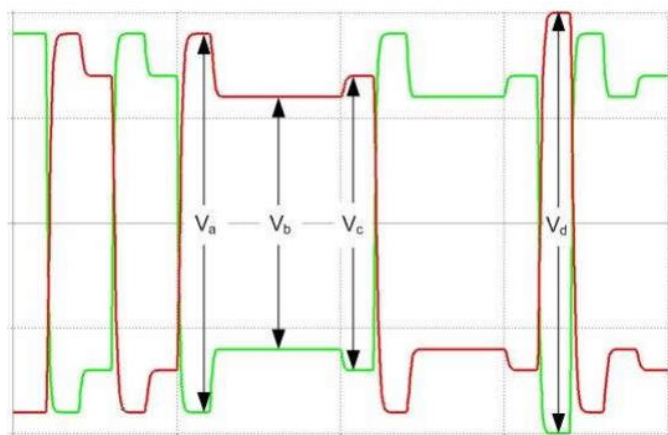
FFE stands for Feed-Forward Equalization. The IP supports automatic and manual adjustment of the TX FFE coefficients. When the user configures the FFE Mode as Auto, the IP automatically adjusts the FFE coefficients based on the hardware environment, and in this case, the configuration of C_m , C_0 , and C_1 is invalid. When the user configures the FFE Mode as Manual, he can manually adjust the 3-tap coefficients to configure the pre-emphasis of the TX signal.

As shown in Figure 3-7, when the user configures the FFE Mode as Manual, he can adjust the values of C_m , C_0 , and C_1 to modify the voltage amplitudes of V_a , V_b , and V_c . The calculation formula is as follows:

$$V_a = V_{diffpp} * (-C_m + C_0 + C_1) / 40$$

$$V_b = V_{diffpp} * (-C_m + C_0 - C_1) / 40$$

$$V_c = V_{diffpp} * (C_m + C_0 - C_1) / 40$$

Figure 3-7 Voltage Definition for FFE TX

3.3.2 Receive

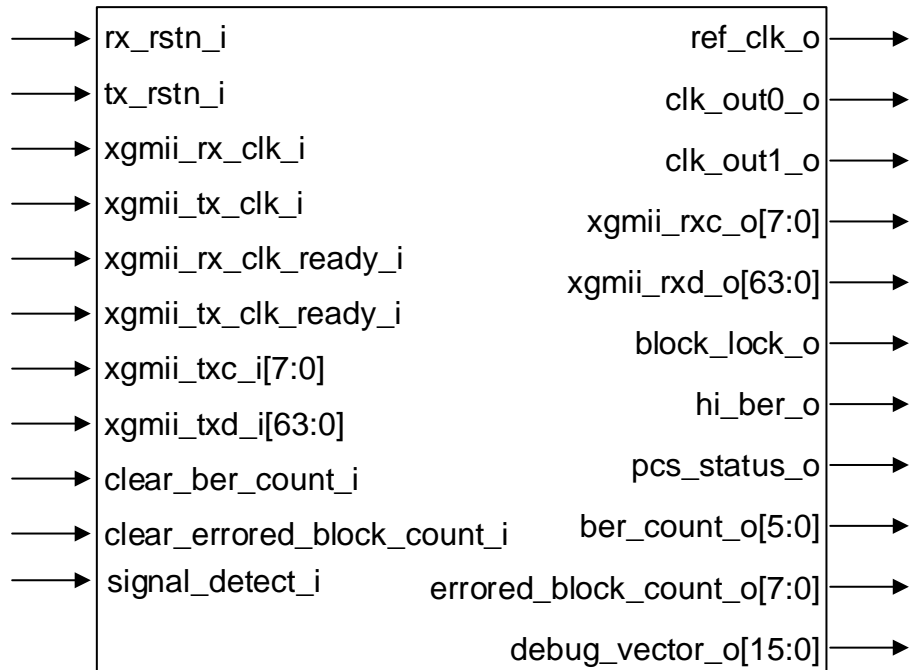
Receive Differential Signal Threshold

Users can configure the SD Threshold to adjust the voltage threshold for the RX signal. When the received differential signal is greater than the SD Threshold, the SerDes determines that valid data has been received. When the received differential signal is less than the SD Threshold, the SerDes determines that valid data has not been received, and it enters the Electrical Idle state.

4 Port List

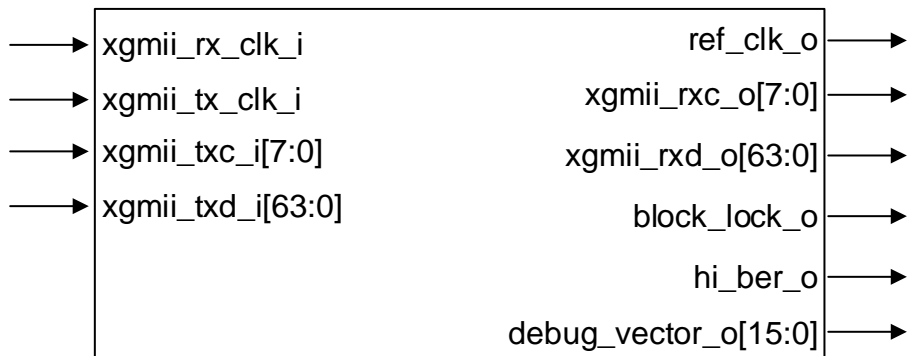
For GW5AT-138/75 devices, the I/O port of Gowin 10G Serial Ethernet IP is shown in Figure 4-1.

Figure 4-1 I/O Port Diagram of Gowin 10G Serial Ethernet IP (GW5AT-138/75)



For GW5AT-60/15 devices, the I/O port of Gowin 10G Serial Ethernet IP is shown in Figure 4-2.

Figure 4-2 I/O Port Diagram of Gowin 10G Serial Ethernet IP (GW5AT-60)



For the IO descriptions of Gowin 10G Serial Ethernet IP, you can see Table 4-1.

Table 4-1 IO Port List of Gowin 10G Serial Ethernet IP

| Signal | I/O | Data Width | Description |
|-------------------------|--------|------------|---|
| Signal Detection | | | |
| signal_detect_i | input | 1 | Input signal valid detection, which can be connected to the LOS pin of SFP+ module. 1: Input signal valid 0: Input signal invalid This signal is only available for GW5AT-138/75. |
| Reset | | | |
| rx_rstn_i | input | 1 | Asynchronous reset input for RX, active-low. This signal is only available for GW5AT-138/75. |
| tx_rstn_i | input | 1 | Asynchronous reset input for TX, active-low. This signal is only available for GW5AT-138/75. |
| Clock input | | | |
| xgmii_rx_clk_i | input | 1 | XGMII RX clock with a frequency of 156.25MHz. This clock can either share the same source with xgmii_tx_clk_i or can be an independent clock. |
| xgmii_tx_clk_i | input | 1 | XGMII TX clock with a frequency of 156.25MHz. This clock must be related to the frequency of the output clock ref_clk_o. |
| xgmii_rx_clk_ready_i | input | 1 | xgmii_rx_clk_i ready indicator. When the xgmii_rx_clk_i clock is not ready, it should be input 0; once the xgmii_rx_clk_i clock is ready, it should be input 1. This signal is only available for GW5AT-138/75. |
| xgmii_tx_clk_ready_i | input | 1 | xgmii_tx_clk_i ready indicator. When the xgmii_tx_clk_i clock is not ready, it should be input 0; once the xgmii_tx_clk_i clock is ready, it should be input 1. This signal is only available for GW5AT-138/75. |
| Clock Output | | | |
| ref_clk_o | output | 1 | This signal is directly output to provide the reference clock for SerDes, and its frequency is consistent |

| Signal | I/O | Data Width | Description |
|-----------------------------|--------|------------|--|
| | | | with SerDes input reference clock. |
| clk_out0_o | output | 1 | The internal clock output for the IP, operating at a frequency of 162MHz under normal conditions. This signal is only available for GW5AT-138/75. |
| clk_out1_o | output | 1 | The internal clock output for the IP, operating at a frequency of 162MHz under normal conditions. This signal is only available for GW5AT-138/75. |
| XGMII Interface | | | |
| xgmii_txc_i | input | 8 | XGMII TX control word, 8 bits, synchronized with xgmii_tx_clk_i |
| xgmii_txd_i | input | 64 | XGMII TX data, 64 bits, synchronized with xgmii_tx_clk_i |
| xgmii_rxc_o | output | 8 | XGMII RX control word, 8 bits, synchronized with xgmii_rx_clk_i |
| xgmii_rxd_o | output | 64 | XGMII RX Data, 64 bits, synchronized with xgmii_rx_clk_i |
| IP Status | | | |
| block_lock_o | output | 1 | Block RX lock indicator, synchronized with clk_out0_o 1: Locked 0: Unlocked |
| hi_ber_o | output | 1 | Hi BER RX indicator, synchronized with clk_out0_o |
| pcs_status_o | output | 1 | PCS status indicator, synchronized with clk_out0_o 1: Normal 0: Abnormal This signal is only available for GW5AT-138/75. |
| clear_ber_count_i | input | | Clear BER count, active-high, synchronized with clk_out0_o. This signal is only available for GW5AT-138/75. |
| ber_count_o | output | 6 | BER count with maximum 63; stop counting after reaching 63, synchronized with clk_out0_o. This signal is only available for GW5AT-138/75. |
| clear_errored_block_count_i | input | | Clear Error Block count, active-high, synchronized with clk_out0_o. This signal is only available for GW5AT-138/75. |
| errored_block_count_o | output | 8 | Error Block count with maximum 255; stop counting after reaching 255, synchronized with clk_out0_o. This signal is only available for GW5AT-138/75. |
| Debug Interface | | | |
| debug_vector_o | output | 16 | <ul style="list-style-type: none"> If the device is GW5AT-138/75, then [0]: SerDes PLL lock indicator 1: Locked 0: Unlocked |

| Signal | I/O | Data Width | Description |
|--------|-----|------------|---|
| | | | <p>[1]: SerDes RX CDR lock indicator</p> <p>1: Locked</p> <p>0: Unlocked</p> <p>[2]: SerDes RX valid signal detection indicator</p> <p>1: Valid</p> <p>0: Invalid</p> <p>[3]: Indicator for RX elastic Buffer deleting IDLE, synchronized with clk_out0_o.</p> <p>1: Perform one IDLE deletion operation</p> <p>0: No IDLE deletion operation</p> <p>[4]: Indicator for RX elastic Buffer deleting SEQUENCE, synchronized with clk_out0_o.</p> <p>1: Perform one SEQUENCE deletion operation</p> <p>0: No SEQUENCE deletion operation</p> <p>[5]: Indicator for RX elastic inserting IDLE, synchronized with xgmii_rx_clk_i.</p> <p>1: Perform one IDLE inserting operation</p> <p>0: No IDLE inserting operation</p> <p>[6]: Indicator for RX elastic Buffer overflow error, synchronized with clk_out0_o.</p> <p>1: Error</p> <p>0: Normal</p> <p>[7]: Indicator for RX elastic underflow error, synchronized with xgmii_rx_clk_i.</p> <p>1: Error</p> <p>0: Normal</p> <p>[8]: RX gearbox bit slip indicator, synchronized with clk_out0_o.</p> <p>1: Perform one bit slip operation</p> <p>0: No bit slip operation</p> <p>[15:9]: Reserved</p> <ul style="list-style-type: none"> ● If the device is GW5AT-60, then <p>[0]: SerDes PLL lock indicator</p> <p>1: Locked</p> <p>0: Unlocked</p> <p>[1]: SerDes RX CDR lock indicator</p> <p>1: Locked</p> <p>0: Unlocked</p> <p>[2]: SerDes RX valid signal detection indicator</p> |

| Signal | I/O | Data Width | Description |
|--------|-----|------------|--|
| | | | 1: Valid 0: Invalid [3]: Indicator for RX elastic Buffer deleting IDLE/SEQUENCE 1: Perform one IDLE deletion operation 0: No deletion operation [4]: Reserved [5]: Indicator for RX elastic inserting IDLE 1: Perform one IDLE inserting operation 0: No IDLE inserting operation [6]: Reserved [7]: Reserved [8]: Reserved [9]: Indicator for RX invalid header 1: Invalid header received 0: No invalid header received [15:10]: Reserved |

5 Parameter Configuration

You can configure the static parameters of Gowin 10G Serial Ethernet IP according to the design requirements, as shown in Table 5-1.

Table 5-1 Static Parameters of Gowin 10G Serial Ethernet IP

| Name | Description | Option |
|---------------------------|-----------------------------------|--|
| PHY Configuration | | |
| Channel Selection | Lane selection | Q0 lane 0, Q0 lane 1, Q0 lane 2, Q0 lane 3, Q1 lane 0, Q1 lane 1, Q1 lane 2, Q1 lane 3 |
| Loopback Mode | Loopback mode selection | OFF, LB_NES, LB_FES, LB_ENC |
| Line Rate | Lane Rate | 10.3125Gbps |
| Reference Clock Source | Reference clock source selection | Q0 REFCLK0, Q0 REFCLK1, Q1 REFCLK0, Q1 REFCLK1 |
| Reference Clock Frequency | Reference clock frequency setting | 125MHz, 156.25 MHz, 312.5 MHz, 625 MHz |
| PLL Selection | PLL selection | QPLL0, QPLL1, CPLL |
| AFE | | |
| Differential Swing | 100mV~900mV | Configure the swing of the differential signal V_{diffpp} , where $V_{diffpp} = 2 \times V_{diff}$ |
| FFE Mode | Auto Manual | Configure TX FFE mode Auto: Auto mode Manual: Manual mode |
| Cm | 0~19 | Transmit FFE pre-cursor |
| C0 | 21~40 | Transmit FFE main-cursor |
| C1 | 0~19 | Transmit FFE post-cursor |
| SD Threshold | 25mV~200mV | SD threshold for RX differential signal |

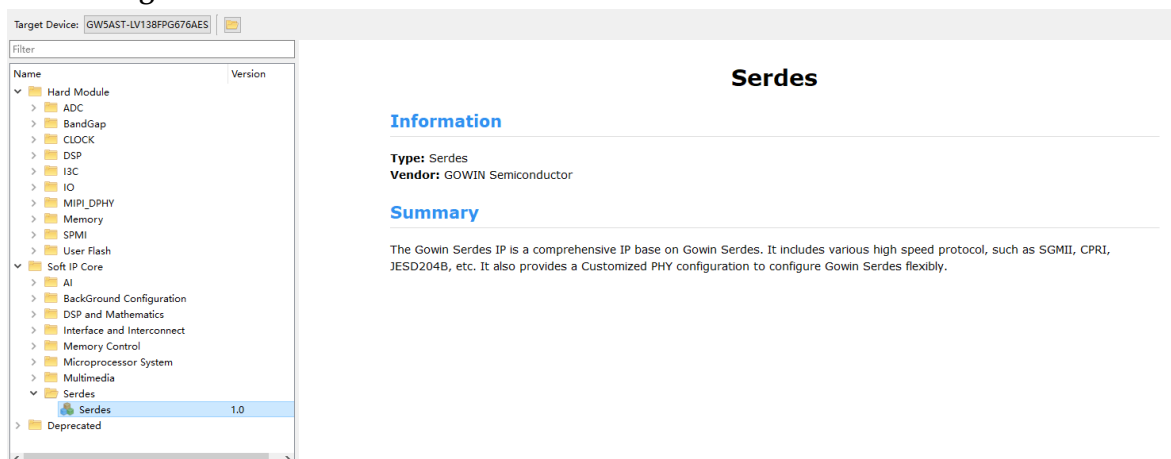
6 Interface Configuration

You can invoke and configure Gowin 10G Serial Ethernet IP using the IP Core Generator tool in the IDE.

1. Open IP Core Generator.

After creating the project, click the "Tools" tab in the upper left, click "IP Core Generator" to open Gowin IP Core Generator via the drop-down list, as shown in Figure 6-1.

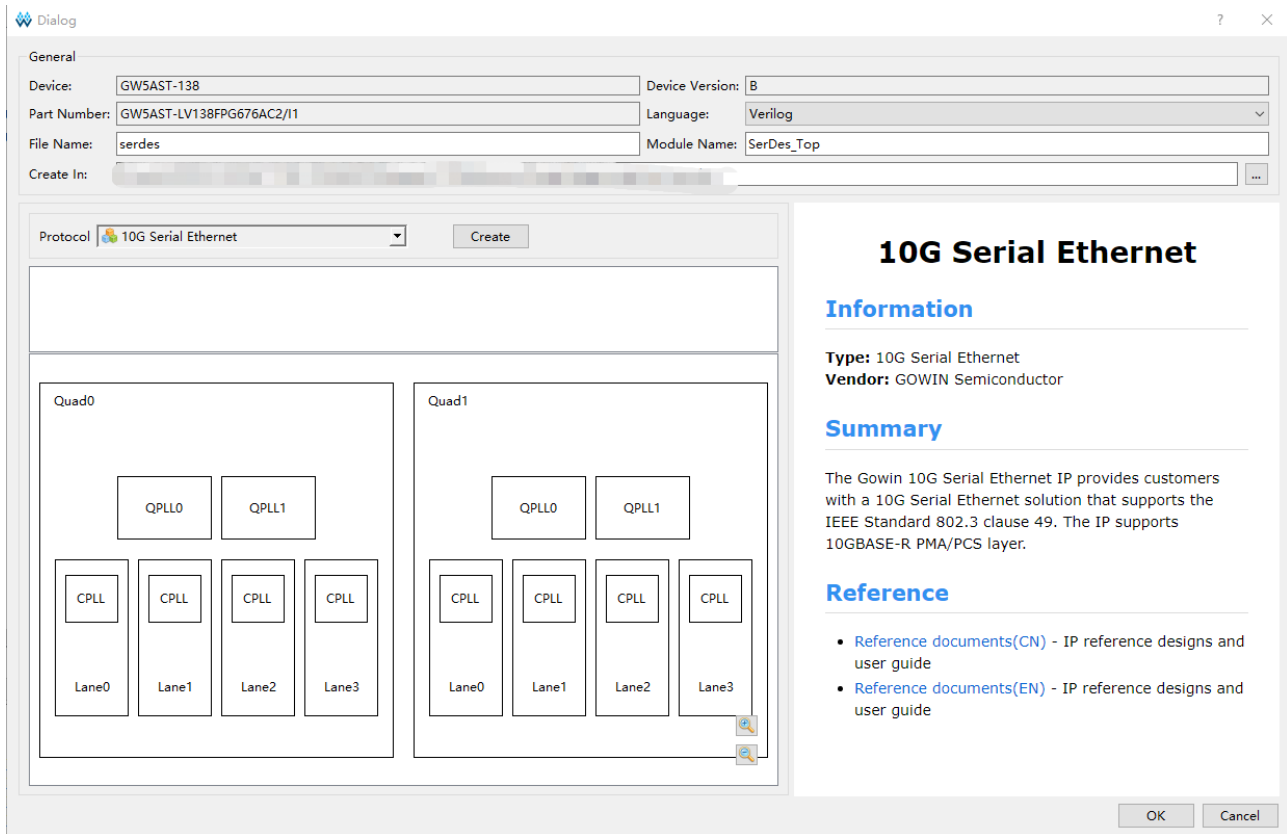
Figure 6-1 IP Core Generator



2. Open SerDes IP Configuration Interface.

Select "SerDes" in IP Core Generator and open SerDes IP configuration interface, as shown in Figure 6-2.

Figure 6-2 SerDes IP Configuration Interface



First configure "General" tab in the SerDes IP interface.

- Device, Device Version, Part Number: Used to set part number, and it is determined by the current project; and the user can not set it.
- Language: Support Verilog and VHDL, and you can choose the language as requirements, and the default is Verilog.
- File Name, Module Name, Create In: SerDes file name, module name and the generated file path settings.

You can select the protocol in "Protocol" option according to your needs. Click "Create" button on the right to open the protocol configuration, and it displays the current protocols supported by SerDes IP and the corresponding Quad, PLL and Lane usage; on the right side, it displays the information about the selected protocol, including "Information", "Summary" and "Reference".

3. Open 10G Serial Ethernet IP Interface Configuration.

Select "10G Serial Ethernet" in the "Protocol" option, and click "Create" button to open the 10G Serial Ethernet IP configuration interface, as shown in Figure 6-3.

Figure 6-3 PHY Configuration

The image shows a 'PHY Configuration' dialog box with two tabs: 'PHY Configuration' and 'AFE'. The 'PHY Configuration' tab is active. It contains the following settings:

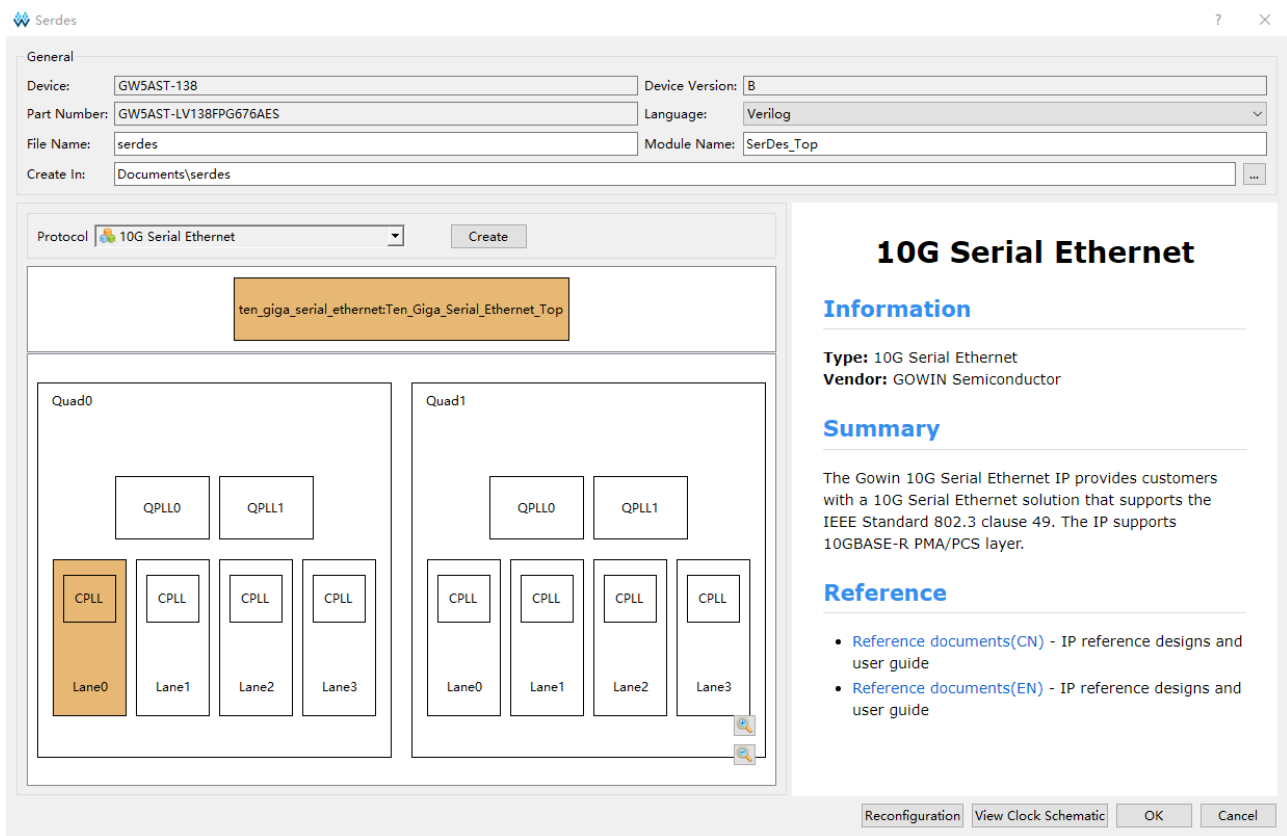
- Channel Selection: Q1 Lane1 (dropdown)
- Loopback Mode: OFF (dropdown)
- Line Rate: 10.3125 Gbps (text input)
- Refclk Selection (grouped box):
 - Reference Clock Source: Q1 REFCLK1 (dropdown)
 - Reference Clock Frequency: 156.250 MHz (dropdown)
 - PLL Selection: CPLL (dropdown)
- ☒ Debug Ports
- Calculate button
- OK and Cancel buttons at the bottom right.

The left side of the configuration interface displays the port diagram of 10G Serial Ethernet IP, and on the right side, it shows parameter configuration options, which includes the PHY Configuration option and AFE option. For the configuration options, you can see Table 5-1.

4. IP Generation

After completing 10G Serial Ethernet IP configuration, click "OK" button at the bottom right corner of the interface to generate files of the 10G Serial Ethernet IP, and return to the SerDes IP configuration interface, then the SerDes IP configuration interface displays the current generated 10G Serial Ethernet IP and the corresponding Quad, PLL and Lane usage, as shown in Figure 6-4.

Figure 6-4 10G Serial Ethernet IP Interface

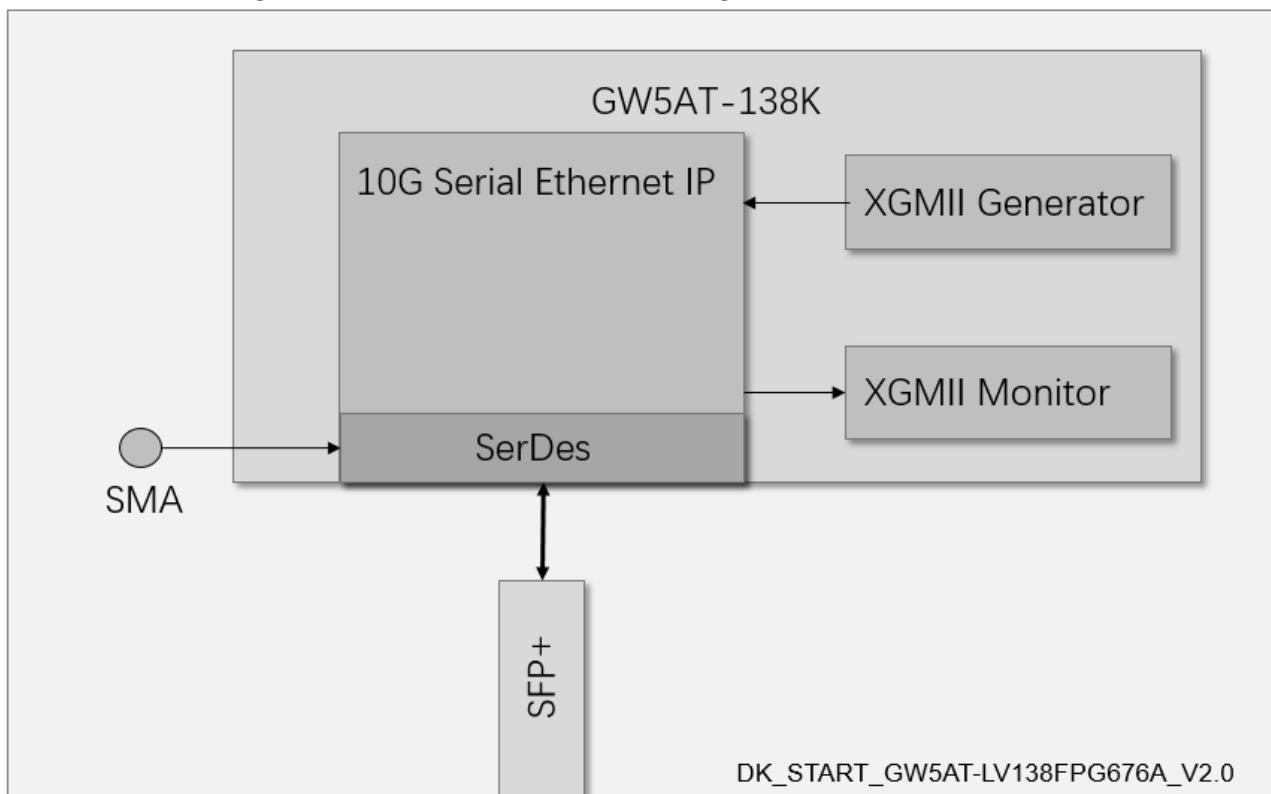


Then, click "OK" button at the bottom right corner of the interface to generate SerDes IP files and complete the whole 10G Serial Ethernet IP generation.

7 Reference Design

See Gowin 10G Serial Ethernet IP [reference design](#) for details at Gowinsemi website. The hardware platform is as shown in Figure 7-1.

Figure 7-1 Hardware Platform and Diagram



This reference design takes DK_START_GW5AT-LV138FPG676A_V2.0 development board as the hardware platform. As shown in the above figure, the FPGA connects to a 10G SFP+ module via SFP1 on the development board, serving as the channel for 10G Ethernet transmission. Additionally, a differential clock with a frequency of 156.25MHz is input to the SerDes as a reference clock through SMA (AA13 and AB13).

In the reference design, XGMII Generator module is used to send XGMII-formatted data to the 10G Serial Ethernet IP, and the XGMII Monitor

module is employed to monitor the data received by the 10G Serial Ethernet IP. Users can observe the transmitted and received XGMII data through GAO.

