Gowin USB 3.0 PHY IP

User Guide

IPUG1187-1.2E, 05/23/2025

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Revision History

Date	Version	Description
05/17/2024	1.0E	Initial version published.
01/17/2025	1.1E	ref_clk signal added.
05/23/2025	1.2E	Arora V 15K devices supported.

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1 About This Guide

1.1 Purpose

The purpose of Gowin USB 3.0 PHY IP User Guide is to help you learn the features and usage of Gowin USB 3.0 PHY IP by providing descriptions of functions, signals, and interface configuration, etc. The software screenshots and the supported products listed in this manual are based on Gowin Software 1.9.11. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI website. You can find the related documents at www.gowinsemi.com:

- DS981, GW5AT series of FPGA Products Data Sheet
- DS1104, GW5AST series of FPGA Products Data Sheet
- SUG100, Gowin Software User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
CDR	Clock and Data Recovery
IP	Intellectual Property
LFPS	Low Frequency Periodic Signaling

Terminology and Abbreviations	Meaning
PIPE	Physical Interface for PCI Express
USB	Universal Serial Bus

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Function Overview

2.1 Overview

Universal Serial Bus, commonly known as USB, is an external bus used to standardize the connection and communication between computers and external devices. Gowin USB 3.0 PHY IP is a USB 3.0 physical layer transceiver that can support data receive and transmit at high speed (5Gbps).

Table 2-1 Gowin USB 3.0 PHY IP Overview

Gowin USB 3.0 PHY IP	
Logic Resource	Please refer to Table 2-1
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.9.01 and above)

Note!

For the devices supported, you can click here to get the information.

2.2 Features

The features of Gowin USB 3.0 PHY IP are as follows:

- Supports 5Gbps mode
- Supports data serial and parallel conversion
- Supports 8B/10B encoding and decoding

- Supports receiver detection
- Supports LFPS detection and transmission
- Supports PIPE 3.0 interface

2.3 Resource Utilization

Gowin USB 3.0 PHY IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades. Taking Gowin GW5AST-138 and GW5AT-60/15 devices as an instance, the resource utilization of Gowin USB 3.0 PHY IP is as shown in Table 2-2.

Table 2-2 Resource Utilization

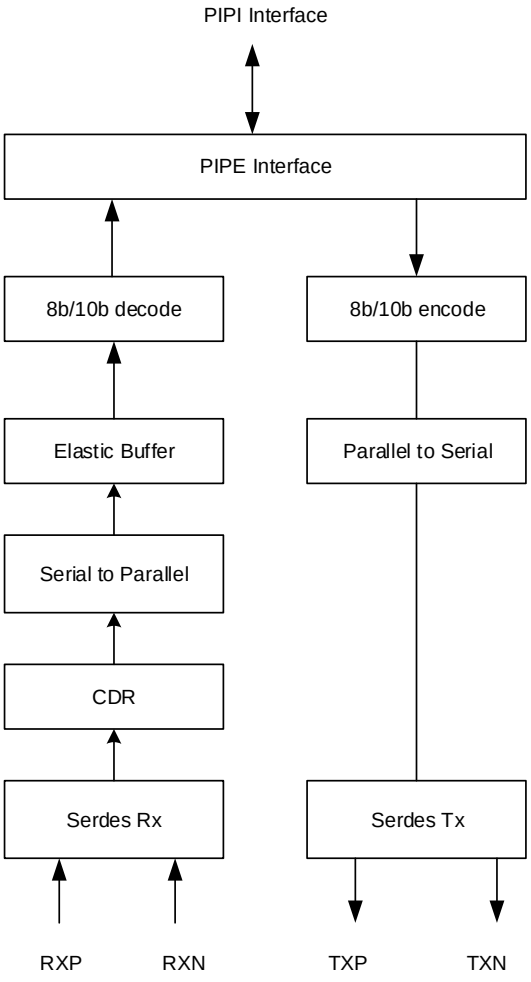
Device	Speed Grade	Name	Resource Utilization
GW5AST-138	ES	LUT	1337
		REG	684
		ALU	7
		BSRAM	0
GW5AT-60	C1/I0	LUT	2139
		REG	1002
		ALU	20
		BSRAM	1
GW5AT-15	C2/I1	LUT	2155
		REG	993
		ALU	20
		BSRAM	1

3 Functional Description

3.1 USB 3.0 PHY

USB 3.0 PHY locates between the Link Layer and the counterpart PHY, facilitating TX/RX data at the Physical layer. The USB 3.0 PHY block diagram is as shown below.

Figure 3-1 USB 3.0 PHY Block Diagram



3.2 USB Power Management

The USB 3.0 specification defines 4 power states, U0, U1, U2, and U3, and the PIPE specification defines P0, P1, P2, and P3. The PowerDown pin states are mapped to LTSSM states as described in Table 3-1. For all power state transitions, the link layer controller must not begin any operational sequences or further power state transitions until the PhyStatus has indicated that the internal state transition is completed.

Table 3-1 Power State

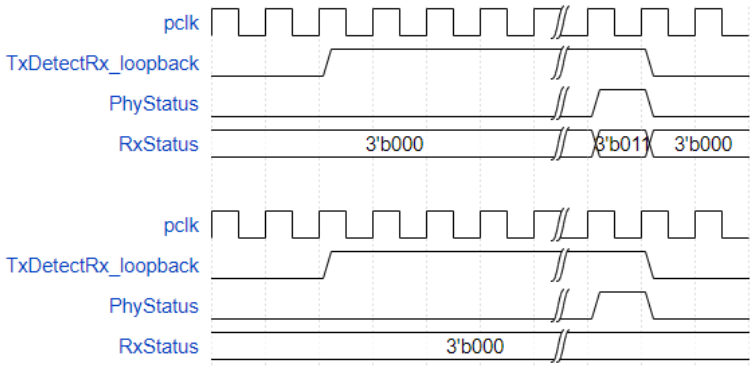
PIPE Power State	USB Power State	PCLK	PLL	TX	RX	PhyStatus
P0	U0, other states	On	On	On	On	Single cycle pulse
P1	U1	On	On	Idle, LFPS	Idle	Single cycle pulse
P2	U2, RxDetect, SS.inactive	On	On	Idle, LFPS, RxDetect	Idle	Single cycle pulse
P3	U3, SS.disable	None	None	LFPS, RxDetect	Idle	Pulled down

3.3 USB RX Status

3.3.1 RX Detection

When the PHY operates in P2 or P3 state, users can pull up the TxDetectRx_loopback signal. When the PHY detection is complete, the PhyStatus signal will be asserted for one clock cycle. If USB 3.0 is detected on the counterpart, RxStatus is encoded as 3'b011. If USB 3.0 is not detected on the counterpart, RxStatus is 3'b000.

Figure 3-2 RX Detection Timing



3.3.2 Clock Tolerance Compensation

The receiver contains an elastic buffer used to compensate for differences in frequencies between bit rates at the two ends of a link. The elastic buffer must be capable of holding enough symbols to handle worst case differences in frequency and worst case intervals between SKP ordered sets. When an SKP ordered set from the data stream is added, RxStatus is encoded as 3'b001, and it is asserted for one clock cycle. When an SKP ordered set is removed from the data stream, RxStatus is encoded as 3'b010, and it is asserted for one clock cycle.

3.3.3 Error Detection

The PHY can detect several types of receive errors. These errors are indicated by the RxStatus signal. When a receive error occurs, the error code closest to the error actually occurred in the data stream is asserted for one clock cycle. There are four errors on the RxStatus signal.

- 8B/10B decode error
- Elastic buffer overflow
- Elastic buffer read empty
- Disparity error

If an error occurs during an SKP ordered set, causing the error signal on RxStatus to coincide with the SKP add/remove signal on the same CLK, the error signal takes priority.

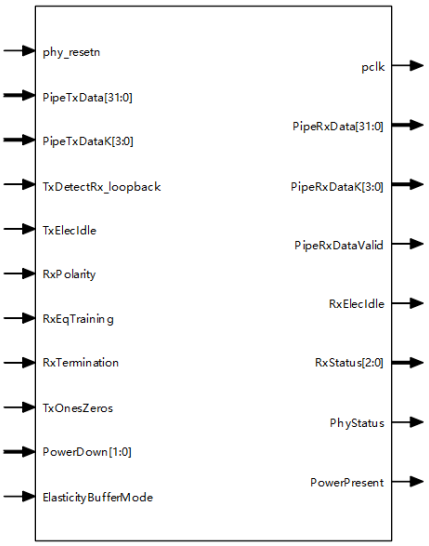
3.3.4 Loopback Mode

When TxDetectRx_loopback is pulled up and TxElecidle is pulled down, the PHY enters loopback mode. In loopback mode, data transmission from the PIPE TX interface to the SerDes TX channel stops, and data transmission from the Serdes TX to SerDes RX channel begins. During loopback, the received data is still transmitted to the PIPE RX interface. Loopback operation is terminated when TxDetectRx_loopback is pulled down.

4 Signal Definition

The IP port diagram of Gowin USB 3.0 PHY IP is shown in Figure 4-1.

Figure 4-1 Gowin Gowin USB 3.0 PHY IP Port Diagram



The signal definitions of Gowin USB 3.0 PHY IP signals are shown in Table 4-1.

Table 4-1 Signal Definition

No.	Signal Name	I/O	Data Width	Description
1	phy_resetn	Input	1	PHY reset signal, active-low
2	ref_clk	Input	1	The RX reference clock with frequency of 125 MHz
2	pclk	Output	1	Parallel interface data clock, 125MHz
3	PipeTxData	Input	32	Parallel USB input bus 32 bits represent 4 symbols of transmit data. PipeTxData [7:0] is the first symbol to be transmitted, and PipeTxData [15:8] is the

No.	Signal Name	I/O	Data Width	Description
				second symbol. PipeTxData [23:16] is the third symbol to be transmitted, and PipeTxData [31:24] is the fourth symbol.
4	PipeTxDataK	Input	4	Data/Control for the symbols of transmit data PipeTxDataK[0] corresponds to PipeTxData [7:0]; PipeTxDataK[1] corresponds to PipeTxData [15:8]; PipeTxDataK[2] corresponds to PipeTxData [23:16]; PipeTxDataK[3] corresponds to PipeTxData [31:24].
5	PipeRxData	Input	32	Parallel USB output bus 32 bits represent 4 symbols of transmit data. PipeRxData [7:0] is the first symbol to be transmitted, and PipeRxData [15:8] is the second symbol. PipeRxData [23:16] is the third symbol to be transmitted, and PipeRxData [31:24] is the fourth symbol.
6	PipeRxDataK	Output	4	Data/Control bit for the symbols of receive data; PipeRxDataK[0] corresponds to PipeRxData [7:0]; PipeRxDataK[1] corresponds to PipeRxData [15:8]; PipeRxDataK[2] corresponds to PipeRxData [23:16]; PipeRxDataK[3] corresponds to PipeRxData [31:24].
7	PipeRxDataValid	Output	1	RX data valid, active-high
8	TxDetectRx_loopback	Input	1	Used to indicate the PHY to begin a receiver detection operation or to begin loopback or to signal LFPS during P0 for USB Polling state.
9	TxElecIdle	Input	1	Force TX output to electrical idle according to power state, active-high
10	RxPolarity	Input	1	Tell PHY to do a polarity inversion on the received data 0: PHY does no polarity inversion 1: PHY does polarity inversion.
11	RxEqTraining	Input	1	Used to instruct the receiver to bypass normal operation to perform equalization training. While performing training, the state of the RxData interface is undefined.

No.	Signal Name	I/O	Data Width	Description
12	RxTermination	Input	1	Used to control receiver termination, active-high
13	RxElecIdle	Output	1	Receiver detection of an electrical idle, indicating that LFPS is detected.
14	RxStatus	Output	3	Encodes the receiver state and error code of the received data stream, see details in Table 4-2.
15	TxOnesZeros	Input	1	Tells PHY to transmit an alternating sequence of 50-250 ones and 50-250 zeros
16	PowerDown	Input	2	PHY power state, see details in Table 4-3.
17	PhyStatus	Output	1	Used to indicate completion of several PHY functions including stable PCLK after Reset, power management state transitions, rate change, and receiver detection.
18	PowerPresent	Output	1	Used to indicate the presence of VBUS

Table 4-2 RxStatus Definition

RxStatus [2]	RxStatus [1]	RxStatus [0]	Description
0	0	0	Received data normal
0	0	1	1 SKP ordered set added
0	1	0	1 SKP ordered set removed
0	1	1	Receiver detected
1	0	0	8B/10B decode error
1	0	1	Elastic buffer overflow
1	1	0	Elastic Buffer underflow
1	1	1	Receive disparity error

Table 4-3 PowerDown Definition

PowerDown [1]	PowerDown [0]	Description
0	0	P0, normal operation
0	1	P1, low recovery time latency, power saving state
1	0	P2, longer recovery time latency, lower power state
1	1	P3, lowest power state

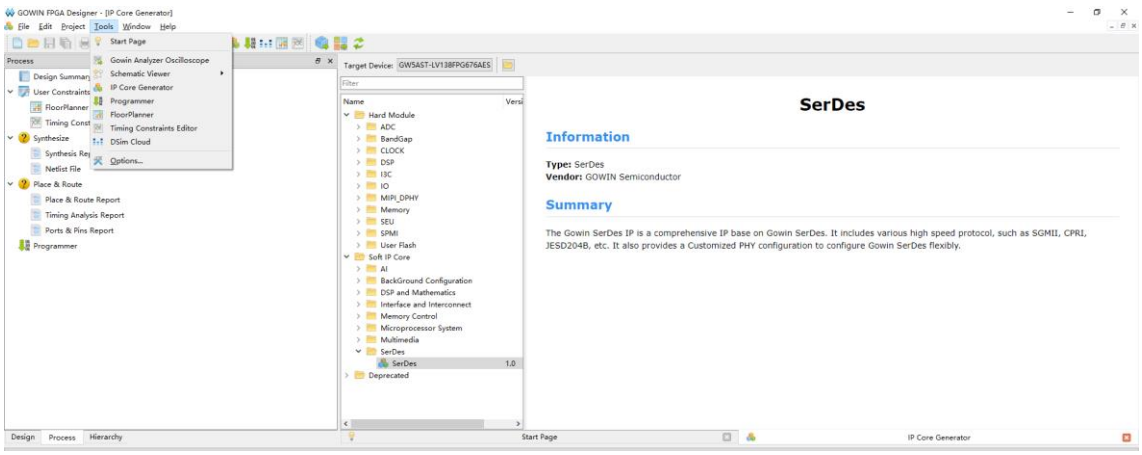
5 Interface Configuration

You can select Tools in Gowin Software to start the IP Core Generator to call and configure USB 3.0 PHY.

1. Open IP Core Generator.

After creating the project, you can click the "Tools" tab in the upper-left corner, then click the "IP Core Generator" via the drop-down list, as shown in Figure 5-1.

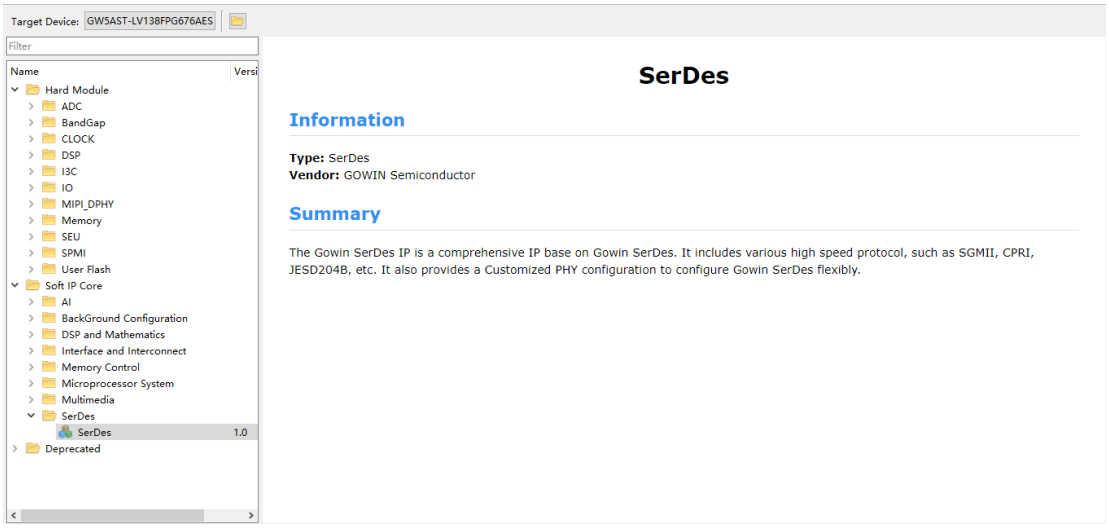
Figure 5-1 IP Core Generator



2. Open SerDes IP

Select "SerDes" in IP Core Generator and open SerDes IP configuration interface, as shown in Figure 5-2.

Figure 5-2 SerDes IP Core



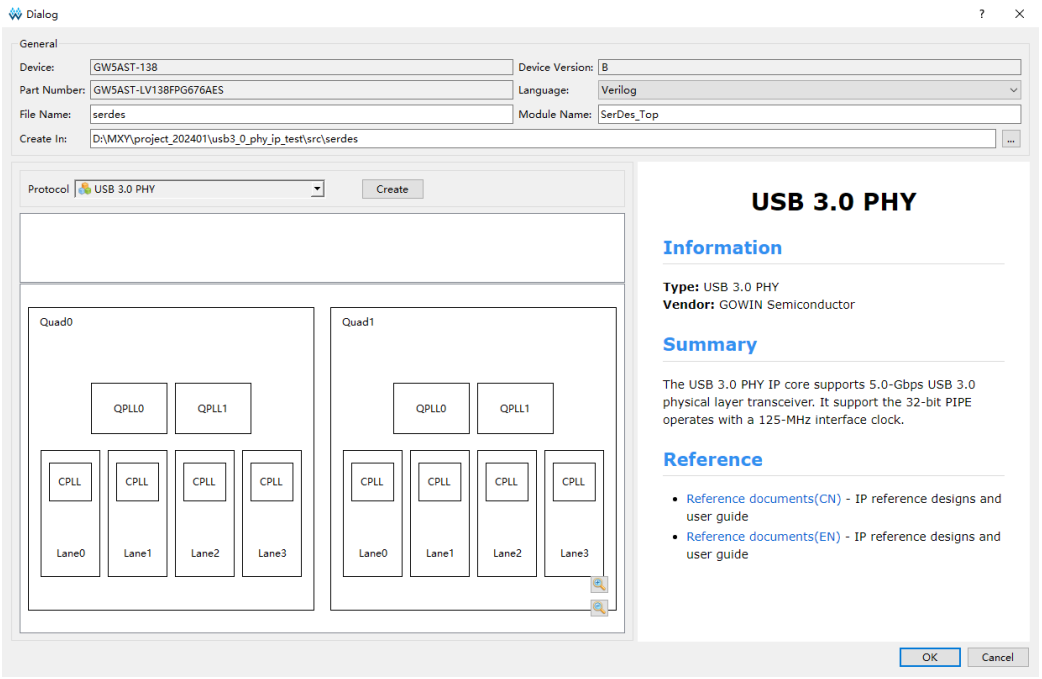
3. SerDes IP Core Configuration Interface

First configure "General" tab in the SerDes IP interface.

- Device, Device Version, Part Number: Part number settings, determined by the current project, and the user can not set it.
- Language: Support Verilog and VHDL; choose the language as requirements, and the default is Verilog.
- File Name, Module Name, Create In: Display SerDes file name, module name and the generated file path settings.

You can select the protocol in "Protocol" option according to your needs. Click "Create" button on the right to open the protocol configuration, and it displays the current protocols supported by SerDes IP and the corresponding Quad, PLL and Lane usage; on the right side, it displays the information about the selected protocol, including "Information", "Summary" and "Reference".

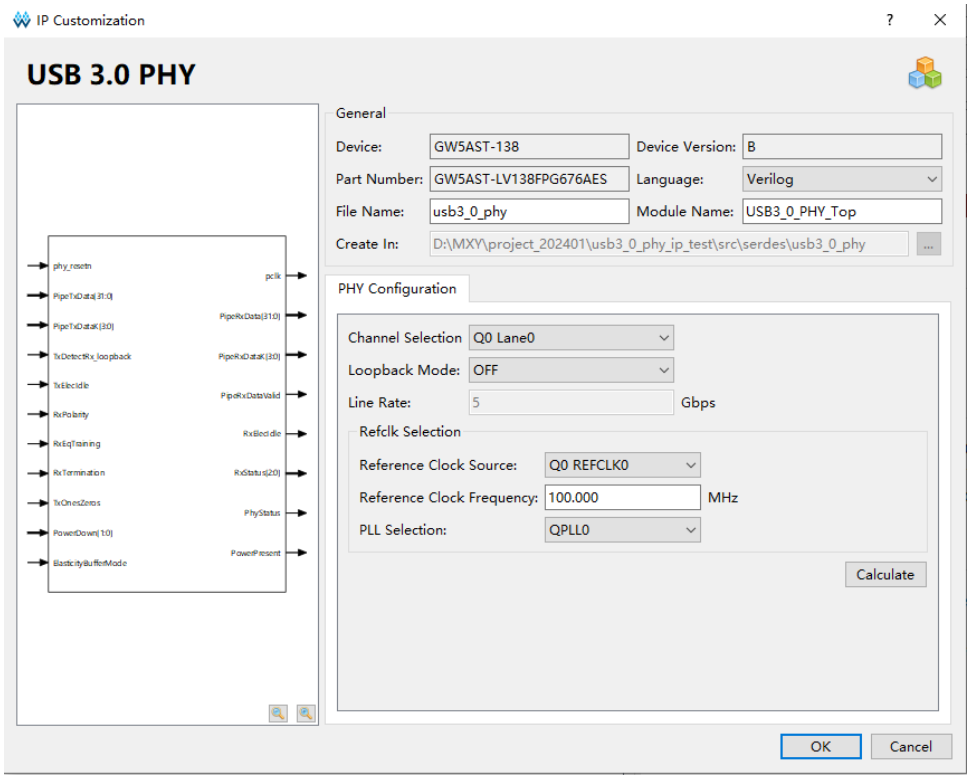
Figure 5-3 SerDes Configuration Interface



4. Open USB 3.0 PHY IP configuration interface

Select "USB 3.0 PHY" in the "Protocol" option, and click "Create" button to open the USB 3.0 PHY IP configuration interface, as shown in Figure 5-4.

Figure 5-4 PHY Configuration



The left side of the configuration interface displays the port diagram of USB 3.0 PHY IP, and on the right side, it shows parameter configuration options, which includes the PHY Configuration option.

- Channel Selection option: Select the required lane from the drop-down list, including eight lanes, Q0 Lane0, Q0 Lane1, Q0 Lane2, Q0 Lane3, Q1 Lane0, Q1 Lane1, Q1 Lane2 and Q1 Lane3; if the lane is already in use, it will not be displayed.
- Loopback Mode option: Includes four modes, OFF, LB_NES, LB_FES and LB_ENC.
- Line Rate option: The default rate is 5 Gbps, which cannot be configured.
- Reference Clock Source option: Reference clock source, and you can select REFCLK0 and REFCLK1 of Quad0 or REFCLK0 and REFCLK1 of Quad1.
- Reference Clock Frequency option: Reference clock frequency, if the reference clock source is used, the frequency displayed here is the one of the selected reference clock source.
- PLL Selection: PLL source; you can select QPLL0, QPLL1, or CPLL.

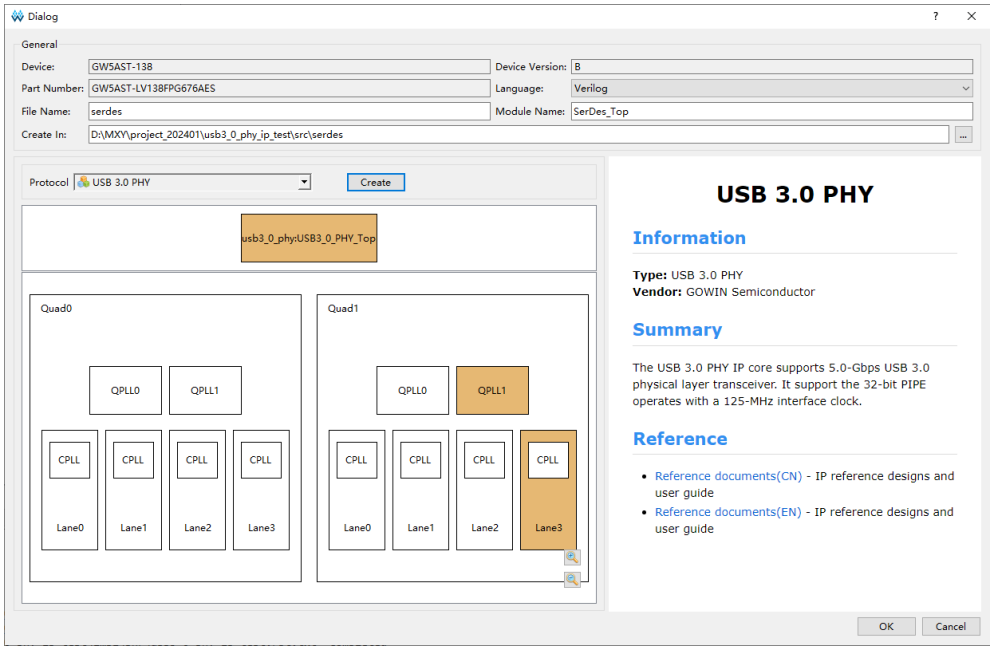
There is a limitation between the line rate and the reference clock; make sure that the reference clock can generate the above line rate, which can also be detected through clicking "Calculate" button.

5. IP Generation

After completing USB 3.0 PHY IP configuration, click "OK" button at the bottom right corner of the interface to generate files of the USB 3.0 PHY IP, and return to the SerDes IP configuration interface, and then the SerDes IP configuration interface displays the current generated IP and the corresponding Quad, PLL, and Lane usage, as shown in Figure 5-5.

Then, click "OK" button at the bottom right corner of the interface to generate SerDes IP files and complete the whole USB 3.0 PHY IP generation.

Figure 5-5 USB 3.0 PHY Generation



6 Reference Design

See Gowin USB3.0 PHY RefDesign at Gowinsemi website.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