




Gowin USB 2.0 SoftPHY IP

User Guide

IPUG781-1.7E, 07/18/2025

Copyright © 2025 Guangdong Gowin Semiconductor Corporation. All Rights Reserved.

GOWIN  is a trademark of Guangdong Gowin Semiconductor Corporation and is registered in China, the U.S. Patent and Trademark Office, and other countries. All other words and logos identified as trademarks or service marks are the property of their respective holders. No part of this document may be reproduced or transmitted in any form or by any denotes, electronic, mechanical, photocopying, recording or otherwise, without the prior written consent of GOWINSEMI.

Disclaimer

GOWINSEMI assumes no liability and provides no warranty (either expressed or implied) and is not responsible for any damage incurred to your hardware, software, data, or property resulting from usage of the materials or intellectual property except as outlined in the GOWINSEMI Terms and Conditions of Sale. GOWINSEMI may make changes to this document at any time without prior notice. Anyone relying on this documentation should contact GOWINSEMI for the current documentation and errata.

Revision History

Date	Version	Description
07/23/2021	1.0E	Initial version published.
08/13/2021	1.1E	The property configuration of IO ports modified.
10/12/2021	1.2E	Chapter 2.3 "Using 5V Host Supply to Power USB Device Solution" added.
12/23/2021	1.3E	<ul style="list-style-type: none">● The configuration method of peripheral circuit modified.● IO configuration constraints added.
03/29/2022	1.4E	The description of resource utilization added.
06/20/2022	1.5E	<ul style="list-style-type: none">● The speed grade modified.● The description of pin constraints updated.
07/20/2022	1.5.1E	A note added in Table 2-1.
03/28/2025	1.6E	<ul style="list-style-type: none">● LVDS mode added.● Peripheral circuit configuration modified.
07/18/2025	1.7E	<ul style="list-style-type: none">● Reference for the use of UTMI and ULPI interfaces added.● Descriptions of the external circuit connections for USB 2.0 SoftPHY improved.● Figure 3-3 USB Slave Device Interface Implementation in Dual LVDS Mode updated.● Descriptions of the utmi_xcvrselect_i and utmi_termselect_i ports updated.

Contents

Contents	i
List of Figures	ii
List of Tables	iii
1 About This Guide	1
1.1 Purpose	1
1.2 Related Documents	1
1.3 Terminology and Abbreviations.....	2
1.4 Support and Feedback	2
2 Introduction	3
2.1 Overview.....	3
2.2 Features.....	4
2.3 Using 5V Host Supply to Power USB Device Solution.....	4
2.4 Resource Utilization.....	5
3 Functional Description	6
3.1 USB 2.0 SoftPHY Block Diagram	6
3.2 USB 2.0 SoftPHY External Circuit Connection.....	7
4 Signal Description	11
5 Interface Configuration	14

List of Figures

Figure 3-1 USB 2.0 SoftPHY Block Diagram	6
Figure 3-2 USB Slave Device Interface Implementation in Single LVDS Mode	7
Figure 3-3 USB Slave Device Interface Implementation in Dual LVDS Mode.....	8
Figure 3-4 GW1NSR-4 Pinout	10
Figure 5-1 IP Core Generator	14
Figure 5-2 Open USB 2.0 SoftPHY IP Core	15
Figure 5-3 USB 2.0 SoftPHY IP Configuration Interface	15

List of Tables

Table 1-1 Terminology and Abbreviations	2
Table 2-1 Gowin USB 2.0 SoftPHY IP Overview	3
Table 2-2 DC Electrical Characteristics	4
Table 2-3 Resource Utilization (I).....	5
Table 2-4 Resource Utilization (II)	5
Table 4-1 Signal Description	11

1 About This Guide

1.1 Purpose

The purpose of Gowin USB 2.0 SoftPHY IP User Guide is to help you learn the features and usage of this IP by providing the descriptions of functions, signals, and interface configuration. The software screenshots in this manual are based on V 1.9.11.01. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at: www.gowinsemi.com.

- [DS100, GW1N series of FPGA Products Data Sheet](#)
- [DS117, GW1NR series of FPGA Products Data Sheet](#)
- [DS821, GW1NS series of FPGA Products Data Sheet](#)
- [DS861, GW1NSR series of FPGA Products Data Sheet](#)
- [DS891, GW1NRF series of FPGA Products Data Sheet](#)
- [DS881, GW1NSER series of Bluetooth FPGA Products Data Sheet](#)
- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [DS961, GW2ANR series of FPGA Products Data Sheet](#)
- [DS976, GW2AN-55 Data Sheet](#)
- [DS971, GW2AN-18X & 9X Data Sheet](#)
- [DS981, GW5AT series of FPGA Products Data Sheet](#)

- [DS1103, GW5A series of FPGA Products Data Sheet](#)
- [DS1239, GW5AST series of FPGA Products Data Sheet](#)
- [DS1105, GW5AS series of FPGA Products Data Sheet](#)
- [DS1108, GW5AR series of FPGA Products Data Sheet](#)
- [DS1118, GW5ART series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FS	Full Speed
HS	High Speed
IP	Intellectual Property
LS	Low Speed
NRZI	Non Return Zero Inverted
ULPI	UTMI+ Low Pin Interface
USB	Universal Serial Bus
UTMI	USB 2.0 Transceiver Macrocell Interface

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Introduction

2.1 Overview

Gowin USB 2.0 SoftPHY IP is a USB physical layer transceiver that can support data reception and transmission at high speed (480Mbps), full speed (12Mbps), and low speed (1.5Mbps).

Table 2-1 Gowin USB 2.0 SoftPHY IP Overview

Gowin USB 2.0 SoftPHY IP	
Supported Devices ^[1]	<ul style="list-style-type: none"> ● Arora family ● LittleBee family, excluding GW1N-1/GW1N-1S/GW1NZ-1/GW1N-1P5 devices.
Logic Resource	Please refer to Table 2-3 and Table 2-4.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.8.05 and above)

Note!

^[1] Only part number with speed grade C7 and above (Arora V excluded) support Gowin USB 2.0 SoftPHY IP.

2.2 Features

The features of GowinUSB 2.0 SoftPHY IP include:

- Supports HS (480 Mbps), FS (12 Mbps), and LS (1.5 Mbps) peripheral modes
- Supports data serial and parallel conversion
- Supports bit stuffer and unstuffer
- Supports NRZI encoder and decoder
- Supports UTMI interface peripheral mode, compliant with USB 2.0 Transceiver Macrocell Interface (UTMI) Version 1.05
- Supports ULPI interface peripheral mode, compliant with UTMI+ Low Pin Interface (ULPI) Specification Revision 1.1

2.3 Using 5V Host Supply to Power USB Device Solution

Many solutions may provide power to a USB device using the 5V provided over the cable from the Host without providing a separate power supply. To support cable powered USB device use cases, designers must be careful to ensure the total PCB BOM of the device does not exceed the current limitations of the USB Host as well as voltage drops over the cable.

The USB v2.0 specification, sections 7.1.2 and 7.3.2 provides information on current and voltage drop requirements expected to be supplied by a USB Host. If the total PCB BOM cannot meet the current and minimum voltage requirements of the specified host, the board can be powered with a separate power supply.

Table 2-2 DC Electrical Characteristics

Parameter	Symbol	Condition	Min.	Max.	Unit
Supply voltage					
High-power Port	V_{BUS}	Note 2, Section 7.2.1	4.75	5.25	V
Low-power Port	V_{BUS}	Note 2, Section 7.2.1	4.40	5.25	V
Supply Current					
High-power Hub Port (out)	I_{CCPRT}	Section 7.2.1	500	–	mA
Low-power Hub Port (out)	I_{CCUPT}	Section 7.2.1	100	–	mA
High-Power Function (in)	I_{CCHPF}	Section 7.2.1	–	500	mA

Parameter	Symbol	Condition	Min.	Max.	Unit
Low-power Function (in)	I _{CCLPF}	Section 7.2.1	–	100	mA
Unconfigured Function/Hub (in)	I _{CCINIT}	Section 7.2.1.4	–	100	mA
Suspended High-power Device	I _{CCSH}	Note 15, Section 7.2.3	–	2.5	mA
Suspended Low-power Device	I _{CCSL}	Section 7.2.3	–	500	μA

2.4 Resource Utilization

Gowin USB 2.0 SoftPHY IP can be implemented by Verilog. Its resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades. Taking Gowin GW1N-9 and GW5A-25 series of FPGA products as an instance, the resource utilization is as shown in Table 2-3 and Table 2-4.

Table 2-3 Resource Utilization (I)

Device	Speed Grade	Resource	Utilization
GW1N-9	C7/I6	LUT	432
		REG	1040
		ALU	14
		BSRAM	2
		SSRAM	0
		IO	Single Mode: 9 Dual Mode: 11

Note!

Please use chips with speed grade C7/I6.

Table 2-4 Resource Utilization (II)

Device	Speed Grade	Resource	Utilization
GW5A-25	C2/I1	LUT	436
		REG	1029
		ALU	14
		BSRAM	2
		SSRAM	0
		IO	Single Mode: 9 Dual Mode: 11

3 Functional Description

3.1 USB 2.0 SoftPHY Block Diagram

In the RX direction of the USB 2.0 SoftPHY, USB serial data is received through the IDER8, NRZI decoder, bit unstuff, and shift Reg modules in sequence to complete USB RX data reception. The received data is then transmitted to the upper-layer module via the UTMI or ULPI interface. In the TX direction, after receiving data from the UTMI or ULPI interface, the data passes through the data shift, bit stuffer, and NRZI encoder modules to generate a serial TX data stream, which is then sent to the USB interface via the OSER8.

Figure 3-1 USB 2.0 SoftPHY Block Diagram

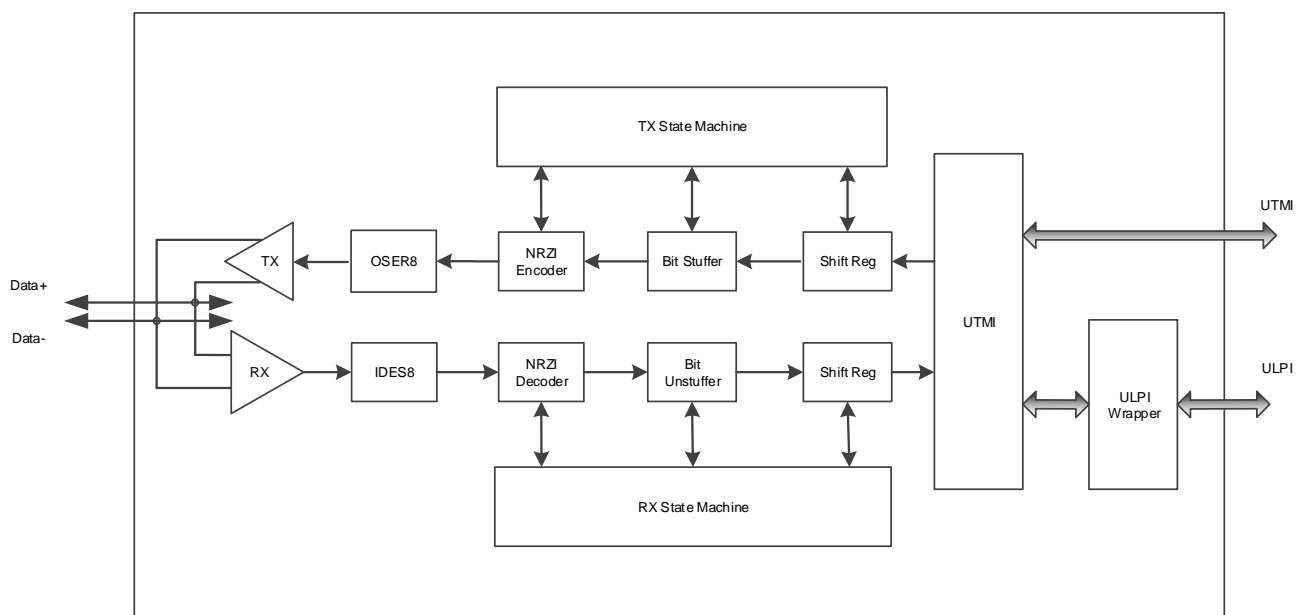
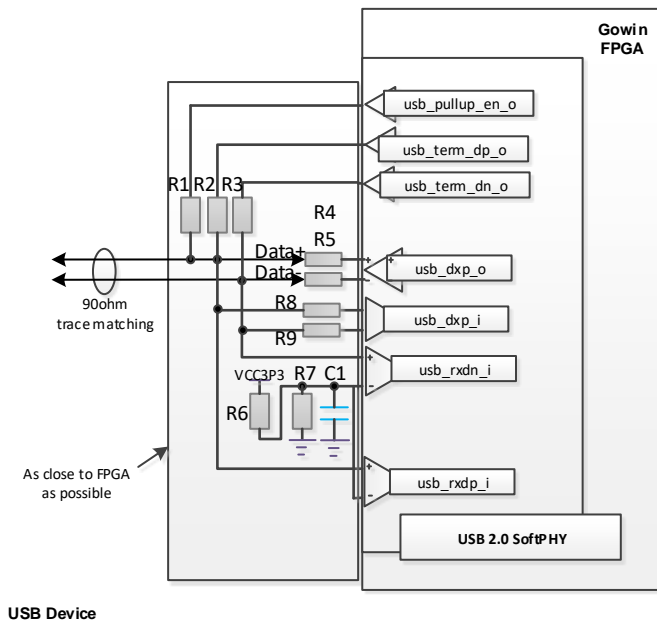


Figure 3-3 USB Slave Device Interface Implementation in Dual LVDS Mode

R1:1.5K ohm
 R2:0 ohm(1N/2A), 36 ohm(Arora V)
 R3:0 ohm(1N/2A), 36 ohm(Arora V)
 R4:42 ohm(1N/2A), 100 ohm(Arora V)
 R5:42 ohm(1N/2A), 100 ohm(Arora V)
 R6:1.8K ohm
 R7: 75 ohm(1N), 56 ohm(2A), 75 ohm(Arora V)
 R8: 0 ohm
 R9: 0 ohm
 C1:1uF



1. You can see the followings for the IO port attribute constraints of GW2A series of FPGA.
 - usb_dxp_io: IO_TYPE= LVCMOS33D PULL_MODE= NONE DRIVE=4
 - usb_term_dn_o: IO_TYPE=LVCMOS33 PULL_MODE= NONE DRIVE=8
 - usb_term_dp_o: IO_TYPE=LVCMOS33 PULL_MODE=NONE DRIVE=8
 - usb_pullup_en_o: IO_TYPE=LVCMOS33 PULL_MODE=NONE DRIVE=8
 - usb_rxdn_i: IO_TYPE=LVDS25 PULL_MODE=NONE
 - usb_rxdp_i: IO_TYPE=LVDS25 PULL_MODE=NONE
2. You can see the followings for the IO port attribute constraints of GW1N series of FPGA.
 - usb_dxp_io: IO_TYPE= LVCMOS33D PULL_MODE= NONE DRIVE=8


- usb_term_dn_o: IO_TYPE=LVC MOS33 PULL_MODE= NONE DRIVE=16
 - usb_term_dp_o: IO_TYPE=LVC MOS33 PULL_MODE= NONE DRIVE=16
 - usb_pullup_en_o: IO_TYPE=LVC MOS33 PULL_MODE= NONE DRIVE=8
 - usb_rxdn_i: IO_TYPE=LVDS25 PULL_MODE=NONE
 - usb_rxdp_i: IO_TYPE=LVDS25 PULL_MODE=NONE
 - usb_rxdn_i: IO_TYPE=LVDS25 PULL_MODE=NONE DIFF_RESISTOR=OFF
 - usb_rxdp_i: IO_TYPE=LVDS25 PULL_MODE=NONE DIFF_RESISTOR=OFF
 - usb_rxdn_i: IO_TYPE=LVDS25 PULL_MODE=NONE DIFF_RESISTOR=OFF
 - usb_rxdp_i: IO_TYPE=LVDS25 PULL_MODE=NONE DIFF_RESISTOR=OFF
3. You can see the followings for the IO port attribute constraints of Arora V devices.
- usb_dxp_io: IO_TYPE= LVC MOS33D PULL_MODE= NONE DIFF_RESISTOR=OFF DRIVE=8; (Single Mode Only)
 - usb_dxp_o: IO_TYPE= LVC MOS33D PULL_MODE= NONE DIFF_RESISTOR=OFF DRIVE=8; (Dual Mode Only)
 - usb_dxp_i: IO_TYPE= LVC MOS33D PULL_MODE= NONE; (Dual Mode Only)
 - usb_term_dn_o: IO_TYPE=LVC MOS33 PULL_MODE= NONE DRIVE=8
 - usb_term_dp_o: IO_TYPE=LVC MOS33 PULL_MODE=NONE DRIVE=8
 - usb_pullup_en_o: IO_TYPE=LVC MOS33 PULL_MODE=NONE DRIVE=8
 - usb_rxdn_i: IO_TYPE=LVDS25 PULL_MODE=NONE DIFF_RESISTOR=OFF
 - usb_rxdp_i: IO_TYPE=LVDS25 PULL_MODE=NONE DIFF_RESISTOR=OFF
4. All signals related to the USB interface on the FPGA are recommended

to be placed in one Bank, with adjacent pin assignments being ideal. The supply voltage for the I/O bank should be 3.3V. Differential signals such as `usb_dxp_io`, `usb_dxp_o`, and `usb_dxp_i` should be routed with matched trace on the PCB. Other signals, such as `usb_term_dp_o` and `usb_term_dn_o`, should also be trace-matched on the PCB.

- For LittleBee family and Arora family (Arora V excluded), it is required that the adjacent differential pair pins in the same Bank where the `usb_dxp_io` differential pair is located exist and are not used. Taking GW1NSR-4 as an example, Figure 3-4 shows the GW1NSR-4 Pinout. If the `usb_dxp_io` differential pair is located at G5, H5 (i.e. IOR11A/IOR11B) in the diagram, it will cause the project to report an error when implementing synthesis and placement with Gowin Software, as the adjacent differential pair pins IOR10A/IOR10B do not exist. If `usb_dxp_io` differential pair is located at G6/H6 (i.e. IOR13A/IOR13B), the project will synthesize and place successfully with Gowin Software, as the adjacent differential pair pins IOR12A/IOR12B exists.

Figure 3-4 GW1NSR-4 Pinout

GW1NSR Series of FPGA Products
GW1NSR-4 Pinout
Pin List



Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	MG64P
IOB13A	I/O	3		True_of IOB13B	NONE	NONE	
IOB13B	I/O	3		Comp_of IOB13A	NONE	NONE	
IOB14A	I/O	3		True_of IOB14B	NONE	NONE	
IOB14B	I/O	3		Comp_of IOB14A	NONE	NONE	
IOB15A	I/O	3		True_of IOB15B	NONE	NONE	
IOB15B	I/O	3		Comp_of IOB15A	NONE	NONE	
IOB16A/GCLKT_5	I/O	3	GCLKT_5	True_of IOB16B	NONE	NONE	
IOB16B/GCLKC_5	I/O	3	GCLKC_5	Comp_of IOB16A	NONE	NONE	
IOB22A/GCLKT_4	I/O	3	GCLKT_4	True_of IOB22B	NONE	NONE	
IOB22B/GCLKC_4	I/O	3	GCLKC_4	Comp_of IOB22A	NONE	NONE	
IOB23A	I/O	3		True_of IOB23B	NONE	NONE	
IOB23B	I/O	3		Comp_of IOB23A	NONE	NONE	
IOB24A	I/O	3		True_of IOB24B	NONE	NONE	
IOB24B	I/O	3		Comp_of IOB24A	NONE	NONE	
IOB25A	I/O	3		True_of IOB25B	NONE	NONE	
IOB25B	I/O	3		Comp_of IOB25A	NONE	NONE	
IOB29A	I/O	3		True_of IOB29B	NONE	NONE	
IOB29B	I/O	3		Comp_of IOB29A	NONE	NONE	
IOB4A	I/O	3		True_of IOB4B	NONE	NONE	
IOB4B	I/O	3		Comp_of IOB4A	NONE	NONE	
IOB5A	I/O	3		True_of IOB5B	NONE	NONE	
IOB5B	I/O	3		Comp_of IOB5A	NONE	NONE	
IOB6A	I/O	3		True_of IOB6B	NONE	NONE	
IOB6B	I/O	3		Comp_of IOB6A	NONE	NONE	
IOB7A	I/O	3		True_of IOB7B	NONE	NONE	
IOB7B	I/O	3		Comp_of IOB7A	NONE	NONE	
IOR11A/GCLKT_3	I/O	2	GCLKT_3	True_of IOR11B	TRUE	x16	G5
IOR11B/GCLKC_3	I/O	2	GCLKC_3	Comp_of IOR11A	TRUE	NONE	H5
IOR12A	I/O	2		True_of IOR12B	NONE	NONE	
IOR12B	I/O	2		Comp_of IOR12A	NONE	NONE	
IOR13A	I/O	2		True_of IOR13B	TRUE	x16	G6
IOR13B	I/O	2		Comp_of IOR13A	TRUE	NONE	H6
IOR14A	I/O	2		True_of IOR14B	NONE	NONE	

© 2021 GOWINSEMI

UG864-1.1E

1(4)

4 Signal Description

A description of Gowin USB 2.0 SoftPHY IP signals is as shown in Table 4-1.

Table 4-1 Signal Description

No.	Signal Name	I/O	Data Width	Description
1	clk_i	I	1	Input clock signal (60MHz)
2	fclk_i	I	1	Input clock signal (480MHz)
3	rst_i	I	1	Asynchronous reset signal resets the state machine inside of PHY.
4	pll_locked_i	I	1	pll lock signal generating fclk_i
5	utmi_data_out_i	I	8	Data input, 8-bit parallel data transmit bus.
6	utmi_txvalid_i	I	1	Transmit data valid indicator, active-high.
7	utmi_txready_o	O	1	Transmit data ready signal, indicating that PHY can receive the data to be transmitted from the controller end.
8	utmi_data_in_o	O	8	Data output, 8-bit parallel data receive bus.
9	utmi_rxactive_o	O	1	Rx data active, indicating that PHY detects the SYNC signal and then starts receiving data.
10	utmi_rxvalid_o	O	1	RX data valid, active-high.
11	utmi_rxerror_o	O	1	Receive data error, active high indicates receive error.

No.	Signal Name	I/O	Data Width	Description
12	utmi_linestate_o	O	2	Line status of receive end: DM DP 2'b00: SE0 2'b01: "J" 2'b10: "K" 2'b11: SE1
13	utmi_opmode_i	I	2	Operation mode selection signal: 2'b00: USB normal mode; enable bit stuffing and NRZI encoding. 2'b01: USB non-driving mode; USB TX enters high-impedance state. 2'b10: Disable bit stuffing and NRZI encoding 2'B11: Reserved
14	utmi_xcvsselect_i	I	2	Transmission mode selection signal: 2'b00: Enable HS mode 2'b01: Enable FS mode 2'b10: Enable LS mode 2'B11: Reserved
15	utmi_termselect_i	I	1	Termination Selection: 1' b0: Enable HS termination resistor 1' b1: Enable FS/LS pull-up signaling
16	ulpi_txdata_i	I	8	ULPI interface data input, 8-bit parallel transmit data bus.
17	ulpi_rxdata_o	O	8	ULPI interface data output, 8-bit parallel receive data bus.
18	ulpi_dir_o	O	1	ULPI interface data direction indicator: 1'b0: Data direction from Link to PHY 1'b1: Data direction from PHY to Link
19	ulpi_stp_i	I	1	ULPI interface stop signal for data

No.	Signal Name	I/O	Data Width	Description
				transmission, active high.
20	ulpi_nxt_o	O	1	ULPI interface Link data received signal, active high.
21	usb_dxp_io	I/O	1	USB data signal Data+, bidirectional, valid when LVDS_Mode is configured as Single.
22	usb_dxn_io	I/O	1	USB data signal Data-, bidirectional, valid when LVDS_Mode is configured as Single.
23	usb_dxp_i	I	1	USB data signal Data+ input, valid when LVDS_Mode is configured as Dual.
24	usb_dxn_i	I	1	USB data signal Data- input, valid when LVDS_Mode is configured as Dual.
25	usb_dxp_o	O	1	USB data signal Data+ output, valid when LVDS_Mode is configured as Dual.
26	usb_dxn_o	O	1	USB data signal Data- output, valid when LVDS_Mode is configured as Dual.
27	usb_rxdp_i	I	1	USB data signal Data+ input
28	usb_rxdn_i	I	1	USB data signal Data- input
29	usb_pullup_en_o	O	1	1.5K resistor pull-up control on USB data signal Data+
30	usb_term_dp_o	I/O	1	Termination resistor control of USB data signal Data+
31	usb_term_dn_o	I/O	1	Termination resistor control of USB data signal Data-

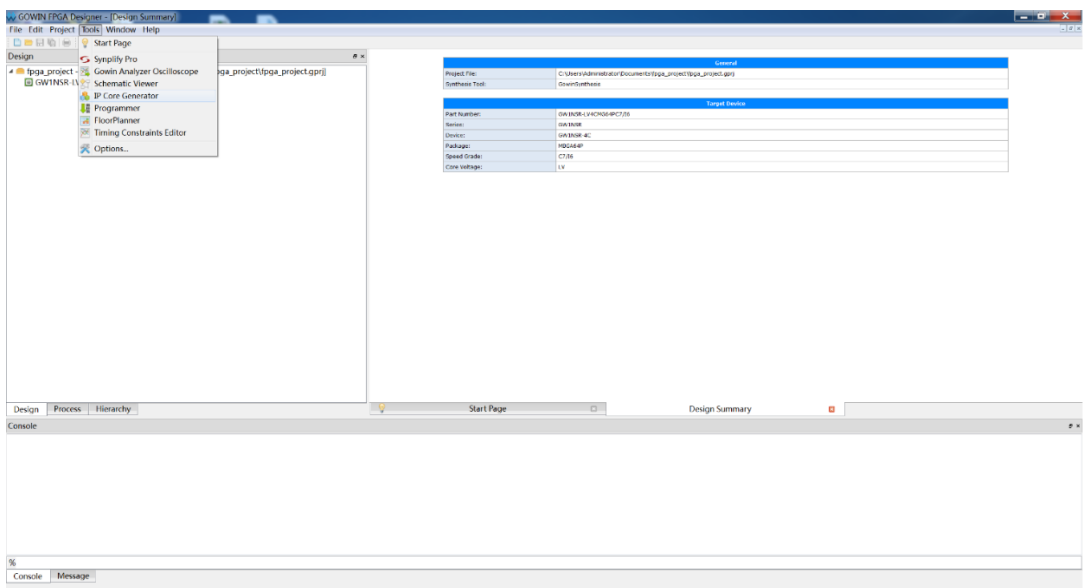
5 Interface Configuration

Selecting "Tools > IP Core Generator" in Gowin Software, you call and configure USB 2.0 SoftPHY.

1. Open IP Core Generator

After creating the project, you can click the "Tools" tab in the upper left, select and open the IP Core Generator via the drop-down list, as shown in Figure 5-1.

Figure 5-1 IP Core Generator



2. Open USB 2.0 SoftPHY IP Core

Select "Soft IP Core > Interface and Interconnect > USB 2.0 IP", as shown in Figure 5-2. Double-click to open the configuration interface.

Figure 5-2 Open USB 2.0 SoftPHY IP Core

USB 2.0 SoftPHY

Information

Type: USB 2.0 SoftPHY
Vendor: GOWIN Semiconductor

Summary

The USB 2.0 SoftPHY IP core is a transceiver compliant with the USB 2.0 Transceiver Macrocell Interface. It is capable of transmitting and receiving serial data at high speed (480M bit/s) data rate, full speed (12M bit/s) data rate and low speed (1.5M bit/s) data rate. While transmitting, the PHY serializes data, generates Synchronize (SYNC) and End-of-Packet (EOP) packet fields, and performs bit stuffing and Non-Return-to-Zero Inverted (NRZI) encoding. While receiving data, the PHY recovers incoming data and clock, de-serializes data, strips SYNC and EOP fields, and performs bit un-stuffing and NRZI decoding.

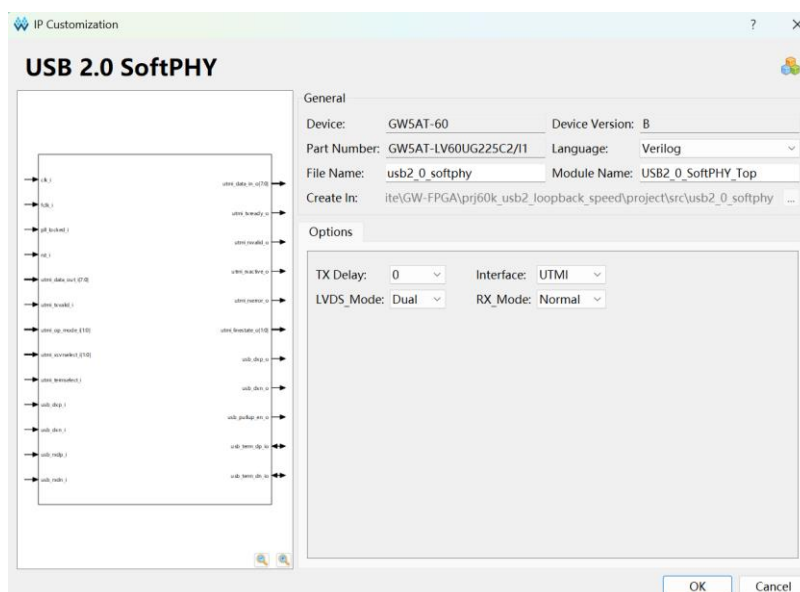
Reference

- [Reference documents\(CN\)](#) - IP reference designs and user guide
- [Reference documents\(EN\)](#) - IP reference designs and user guide

3. USB 2.0 SoftPHY IP Core Configuration Interface

Figure 5-3 shows the USB 2.0 SoftPHY IP core configuration interface. The ports diagram is on the left of the configuration interface. Options are on the right.

Figure 5-3 USB 2.0 SoftPHY IP Configuration Interface



General Tab Configuration

The General tab is used to configure information related to the generated IP design files.

- Device: Displays the configured device information.
- Part Number: Displays the configured part number information.

- **Language:** Specifies the hardware description language for the generated IP design files. Select the target language from the dropdown list on the right, supporting Verilog and VHDL.
- **Module Name:** Specifies the module name for the generated IP design files. The module name can be edited in the text box on the right. The Module Name must not be the same as a primitive name; otherwise, an Error message will be triggered.
- **File Name:** Specifies the file name for the generated IP design files. The file name can be edited in the text box on the right.
- **Create In:** Specifies the target path for the generated IP design files. The path can be edited in the text box on the right, or a target path can be selected using the button next to the text box.

Option Tab Configuration

- **TX Delay:** You can select 0/1/2, and it is used to configure the USB signal output enable delay.
- **Interface:** You can select UTMI/ULPI, and it is used to configure the IP control interface type.
- **LVDS_Mode:** You can select Single/Dual.
 - **Single mode:** Uses one differential pair for USB signal transmission.
 - **Dual Mode:** Uses two differential pairs for signal transmission, decoupling USB TX and RX I/O, which helps improve USB signal reception sensitivity.
- **RX_Mode:** You can select Normal/Advance.
 - **Normal Mode:** Uses a 60MHz low-speed clock to process RX data.
 - **Advance Mode:** Uses a 120MHz high-speed clock to process RX data, reducing data delay and requiring stricter timing. This mode is suitable for Arora V chips.

