Gowin HyperRAM Memory Interface IP

User Guide

IPUG944-2.0E, 08/15/2024

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Revision History

Date	Version	Description
07/30/2020	1.0E	Initial version published.
12/15/2020	1.01E	3.3 Resource Utilization improved.
06/07/2024	1.1E	GW5A(R)(S)(T) devices supported.
08/15/2024	2.0E	The embedded IP and the external IP merged and the relevant descriptions updated.

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1 About This Guide

1.1 Purpose

Gowin HyperRAM Memory Interface IP user guide includes the structure and function description, port description, timing description, configuration and call, reference design, etc. The guide helps you to quickly learn the features and usage of Gowin HyperRAM Memory Interface IP. The IP V2.0 is released with Gowin Software V1.9.10.01 and is compatible with both HyperRAM Memory Interface external IP and HyperRAM Memory Interface embedded IP from previous versions of Gowin Software.

1.2 Related Documents

You can find the related documents at www.gowinsemi.com:

- DS100, GW1N series of FPGA Products Data Sheet
- DS117, GW1NR series of FPGA Products Data Sheet
- DS821, GW1NS series of FPGA Products Data Sheet
- DS102, GW2A series of FPGA Products Data Sheet
- DS226, GW2AR series of FPGA Products Data Sheet
- DS841, GW1NZ series of FPGA Products Data Sheet
- DS861, GW1NSR series of FPGA Products Data Sheet
- DS871, GW1NSE series of FPGA Products Data Sheet
- DS881, GW1NSER series of SecureFPGA Products Data Sheet
- DS891, GW1NRF series of Bluetooth FPGA Products Data Sheet
- DS961, GW2ANR series of FPGA Products Data Sheet
- DS1228, Arora V FPGA Products Overview
- DS981, Arora V 138K & 75K FPGA Products Data Sheet
- DS1225, Arora V 60K FPGA Products Data Sheet
- DS1103, Arora V 25K FPGA Products Data Sheet
- DS1118, Arora V 15K FPGA Products Data Sheet
- SUG100, Gowin Software User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
BSRAM	Block Static Random Access Memory
IP	Intellectual Property
LUT	Look up Table
RAM	Random Access Memory

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

Gowin HyperRAM Memory Interface IP is a common used HyperRAM interface IP, in compliance with HyperRAM standard protocol. The IP includes the HyperRAM MCL (Memory Controller Logic) and the corresponding PHY (Physical Interface) design. Gowin HyperRAM Memory Interface IP provides you a common command interface to connect with the HyperRAM chip for data access and storage.

Table 2-1 Gowin HyperRAM Memory Interface IP

Gowin HyperRAM Memory Interface IP	
Logic Resource	Please refer to Table 3-1
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software

Note!

For the devices supported, you can click here to get the information.

3 Features and Performance

3.1 Features

- Compatible with interfaces of standard HyperRAM devices
- Supports memory data path width of 8 bits, 16 bits, 24 bits, 32 bits, 40 bits, 48 bits, 56 bits, and 64 bits
- Supports x8 data width memory chip
- Programs 16, 32, 64 or 128 burst lengths
- The clock rate is 1:2
- Supports the initial latency of 3, 4, 5, 6, 7, 8
- Supports the fixed latency mode
- Supports the power off option
- Configurable drive strength
- Configurable self-refresh area
- Configurable refresh rate
- The clock interface can be configured as single-ended or differential

3.2 Operating Frequency and Bandwidth Efficiency

The data rate and efficiency of the Gowin HyperRAM Memory Interface IP supports:

- Operating Frequency: Dependent on the part number. For example, if the W956x8MKY is selected, the operating frequency range is 50-200 MHz.
- Maximum Interface Rate: Dependent on the part number. For example, if the W956x8MKY is selected, the maximum rate is 400 Mbps.
- 128 burst lengths with a bandwidth efficiency of 74 per cent.
- 64 burst lengths with a bandwidth efficiency of 59 per cent.
- 32 burst lengths with a bandwidth efficiency of 42 per cent.
- 16 burst lengths with a bandwidth efficiency of 26 per cent.

3.3 Resource Utilization

Gowin HyperRAM Memory Interface IP employs the Verilog language, and the IP is applicable to Gowin FPGAs, excluding the GW1N-1, GW1N-1S, GW1NR-1, and GW1NZ-1. The resource utilization is as shown in Table 3-1.

Table 3-1 Resource Utilization

DQ_WIDTH	LUT	REGs	BSRAM	f_{MAX}	Throughput	Device Series	Speed Level
8(x8)	562	413	1	400Mbps	f_{MAX} x DQ x work efficiency	GW1NSR-4C	C7/I6

Note!

In Table 3-1, the user address width of Gowin HyperRAM Memory Interface IP is 22 bits, the HyperRAM WITDH is x8, and the burst length is 32. The increased burst length will increase the resource utilization.

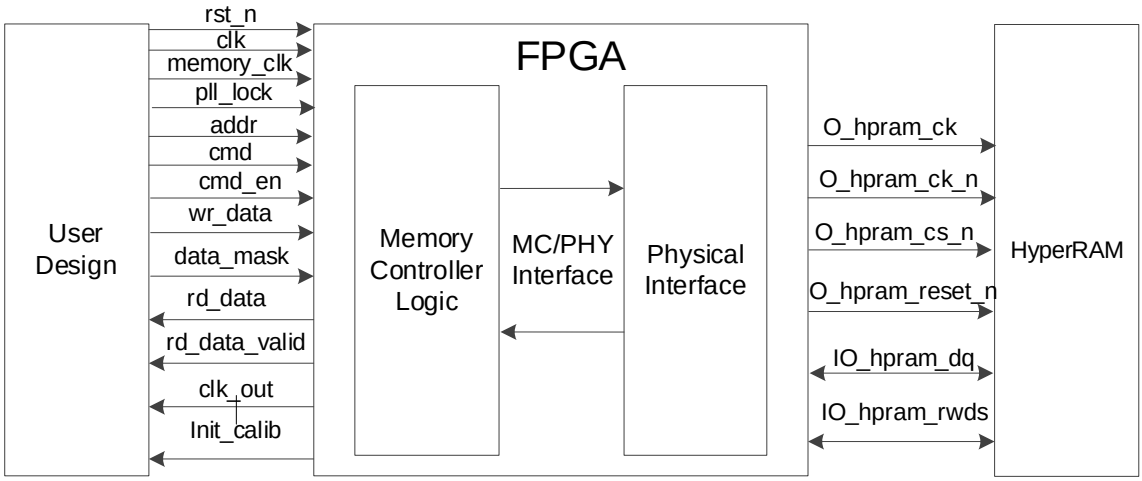
4 Functional Description

4.1 Architecture

As shown in Figure 4-1, Gowin HyperRAM Memory Interface IP mainly includes Memory Controller Logic, Physical Interface, etc.

The User Design module in Figure 4-1 is the module connected to the external HyperRAM chip in FPGA.

Figure 4-1 Gowin HyperRAM Memory Interface IP Structure



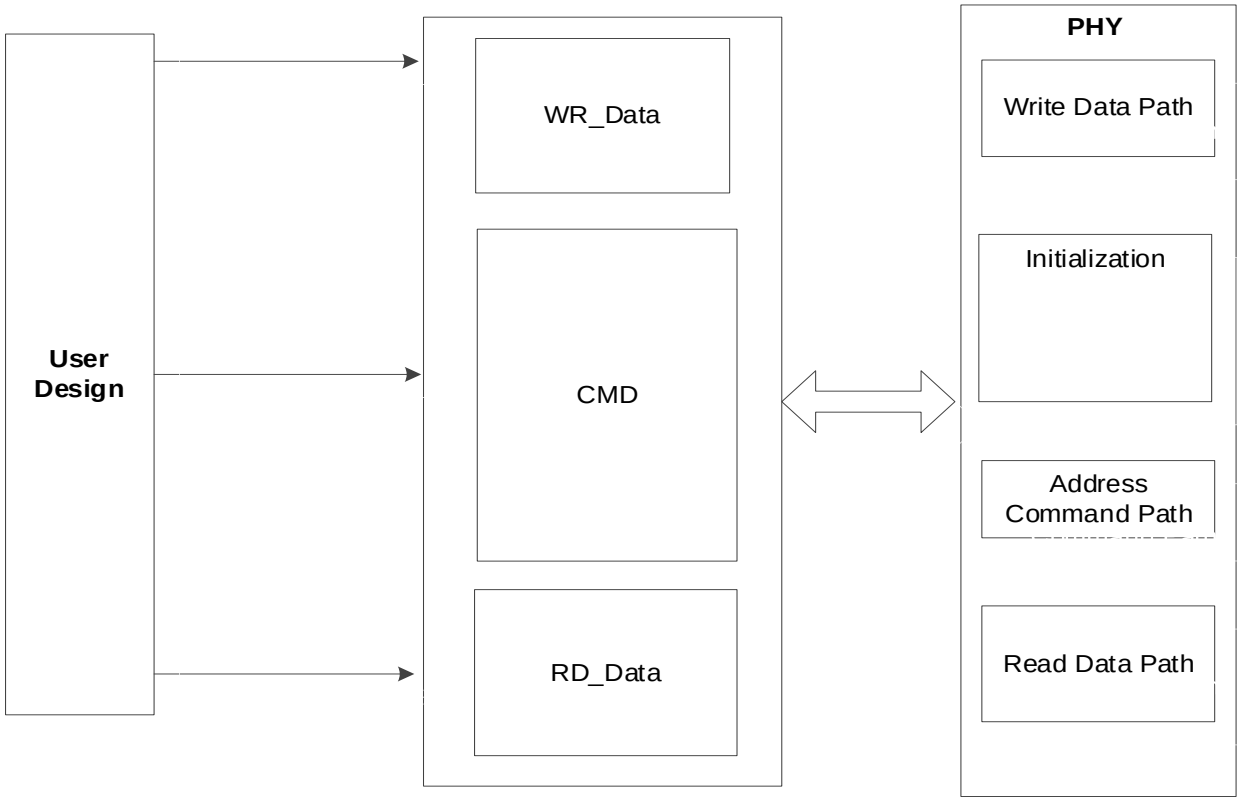
4.2 Memory Controller Logic

Memory Controller Logic is the logic module of the IP, which locates between User Design and PHY. The Memory Controller Logic receives the command, address, and data from the user interface and stores them in logical order.

The write, read and other commands that you sent are sorted and reorganized in Memory Controller Logic to combine a data form that complies with the HyperRAM protocol. During write operations, the Memory Controller Logic reorganizes and buffers the data to meet the initial latency requirements between commands and data. During read operations, it samples and reorganizes the retrieved data to restore it to the correct format.

The HyperRAM Memory Controller consists of the following main modules, including the CMD unit, the WR_Data unit, the RD_Data unit, etc. The main structure is shown in Figure 4-2.

Figure 4-2 HyperRAM Memory Controller Logic Basic Structure

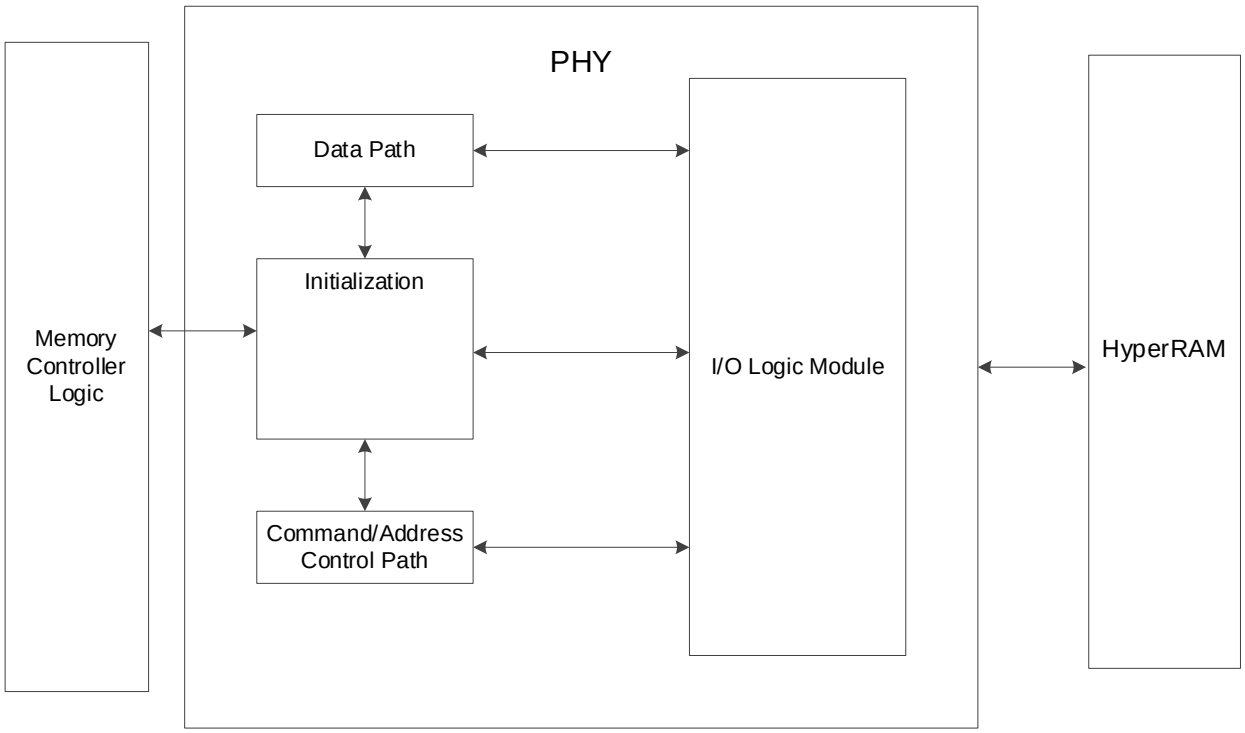


4.3 PHY

The PHY provides the physical layer definition and interface between Memory Controller Logic and the external HyperRAM. It receives the commands and data from the Memory Controller Logic and provides the HyperRAM interface with signals that meet the timing and sequence requirements.

The basic structure of the PHY includes four modules: initialization module, data path, command/address control path and I/O logic module, as shown in Figure 4-3.

Figure 4-3 HyperRAM PHY Basic Structure



4.3.1 Initialization Unit

The initialization module is mainly used for the initialization and read-calibration after HyperRAM power on. After all initialization and read-calibration are finished, the signal "init_calib" will transition from low to high to indicate the completion of the initialization.

Power-on Initialization

According to the HyperRAM protocol, it needs to initialize the PSRAM after power on. This includes the reset, mode register configuration, and read calibration.

4.3.2 Data Path Unit

Data path includes write data and read data.

4.3.3 Control Path Unit

The command/address control path is a unidirectional path that receives the command and address signals sent by the Memory Controller Logic. It works in conjunction with the data path to handle write and read data timing parameters and sends the commands to the I/O logic module.

4.3.4 I/O Logic Unit

The Logic I/O module is mainly used to convert the clock domain of the data, command, and address signals received from the data path and command/address path.

4.4 Major Functions

The functions of the HyperRAM Memory Interface IP are as follows:

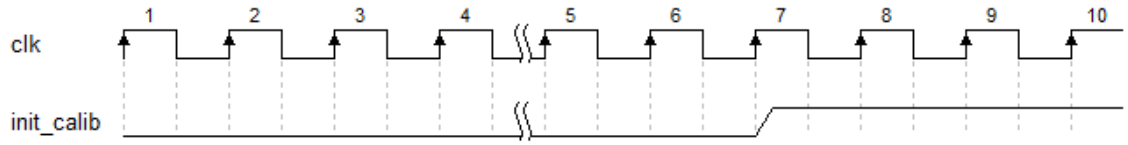
- Initializes the HyperRAM chip
- Sends the addresses and commands
- Writes data
- Reads data

4.4.1 Initialization

HyperRAM must be read calibrated to perform normal write and read operations. After power on, the HyperRAM will be initially read calibrated using the PHY and then returns the "init_calib" initialization mark.

The completion signal is returned to user after the initialization is completed, as shown in Figure 4-4.

Figure 4-4 Initialization Completion Signal Timing Diagram



4.4.2 Send Addresses and Commands

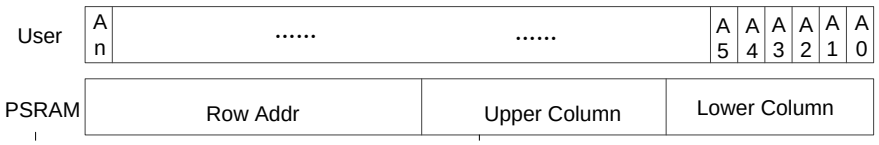
You can send operation commands and addresses through the addr, cmd, and cmd_en ports.

- addr is the address data port.
- During continuous address write operations, the address increments by burst length/2 between successive operations. The same applies to continuous address read operations.
- cmd is the command data port.
- cmd_en is the address and command enable signal, active high.

In the application, a mapping relationship exists between the address bus of user interface and the physical memory ROW, Upper Column, and Lower Column. In this design, it is in ROW-Upper Column-Lower Column order. The addressing scheme is as shown in Figure 4-5. In the application,

you only need to give the address as needed, and the mapping relationship is excluded.

Figure 4-5 Addressing Scheme in Row-Column Order



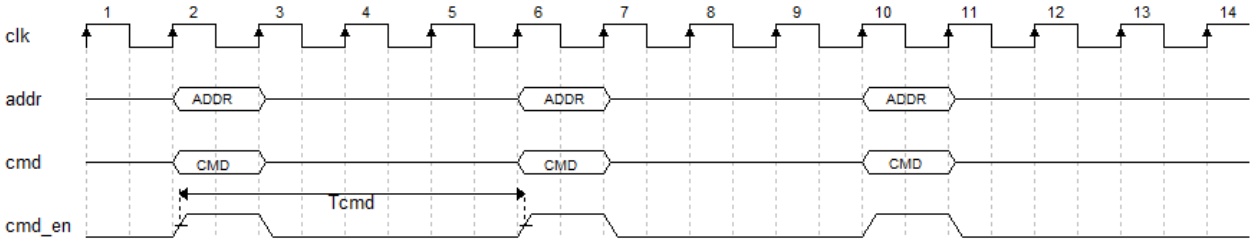
The commands that you sent through the cmd interface are as shown in Table 4-1.

Table 4-1 cmd

Command	cmd
Read	1'b0
Write	1'b1

At the user interface, the timing between the command, address, and enable signals is as shown in Figure 4-6.When the cmd_en is high, the cmd and the addr are valid at this time.

Figure 4-6 Command, Address, and Enable Signal Timing



When used in the application, the interval between two commands (write-read/read-write/write-write/read-read) must meet the minimum interval cycles (Tcmd cycle count in Figure 4-6). For example, when the burst length is 16, the command interval is at least 15 clock cycles; when the burst length is 32, the command interval is at least 19 clock cycles; when the burst length is 64, the command interval is at least 27 clock cycles; when the burst length is 128, the command interval is at least 43 clock cycles. During high-speed read and write operations, the Tcmd cycle count should be appropriately increased, as shown in Table 4-2.

Table 4-2 Relationship between Tcmd Cycle and Burst Length

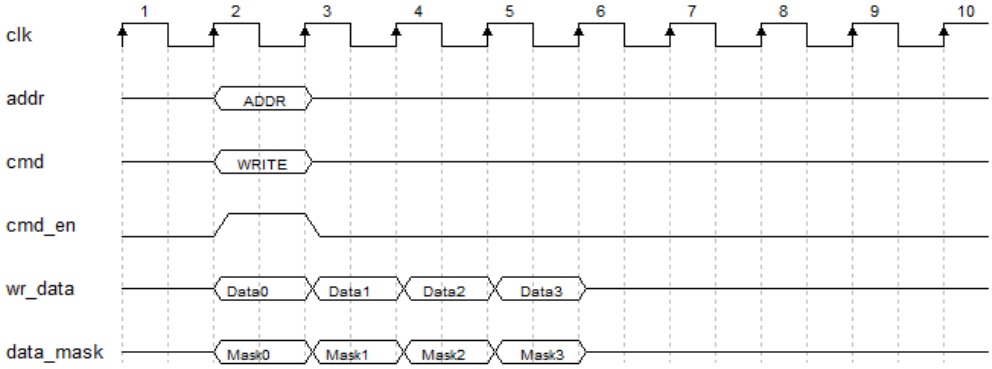
Burst length	Tcmd (interval between two commands, regardless of read or write), with HyperRAM speeds of 166M and below	Tcmd (interval between two commands, regardless of read or write), with HyperRAM speed of above 166M
128	43 user clocks	48 user clocks
64	27 user clocks	32 user clocks
32	19 user clocks	24 user clocks
16	15 user clocks	20 user clocks

4.4.3 Write Data

You can send the data to Gowin HyperRAM Memory Interface IP through the ports of wr_data and data_mask, etc. The write data will be sent to the HyperRAM chip after being processed.

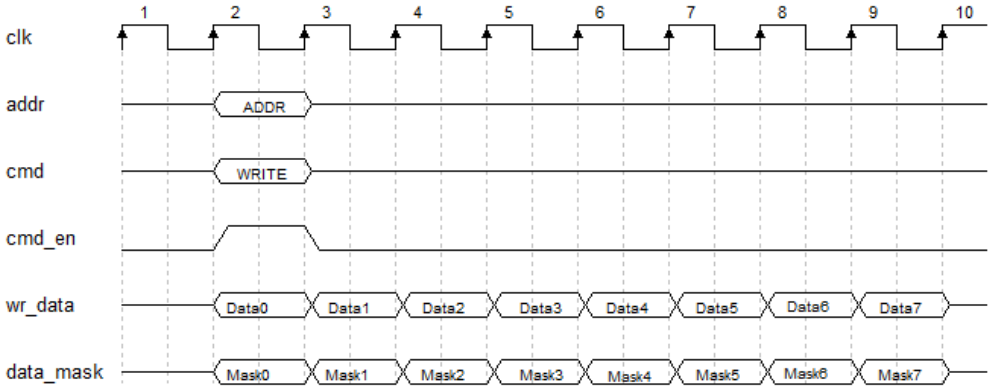
- The wr_data is a write data port.
- Data_mask a write mask port. If the mask function is not used, it can be set to 0.
- There are various timing cases between the write data channel and the command channel. As shown in Figure 4-7, taking a burst length of 16 as an example, the write data occupies 4 clock cycles.

Figure 4-7 Write Data Port Timing



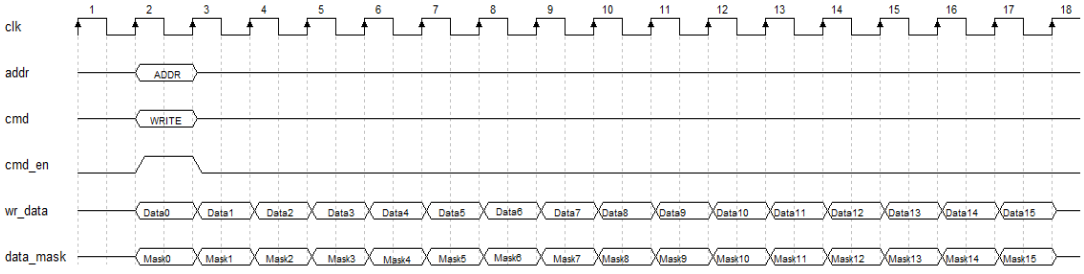
- The write data occupies 8 CLK cycles if the burst length is 32, as shown in Figure 4-8.

Figure 4-8 Write Data Timing with the Burst Length of 32



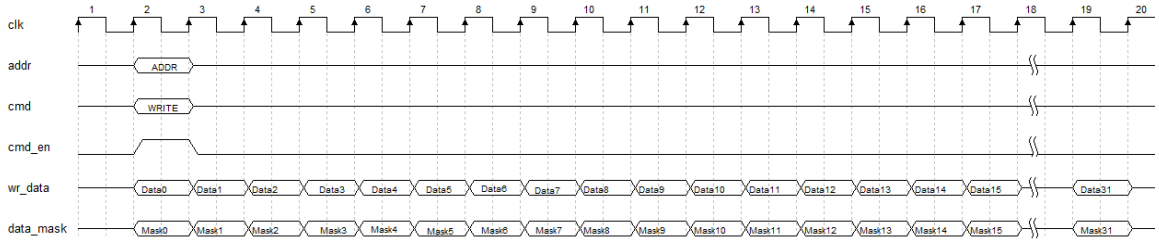
- The write data occupies 16 CLK cycles if the burst length is 64, as shown in Figure 4-9.

Figure 4-9 Write Data Timing with the Burst Length of 64



- The write data occupies 32 CLK cycles if the burst length is 128, as shown in Figure 4-10.

Figure 4-10 Write Data Timing with the Burst Length of 128

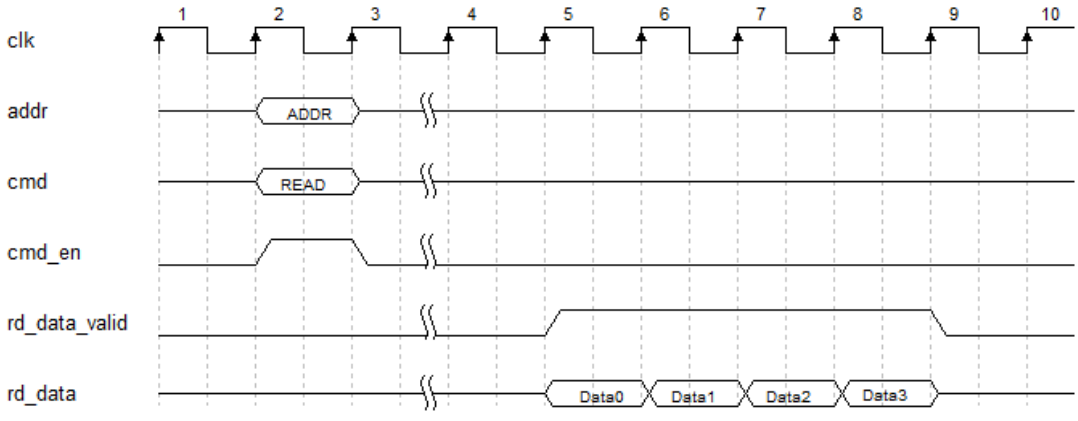


4.4.4 Read Data

You can read the data from the HyperRAM using the ports rd_data and rd_data_valid.

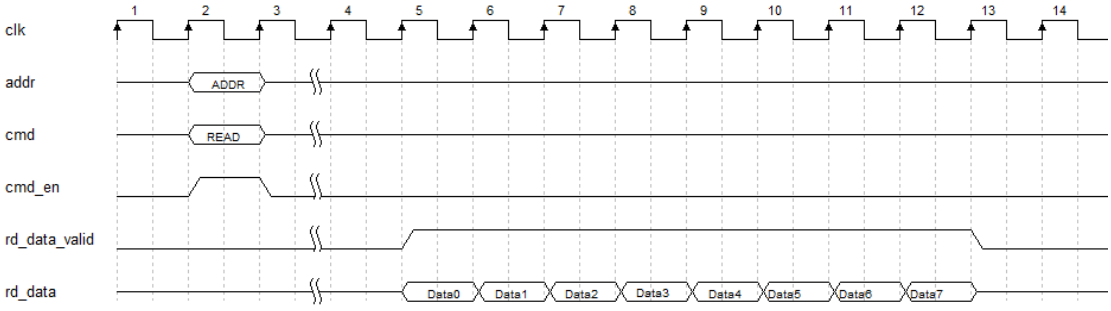
- The rd_data port is the read data port for the returned data.
- The rd_data_valid port indicates the validity of the read data. When it is high, it indicates that the returned rd_data is valid.
- There are many timing cases between the read data channel and the command channel. Take the 16 burst length as an example.

Figure 4-11 Read Data Port Timing



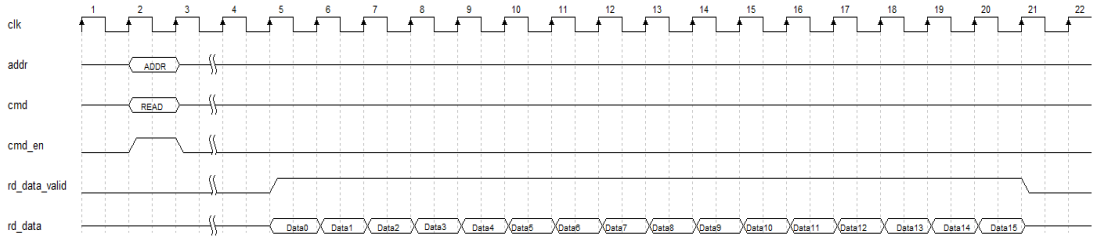
- The read data occupies 8 CLK cycles if the burst length is 32, as shown in Figure 4-12.

Figure 4-12 Read Data Timing with the Burst Length of 32



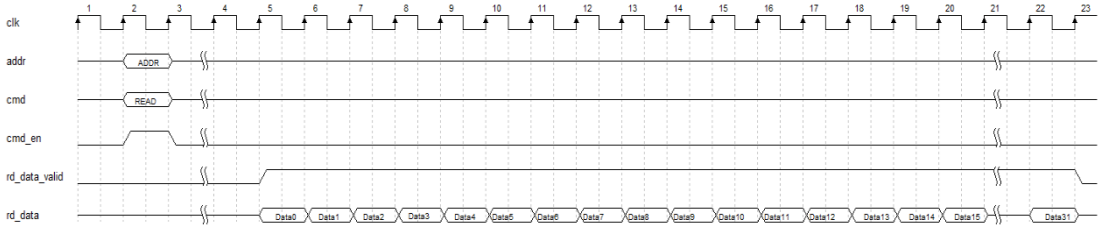
- The read data occupies 16 CLK cycles if the burst length is 64, as shown in Figure 4-13.

Figure 4-13 Read Data Timing with the Burst Length of 64



- The read data occupies 32 CLK cycles if the burst length is 128, as shown in Figure 4-14.

Figure 4-14 Read Data Timing with the Burst Length of 128



5 Ports List

The I/O ports of Gowin HyperRAM Memory Interface IP are shown in Table 5-1.

Table 5-1 I/O List of Gowin HyperRAM Memory Inteface IP

Signal	Data Width	I/O	Description
User Interface			
addr	ADDR_WIDTH	Input	Address input
cmd	1	Input	Command channel
cmd_en	1	Input	Command and address enable signals: 0: invalid 1: valid
rd_data	4*DQ_WIDTH	Output	Read data channel
rd_data_valid	1	Output	rd_data valid signal: 0: invalid 1: valid
wr_data	4*DQ_WIDTH	Input	Write data channel
data_mask	MASK_WIDTH	Input	Provides the masking signal for wr_data
clk	1	Input	Reference input clock, it is usually generated from on-board crystal oscillator clock
init_calib	1	Output	Initialization completed signal
clk_out	1	Output	The user-design clock, with a frequency of 1/2 Memory Clk
rst_n	1	Input	Input reset signal: 0: valid 1: invalid
memory_clk	1	Input	You can input chip working clock, which is generally a high-speed clock multiplied by the PLL, or not use PLL
pll_lock	1	Input	If the memory_clk is a PLL multiplied input, this port is

Signal	Data Width	I/O	Description
			connected to PLL's pll_lock pin If you do not use PLL, this port is connected to 1'b1.
HyperRAM Interface			
O_hpram_cs_n	CS_WIDTH	Output	Chip selected, active-low
O_hpram_ck	CS_WIDTH	Output	A clock signal provided for HyperRAM
O_hpram_ck_n	CS_WIDTH	Output	Composes the differential signal with the O_hpram_ck
O_hpram_reset_n	CS_WIDTH	Output	HyperRAM reset signal
IO_hpram_dq	DQ_WIDTH	Bidirection	HyperRAM data
IO_hpram_rwds	RWDS_WIDTH	Bidirection	HyperRAM MCL data selection signal and mask signal

6 Parameter Configuration

Gowin HyperRAM Memory Interface IP supports HyperRAM devices. You can configure various static parameters and timing parameters according to the design requirements. The specific parameters are as shown in Table 6-1.

Table 6-1 Static Parameter Options of Gowin HyperRAM Memory Interface IP

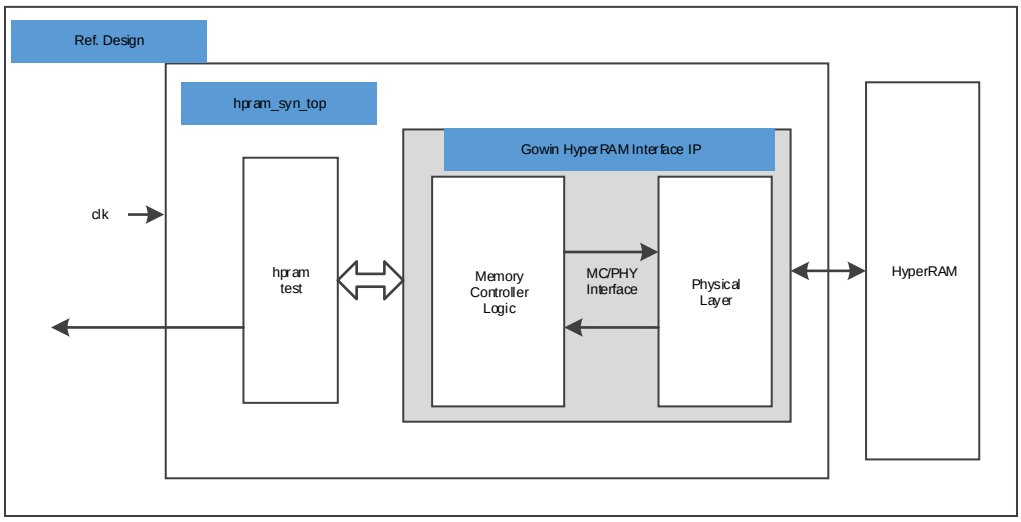
Name	Description	Option
Memory TYPE	HyperRAM type	W956x8MKY/IS66WVH32M8DBLL/ S27KS0641/Custom
CLk Ratio	The CLK ratio of the PSRAM PHY to internal logic clock, and you cannot operate it.	1:2
Memory Clock	The operating frequency that you expected	50-100/50-166/50-200(MHz)
Psram Width	DQ width of HyperRAM	8
Dq Width	The data bit width that you required	8,16, 24,32, 40,48, 56,64
Addr Width	Address width that you filled according to the specific chip	22/24/Others
Data Width	User data bit width	4*Dq Width
CS Width	Chip selection width	Dq Width/Psram Width
Mask Width	Mask width	Data Width/Psram Width
Burst Mode	Data burst length	16, 32, 64, 128
Burst Num	Burst data number	Burst Mode/4
Fixed Latency Enable	Fixed latency enable	Fixed
Initial Latency	Initial latency	3, 4 , 5 ,6 , 7, 8
Drive Strength	Drive strength;	19, 22, 27,34, 46,67, 115
Deep Power Down	Deep power down	"OFF", "ON"
Hybrid Sleep Mode	Sleep mode	"OFF", "ON"
Refresh Rate	Refresh rate	"Normal", "1.5/2/4times"

Name	Description	Option
PASR	Self-refresh area	full, bottom_1/2,bottom_1/4,bottom_1/8, top_1/2, top_1/4, top_1/8.
Clock Type	Clock type	SIGNLE/DIFF

7 Reference Design

To quickly familiar with and use Gowin HyperRAM Memory Interface IP, a simple reference design is provided for you. The basic structure of reference is shown in Figure 7-1.

Figure 7-1 Block Diagram of Reference Design



In the reference design, the hpram_syn_top module serves as the top-level module, and its ports are connected to the input reference clock. The hpram_test module is used to generate the addresses, data, and read/write commands required by the Gowin HyperRAM Interface IP, and this module is synthesizable.

The hpram_test module generates n consecutive write signals and data, after which it performs n consecutive read operations on the written data, and performs data verification. After the verification is complete, it repeats the previous write and read operations in a loop. In this reference design, the memory chip W956x8MKY is selected; the Burst Mode is configured to 16 and the DQ width set to 8 bits. Users can adjust the Burst Mode as needed.

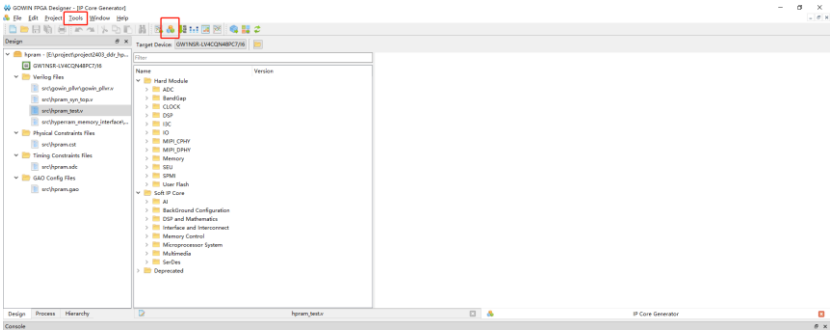
8 Interface Configuration

You can call and configure the IP using the embedded IP Core Generator tool in the IDE (V1.9.10.01 and above). In this chapter, take W956x8MKY HyperRAM as an example, introduce the configuration interface, configuration flow and the meaning of each configuration option.

1. Open IP Core Generator

After creating the project, you can click the "Tools" tab in the upper left, select and open the IP Core Generator via the drop-down list, or you can click "  " icon on the toolbar, as shown in Figure 8-1.

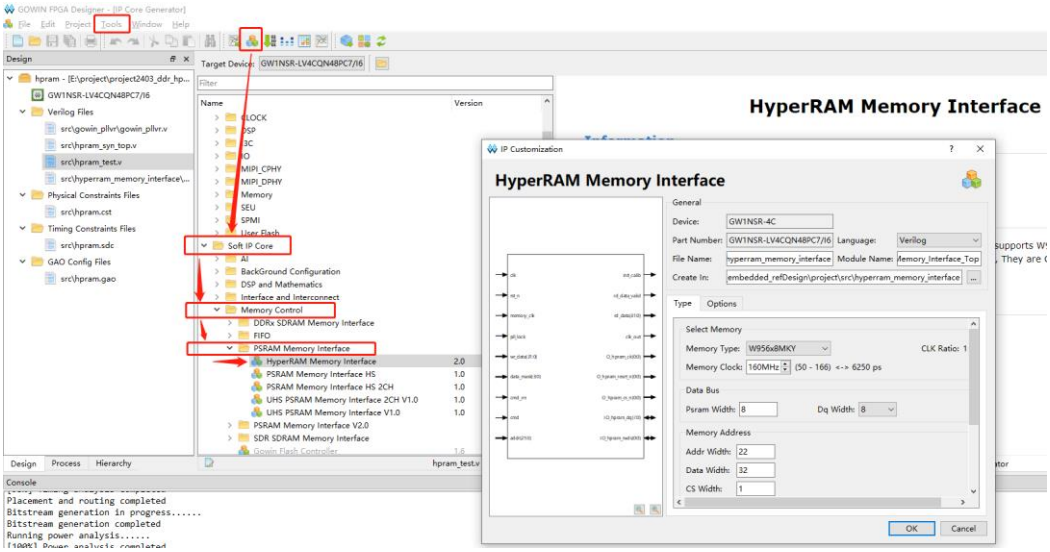
Figure 8-1 Open IP Core Generator



2. Open HyperRAM Memory Interface IP Core

Click the Memory Control option, double-click HyperRAM Memory Interface. HyperRAM Memory Interface embedded IP core opens, as shown in Figure 8-2.

Figure 8-2 Open HyperRAM Memory Interface embedded IP Core

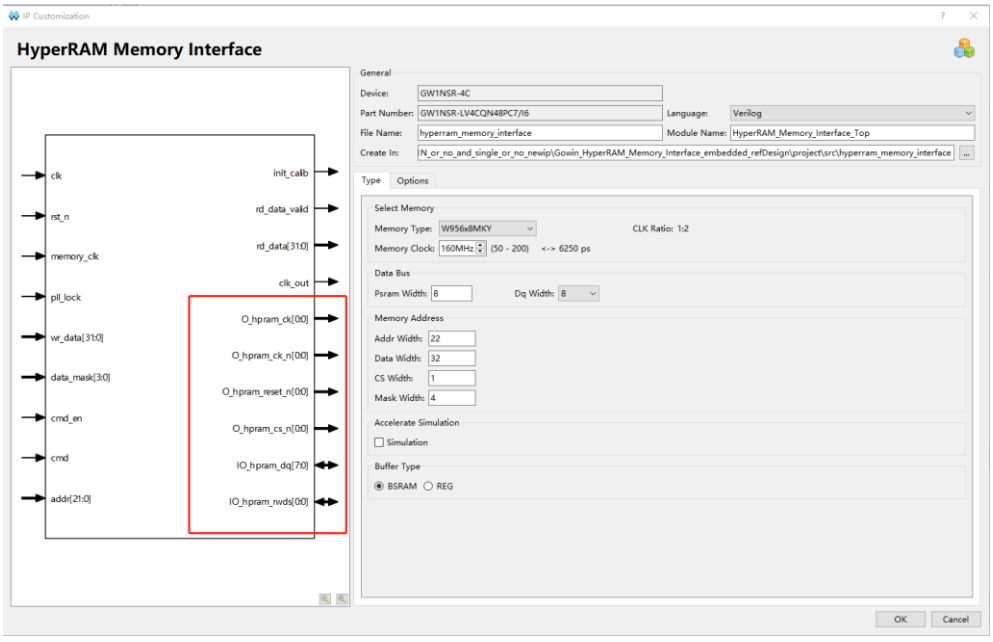


3. HyperRAM Memory Interface IP Core Port Interface

The Interface of the HyperRAM Memory Interface IP core is on the left, as shown in Figure 8-3.

The area outside the red box in the interface view is the interfaces between the HyperRAM Memory Controller and the user port. Users can connect their own designs to the HyperRAM Memory Interface IP to implement command and data transmission. The area inside the red box in the interface view is the interface between the physical interface (PHY) and the memory. Users can access and store the data through connecting the HyperRAM Memory Interface IP core to the desired memory chip. With different configuration information, the signal bit-width and the signal number will change accordingly.

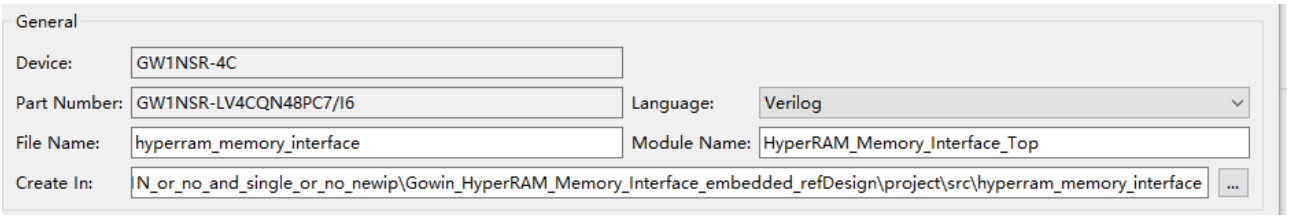
Figure 8-3 IP Core Interface



4. Configure the General Information

See the basic information in the upper part of the configuration interface. Take the GW1NSR-LV4CQN48PC7/I6 as an example. The "Module Name" option shows the generated top-level file name of the project, and the default value is "HyperRam_Memory_Interface_Top", and it can be modified. The "File Name" option shows the folder where the IP core files will be generated and where the necessary files for the HyperRAM Memory Interface IP core will be stored, and the default value is "hyperram_ memory_interface", and it can be modified. The "Create In" option shows the IP core files path, and the default is "…\src\hperram_memory_interface" under the project path, and it can be modified. The "Add to Current Project" option in the lower right is used to ask whether the generated IP should be directly added to your project; it is selected by default, as shown in Figure 8-4.

Figure 8-4 Basic Information Configuration Interface

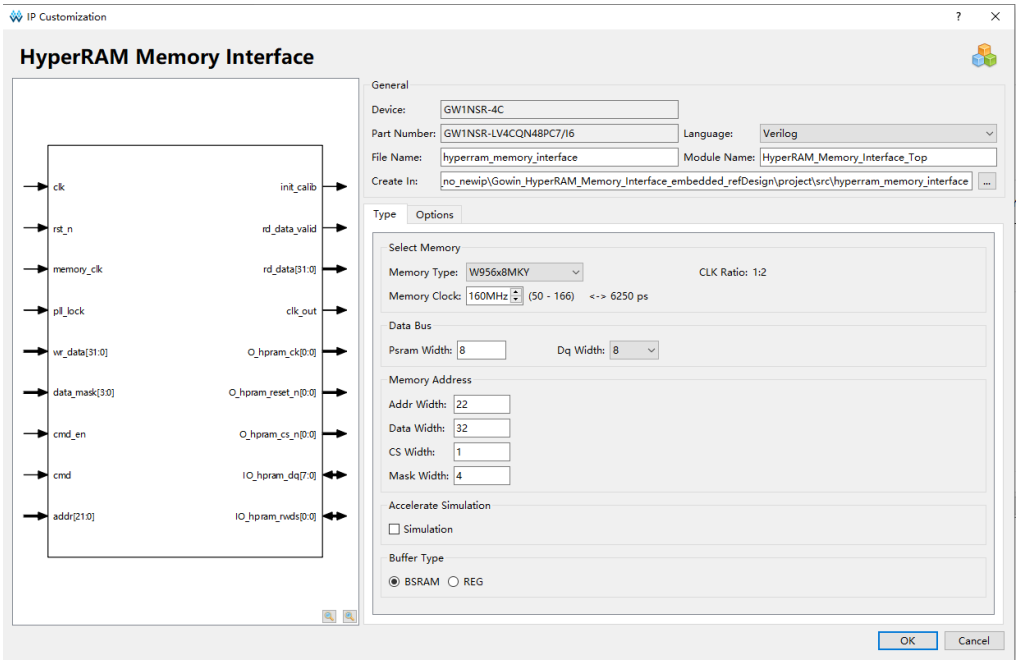


5. Type Tab

You can configure the basic information for the HyperRAM memory chip using "Type" tab.

- Select Memory
- Data Bus
- Memory Address: In "Memory Address" option, you can fill in the Address information of HyperRAM. You need to know the address width of the used chip; and the data equals to the ROW + Upper Column + Lower Column. After choosing the HyperRAM type, the software will be fill in the data automatically; if you choose "Custom", you need to fill in the data according to your used HyperRAM memory type.
- Accelerate Simulation: This option is used to speed up user simulation and can be checked, but it can not be unchecked for board-level testing, and regenerate the IP.
- Nonoperable

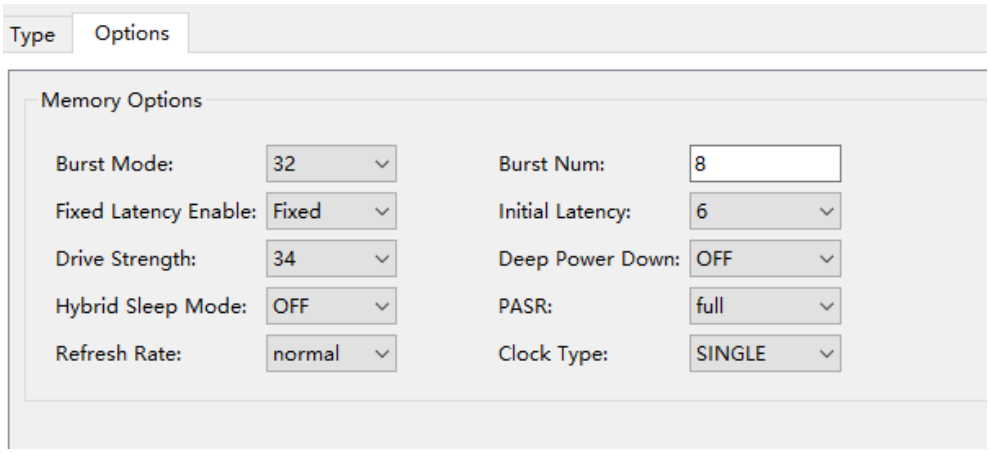
Figure 8-5 Type Tab



6. Options Tab

"Options" Tab is as shown in Figure 8-6, and take W956x8MKY HyperRAM as an example.

Figure 8-6 Options Tab



9 File Delivery

The delivery files for the Gowin HyperRAM Memory Interface IP include the documents and the reference design.

9.1 Documents

The document folder mainly contains PDF file of the user guide.

Table 9-1 Documents List

Name	Description
IPUG944, Gowin HyperRAM Memory Interface IP User Guide	Gowin HyperRAM Memory Interface IP User Manual (this manual).

9.2 Reference Design

The Ref. Design folder contains the netlist file for Gowin HyperRAM Memory Interface IP, the user reference design, the constraint file, the jitter elimination module, the top file, the project file folder, etc.

Table 9-2 Ref. Design Folder Contents

Name	Description
hpram_syn_top.v	The top module of reference design
hpram_test.v	Test stimulus generation module
HyperRam _Memory_Interface.vo	Gowin HyperRAM Memory Interface IP netlist file
hpram.cst	HyperRAM project physical constraints file
hpram.sdc	HyperRAM project timing constraints file
hpram.gao	Capture HyperRAM data
HyperRam _Memory_Interface	HyperRAM IP project file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