

Gowin RiscV_AE350_SOC 快速开发 **用户手册**

MUG1030-1.0, 2023-09-12

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版本信息

日期	版本	描述
2023/09/12	1.0	初始版本。

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1 关于本手册

1.1 手册内容

本手册以 Gowin[®] RiscV_AE350_SOC 硬件参考设计案例和软件编程参考设计案例为例,描述如何快速建立、配置、下载和调试硬件工程和软件工程,旨在帮助用户快速掌握 Gowin RiscV_AE350_SOC 的软硬件开发方法,节省开发时间,提高开发效率。

1.2 术语、缩略语

本手册中的相关术语、缩略语及相关释义如表 1-1 所示。

术语、缩略语	全称	含义
GPIO	Gowin Programmable IO	Gowin 可编程通用管脚
IDE	Integrated Development Environment	集成开发环境
MCU	Micro Controller Unit	微控制器单元
RISC-V	Reduced Instruction Set Computer V	第五代精简指令集计算机
SaG	Scattering and Gathering	散布和收集
SOC	System on Chip	片上系统
UART	Universal Synchronous and Asynchronous Receiver/Transmitter	通用同步和异步接收器/发 射器

表 1-1 术语、缩略语

1.3 技术支持与反馈

高云[®]半导体提供全方位技术支持,在使用过程中如有疑问或建议,可 直接与公司联系:

网址: <u>www.gowinsemi.com.cn</u>

E-mail: <u>support@gowinsemi.com</u>

Tel: +86 755 8262 0391

2 硬件设计方法

2.1 硬件目标

- DK-START-GW5AT138 V2.0
 - GW5AST-LV138FPG676AES
 - GW5AST-138B

2.2 软件版本

已测试软件版本:云源软件 Gowin_V1.9.9 Beta-3。

2.3 参考设计

...\ref_design\FPGA_RefDesign\DK_START_GW5AT138_V2.0\ae350 _demo。

2.4 用户手册

- MUG1031, Gowin RiscV_AE350_SOC 硬件设计用户手册
- <u>SUG100, Gowin</u> 云源软件用户指南
- <u>SUG940, Gowin</u>设计时序约束指南
- <u>SUG935</u>, Gowin 设计物理约束指南
- <u>SUG502</u>, Gowin Programmer 用户指南

2.5 设计流程

Gowin RiscV_AE350_SOC IP 设计流程,如下所示:

- 1. 高云半导体云源[®]软件的 IP 设计工具 "IP Core Generator", 配置 RiscV_AE350_SOC IP 选项,产生 RiscV_AE350_SOC IP 设计;
- 2. 云源软件的 IP 设计工具 "IP Core Generator", 配置 PLL_ADV IP 选项,产生 PLL_ADV IP,为 RiscV_AE350_SOC IP 提供时钟资源;

- 3. 硬件设计中,实例化 RiscV_AE350_SOC IP,实例化 PLL_ADV IP,加 入其他用户逻辑设计,连接各模块组成完整的顶层设计;
- 4. 参照所用开发板,加入物理约束,可以使用云源软件的物理约束工具 "FloorPlanner";
- 5. 参照软件时序分析报告,加入时序约束,可以使用云源软件的时序约束 工具 "Timing Constraints Editor";
- 6. 配置综合选项、布局布线选项和码流选项;
- 7. 云源软件的综合工具 "GowinSynthesis[®]",综合 RiscV_AE350_SOC 硬件设计,产生网表文件;
- 8. 云源软件的布局布线工具 "Place & Route", 布局布线网表文件, 产生 码流文件;
- 9. 云源软件的下载工具"Programmer",下载码流文件。

2.6 详细设计方法

2.6.1 建立工程

双击打开云源软件,新建 FPGA 设计工程。

例如:

- Series: GW5AST
- Device: GW5AST-138
- Device Version: B
- Package: FCPBGA676A
- Speed: ES
- Part Number: GW5AST-LV138FPG676AES

2.6.2 IP 设计

云源软件的 IP 设计工具 "IP Core Generator", 配置 RiscV_AE350_SOC 选项,产生 RiscV_AE350_SOC IP。

在 IP Core Generator 工具中选择 "Soft IP Core > Microprocessor System > Hard-Core-MCU > RiscV AE350 SOC 1.0", 打开 RiscV_AE350_SOC IP Core, 如图 2-1 所示。



图 2-1 RiscV_AE350_SOC IP Core

参照应用需求配置相应功能,例如 Instruction Memory、Data Memory、GPIO 和 UART2。

Instruction Memory

双击打开"Instruction Memory",配置指令存储器选项。

选择 "Embedded Instruction Memory", 开启系统内置的 SPI Flash Memory, 如图 2-2 所示。

	N.4	
struction	iviemory	
		embedded memory as instruction memory.
RESET_N		Extended Instruction Memory exports all ROM AHB bus signals for user level memory.
CORE_CLK		Embedded Instruction Memory is allowed to
	FLASH SPI CSN	erase, read and write flash as a peripheral.
AHB_CLK		
AP B_CLK	Rear an Miso	Options
	FLASH_SPI_MOST	
TMS IN	FLASH_SPI_CLK	Instruction Memory Select
	FLASH_SPI_HOLDN	Embedded Instruction Memory
	FLASH_SPI_WPN	☐ Flash Register R/W Mode
Direct	46360 500	O Extended Instruction Memory

图 2-2 Instruction Memory 配置

Data Memory

双击打开"Data Memory",配置数据存储器选项。

选择 "Embedded Data Memory", 开启系统内置的 DDR3 Memory, 如图 2-3 所示。

图 2-3 Data Memory 配置

Data Memory SOC is for running MCU data, incle embedded data memory mode a data memory mode. Embedded data memory is to embedded memory as data memory data memory exports all RAM AH for user level memory. Options Configurations Data Memory Select	?	×
SOC is for running MCU data, incl embedded data memory mode a data memory mode. Embedded data memory is to embedded memory as data mem data memory exports all RAM AH for user level memory. Options Configurations Data Memory Select		
CONTROL OF A	ding d extended onfigure ory. Extended 3 bus signals	d s v

GPIO

双击打开 GPIO, 配置 GPIO 选项。

选择 "Enable GPIO" 和 "Enable GPIO I/O Ports", 开启 GPIO 和 GPIO "INOUT" 类型端口, 如图 2-4 所示。

图 2-4 GPIO 配置

👶 GPIO	? ×
GPIO	&
	de-bounce functionality for input channels. The GPIO module is a peripheral of APB bus interface in AE350 SOC. If users enable GPIO, it could export GPIO signals for user level. - Base address: 0xF0700000 - End address: 0xF07FFFFF Option Configuration Enable GPIO Interface:
Ris ¢V AE350 SOC	Enable GPIO I/O Ports
	OK Cancel

UART2

双击 UART2, 配置 UART2 选项。

选择"Enable UART2",开启 UART2,如图 2-5 所示。

UART		?
UART		
RESET N CORE CLK DOR CLK	TDO OUT	The UART module is a peripheral of APB bus interface in AE350 SOC. If users enable UART1 or UART2, it could export UART1 or UART2 signals for user level.
AHB CLK APB CLK APB CLK AFC CLK TCK IN		UART1 UART2 - Base address: 0xF0200000 0xF0300000 - End address: 0xF02FFFFF 0xF03FFFFF.
TMS IN TRST IN TDI IN UART2 ROD		Options
UART2 CTSN UART2 CDSN UART2 DCDN UART2 DCDN	UART2 OUTIN	Configuration
RiseV A	E350 SOC	

2.6.3 用户设计

RiscV_AE350_SOC IP 设计

云源软件的 IP 设计工具 "IP Core Generator",完成 RiscV_AE350_SOC IP 配置后,单击 "OK",产生 RiscV_AE350_SOC IP 设计,如图 2-6 所示。



图 2-6 RiscV_AE350_SOC IP 设计

PLL_ADV IP 设计

云源软件的 IP 设计工具 "IP Core Generator", 配置 PLL_ADV IP 选项,产生 PLL_ADV IP 设计,为 RiscV_AE350_SOC IP 提供时钟资源。

在 IP Core Generator 工具中选择 "Hard Module > CLOCK > PLL_ADV 1.0",请参照参考设计的时钟配置,配置 PLL_ADV IP,产生 PLL_ADV IP 设计,如图 2-7 所示。

例如用于 RiscV_AE350_SOC 内核的 PLL_ADV IP:

- Clkout0: DDR clock
- Clkout1: CORE clock
- Clkout2: AHB clock
- Clkout3: APB clock
- Clkout4: RTC clock

用于 RiscV_AE350_SOC DDR3 Memory 的 PLL_ADV IP:

- Clkout0: DDR3 input clock
- Clkout2: DDR3 memory clock

											~
		General									
		Device:	GW5AST	GW5AST-138 GW5AST-LV138FPG676AES L		Dev	ice Version:	in: B			
		Part Number:	GW5AST			Lan	guage:	Verilog			
		File Name:	gowin_p	11		Mo	dule Name:	Gowin_PLL			
		Create In:	C:\Users	\liukai\Desl	ktop\gw5ast	t\ae350_de	mo\src\gov	win_pll			
clkin	ciko ut0 🛶	Common	Clkout0	Clkout1	Clkout2	Clkout3	Clkout4	Clkout5	Clkout6	Clkfb	out
enclk0	cikout1	CLKIN	CLKIN					PLL Reset			
enclk1		Clock Free	Clock Frequency(10~400): 50.000					PLL Reset			
nclk2	cikout2 🛶	Divider F	actor					PLL Power	Down		
enclk3	clkout3 🔶	Opposite	mic 🔿 St	atic 1	(1~64)				der Reset		
andid	clkoust 🔶							- CLKOUT D	vider Reset		
	clkout5 🔶	VCO Freque	ency:								
dio	diout5	CLKFB					L	ock			
clk6	Choose -	Source: 🖲	Internal	 Externa 	al	~	5	Enable Loc	k		
et	lock -	Divider F	actor								
		Oynar	mic 🔿 St	atic 1	(1~64)						
		ICP and LF	PF				c	Optional Port	5		
		ICPSEL						SSC			
		Oynai	mic 🔿 St	atic ICP1	~		5	Clock Enab	ole Ports		

图 2-7 PLL_ADV IP 设计

注!

- RiscV_AE350_SOC 的内核时钟由 "PLL_R[0] > clkout1"直连提供,必须使用 PLL_ADV IP 的 "clkout1"产生内核时钟。
- RiscV_AE350_SOC 的 DDR3 Memory 时钟由 "PLL_L[0] > clkout2" 直连提供,建议 使用 PLL_ADV IP 的 "clkout2" 产生 DDR3 Memory 时钟。

用户设计

硬件设计顶层模块中,实例化 RiscV_AE350_SOC IP,实例化 PLL_ADV IP,加入其他用户逻辑设计,连接各模块组成完整的硬件设计。

2.6.4 约束

物理约束

参照所用开发板,加入物理约束,可以使用云源软件的物理约束工具 "FloorPlanner"。

例如参考设计 DK-START-GW5AT138 V2.0 DVK Board 与 AICE-MINI+ 的 JTAG 接口的对应连接方式,如表 2-1 所示。

表 2-1 参考设计的 JTAG 物理约束

JTAG 接口	DVK Board	AICE-MINI+
GND	J3-8	P3
TMS	J3-3	P4
ТСК	J3-4	P6
VREF (3.3V)	J3-7	P7
TRST	J3-5	P10
TDO	J3-6	P11
TDI	J60-3	P12

注!

- RiscV_AE350_SOC 的内核时钟由 "PLL_R[0] > clkout1"直连提供,必须约束此
 PLL_ADV IP 的位置为 "PLL_R[0]"。例如, INS_LOC
 "u_Gowin_PLL_AE350/PLL_inst" PLL_R[0]。
- RiscV_AE350_SOC 的 DDR3 Memory 时钟由 "PLL_L[0] > clkout2"直连提供,建议 约束此 PLL_ADV IP 的位置为 "PLL_L[0]"。例如, INS_LOC

```
"u_Gowin_PLL_DDR3/PLL_inst" PLL_L[0]。
```

时序约束

参照软件时序分析报告,加入时序约束,可以使用云源软件的时序约束 工具 "Timing Constraints Editor"。

2.6.5 配置

综合选项

"Synthesize > General"综合选项配置,请参照硬件设计的实际需求 配置,如图 2-8 所示。

- Top Module/Entity: ae350_demo_top
- Verilog Language: System Verilog 2017

图 2-8 综合选项配置

🔆 Configuration	×
 Configuration Global Voltage Synthesize General Place & Route General Place Route Dual-Purpose Pin Unused Pin BitStream General sysControl Feature sysControl 	× Synthesize General Synthesis Tool: ● GowinSynthesis Top Module/Entity: ae350_demo_top Include Path: Include Path: IncluPre GowinSynthesis Verilog Language: System Verilog 2017 ▼ Looplimit: 2000 Show All Warnings Disable Insert Pad Ram R/W Check
	Ram R/W Check OK Cancel Apply

布局布线选项

布局布线选项配置,请参照硬件设计的实际需求配置,如图 2-9 所示。 例如 Dual-Purpose Pin:开启复用 SSPI、MSPI 和 CPU。

	×
Dual-Purpose Pin	
 Use JTAG as regular IO Use SSPI as regular IO Use MSPI as regular IO Use READY as regular IO Use DONE as regular IO Use RECONFIG_N as regular IO Use I2C as regular IO ✓ Use CPU as regular IO 	
	Dual-Purpose Pin Use JTAG as regular IO Use SSPI as regular IO Use READY as regular IO Use DONE as regular IO Use RECONFIG_N as regular IO Use I2C as regular IO Use CPU as regular IO

图 2-9 布局布线选项配置

码流选项

码流选项配置,请参照硬件设计的实际需求配置。

2.6.6 综合

云源软件的综合工具"GowinSynthesis[®]",综合 RiscV_AE350_SOC 硬件设计,产生网表文件,如图 2-10 所示。



2.6.7 布局布线

云源软件的布局布线工具 "Place & Route", 布局布线网表文件, 产生 码流文件, 如图 2-11 所示。

		\times
🔋 Ele Edit Project Jools Window Help		
🗋 🗁 🗟 👘 😑 🗠 🔺 🧏 🛍 🔯 👶 👫 👬 🖼 🖾 🏟 👬 🎜		- 8)
Process 8 × PnR Details		1
 Pors & Pins Report Place & Route Report Pins Analysis Report Pors & Pins Report Pors & Pins Report Pine Cast Part Agence Pine Cast Part Part Part Part Part Part Part Par	lm 0.363 lm 0.19s lm 0.162s 0.588s .43s ge = 972	: : MB
Resource		
		>
Design Process Hierarchy 💡 Start Page 😰 Design Summary 🔃 📄 ae350_demo.rpt.html 😰		
Console		5)
Generate file "C:\Users\liukai\Desktop\ae350_demo\impl\pnr\ae350_demo.rpt.html" completed Generate file "C:\Users\liukai\Desktop\ae350_demo\impl\pnr\ae350_demo.rpt.html" completed Generate file "C:\Users\liukai\Desktop\ae350_demo\impl\pnr\ae350_demo.rpt.html" completed Generate file "C:\Users\liukai\Desktop\ae350_demo\impl\pnr\ae350_demo.rpt.html" completed Mon May 22 11:31:06 2023 <		>

图 2-11 布局布线

2.6.8 下载

云源软件的下载工具"Programmer",下载码流文件。

云源软件, "Process > Program Device", 或主菜单"Tools > Programmer", 或工具栏 "↓", 打开 Programmer。

选择 Programmer 主菜单 "Edit > Configure Device",或工具栏 "**》**",配置下载选项,如图 2-12 所示。

- Access Mode: External Flash Mode 5AT
- Operation: exFlash Erase, Program 5AT
- Programming Options > File name: ae350_demo.fs
- External Flash Options > Device: Generic Flash
- External Flash Options > Start Address: 0x000000

Device configurat	ion		?	>
Device Operation -				
Access Mode:	External	Flash Mode 5AT		•
Operation:	exFlash H	Grase, Program 5AT		•
exFlash Erase, Pro	gram 5AT			
Programming Option	5			
Programming Option File name: //Users,	s liukai/Desktop	/ae350_demo/impl/pnr/ae3	50_demo.fs	
Programming Option File name: /Users,	s liukai/Desktop ialization	/ae350_demo/impl/pnr/ae3	50_demo.fs	
Programming Option File name: //Users, User Flash Init	s liukai/Desktop ialization	/ae350_demo/impl/pnr/ae3	50_demo.fs	
Programming Option File name: /Users, User Flash Init External Flash Opt	s liukai/Desktop ialization ions	/ae350_demo/impl/pnr/ae3	50_demo.fs	
Programming Option File name: /Vsers, User Flash Init External Flash Opt Device:	s liukai/Desktop ialization ions	/ae350_demo/impl/pnr/ae3 Generic Flash	50_demo.fs	••••
Programming Option File name: /Users, User Flash Init External Flash Opt Device: Start Address:	s liukai/Desktop ialization ions	/ae350_demo/impl/pnr/ae3 Generic Flash 0x000000	50_demo.fs	••••
Programming Option File name: /Users, User Flash Init External Flash Opt Device: Start Address:	s liukai/Desktop ialization ions	/ae350_demo/impl/pnr/ae3 Generic Flash Dx000000	50_demo.fs	•

图 2-12 下载选项配置

单击"Save",完成下载选项配置。 单击工具栏"**季**",下载码流文件。

3 软件设计方法

3.1 软件版本

已测试软件版本: RiscV_AE350_SOC_RDS_v1.0_win

3.2 参考设计

 $...\label{eq:linear} \label{eq:linear} \end{tabular} \label{eq:linear} \end{tabular} \label{eq:linear} \end{tabular} \label{eq:linear} \end{tabular} \end{$

3.3 用户手册

- MUG1029, Gowin RiscV AE350 SOC 软件编程用户手册
- MUG1025, Gowin RiscV AE350 SOC RDS 软件用户手册
- <u>SUG502, Gowin Programmer 用户指南</u>

3.4 详细设计方法

3.4.1 建立软件工程

步骤1

双击打开 RDS 软件,项目创建视图(Andes Project Creator)中,设置以下选项:

- "Connection Configuration",选择"ICE"
- "Project Language",选择"C"
- "Chip Profile",选择"GOWIN-AE350 > ADP-AE350-A25-GOWIN" 单击"Create Project…",如图 3-1 所示。

nnection Configuration Simulator AndeSim 🗸 🔘	ICE ICE ~		Project Language ● C ○ C++	Create Pro
p Profile (Double click to cre	ate project)			
hip Profile Name	Chip ID	CPU		
GOWIN-AE350				
ADP-AE350-A25-GOWIN	ADP-AE350-A25-GOWIN	[A25]		

图 3-1 Create Project...

步骤 2

设置以下 C Project 信息:

- "Project name"
- "Location"
- "Project type",选择"Empty Project"
- "Toolchains",选择"nds32le-elf-mculib-v5"

单击 "Next",如图 3-2 所示。

图 3-2 C Project

A C Project			×
C Project Create C project of selected type Chip Profile: ADP-AE350-A25-GOWIN			2
Project name: ae350_demo ✓ Use default location Location: D:\RDS5\workspace\ae350_demo Choose file system: default ∨		B <u>r</u> owse	
Project type: Toolchains: Andes Executable Empty Project Hello World ANSI C Project Andes Shared Library Andes Static Library Show project types and toolchains only if they are supported	ib-v5 ib-v5d ib-v5 ib-v5d ib-v5d	ne platfo	<pre> * * * * </pre>
(?) < <u>Back</u> <u>N</u> ext > <u>Finish</u>		Cance	əl

步骤 3

设置部署平台和配置,例如,"Debug"或"Release",单击 "Finish",如图 3-3 所示。

图 3-3 Select Configurations

A C Project	– 🗆 X
Select Configurations Select platforms and configurations you wish to deploy on	Ď
Project type: Andes Executable Toolchains: nds32le-elf-mculib-v5 Configurations:	
☑ స Debug ☑ స Release	Select all Deselect all Advanced settings
Use "Advanced settings" button to edit project's properties Additional configurations can be added after project creati Use "Manage configurations" buttons either on toolbar or	on. on property pages.
? < <u>Back</u> <u>N</u> ext > <u>Fini</u>	sh Cancel

步骤4

参照应用需求,调用 RiscV_AE350_SOC 软件编程函数库,编写应用程序。

3.4.2 配置软件工程

项目资源管理器视图(Project Explorer View)中,右单击选定的软件 工程,下拉菜单中选择 "Build Settings", "Settings"对话框中,参照应用 需求配置 "Tool Settings",如图 3-4 所示。

图 3-4 Build Settings



Andes C Compiler > Directories

选择 "Andes C Compiler > Directories > Include paths (-I)",指定软件工程引用的头文件的路径,如图 3-5 所示。

- "\${workspace_loc:/\${ProjName}/src/bsp/ae350}"
- "\${workspace_loc:/\${ProjName}/src/bsp/config}"
- "\${workspace_loc:/\${ProjName}/src/bsp/driver/ae350}"
- "\${workspace_loc:/\${ProjName}/src/bsp/driver/include}"
- "\${workspace_loc:/\${ProjName}/src/bsp/lib}"
- "\${workspace_loc:/\${ProjName}/src/demo}"

Model and Alexandre and Ale	Include paths (-I)	🛃 💼 😭 🖓 -
🛚 🛞 Andes C Compiler	*/workspace_loc:/\$/ProiName\/src/bsp/ae350*	-
Preprocessor	"\${workspace_loc;/\${ProjName}/src/bsp/config}"	
🖄 Symbols	"\${workspace_loc:/\${ProjName}/src/bsp/driver/ae350}"	
🖄 Directories	"\${workspace_loc:/\${ProjName}/src/bsp/driver/include}"	
🖄 Optimization	"\${workspace_loc:/\${ProjName}/src/bsp/lib}"	
🖄 Debugging	"\${workspace_loc:/\${ProjName}/src/demo}"	
🖄 Warnings		
🖄 Miscellaneous		
🛞 Andes C Linker		
🖄 General		
🖉 Libraries		
Miscellaneous		
🖉 Loaded Address		
🛞 Andes Assembler		
🖄 General		
🛯 🛞 NM (symbol listing)		
🖄 General		
🛞 Readelf (ELF info listing)		
🖄 General		
🛞 Objdump (disassembly)		
🖄 General		
🛞 Objcopy (object content copy)		
🖄 General		
🛞 Size (section size listing)		
🖄 General		
🛞 LdSaG Tool		
🖄 General		

图 3-5 选择 Andes C Compiler > Directories

Andes C Compiler > Optimization

选择 "Andes C Compiler > Optimization", 指定软件工程的优化等级 和代码模型等,如图 3-6 所示。

- Optimization Level: -Og : Optimize for speed with better debug ability • than O1
- Code Model: medium
- Remove unused function sections (-ffunction-sections): 开启
- Remove unused data sections (-fdata-sections): 开启

🛞 Tool Settings 🎤 Build Steps Build Art	tifact 🗟 Binary Parsers	8 Error Parsers
 inds32le-elf-mculib-v5 Configurations indes32le-elf-mculib-v5 Configurations Preprocessor Symbols Directories Optimization Debugging Warnings Miscellaneous Wiscellaneous Some Andes C Linker General Libraries Miscellaneous Loaded Address Andes Assembler General Some Some Address NM (symbol listing) General Some General Some Content copy) General Size (section size listing) General General Size (section size listing) General 	Optimization Level Code Model Other optimization flags □ Link Time Optimization ☑ Remove unused functio ☑ Remove unused data s	-Og : Optimize for speed with better debuggability than -O1 medium (
	<	>

图 3-6 选择 Andes C Compiler > Optimization

Andes C Compiler > Debugging

选择 "Andes C Compiler > Debugging", 指定软件工程的调试等级, 如图 3-7 所示。

例如: Debug Level: Maximum (-g3)

图 3-7 选择 Andes C Compiler > Debugging



Andes C Compiler > Miscellaneous

选择 "Andes C Compiler > Miscellaneous", 指定软件工程的其他各种选项, 如图 3-8 所示。

例如:

- Other flags: -c -fmessage-length=0 -fno-builtin -fomit-frame-pointer fno-strict-aliasing
- Compiler to use: gcc

图 3-8 选择 Andes C Compiler > Miscellaneous



LdSaG Tool > General

选择 "LdSaG Tool > General", 指定 SaG 文件, 如图 3-9 所示。

- Generate linker script: 开启
- Linker script template: \$(ANDESIGHT_ROOT)/utils/nds32_template_v5.txt
- SaG file: \${ProjDirPath}/src/bsp/sag/ae350-ddr.sag

Model and American Action and American Acti	Generate linker scri	pt	
🛚 🛞 Andes C Compiler	Linker script template	\$(ANDESIGHT_ROOT)/utils/nds32_template_v5.txt	<u>B</u> rowse
Preprocessor	SaG file	\$(ProiDirDath)/srs/hsp/sag/ag250_ddr.cog	Province
Bymbols	340 1116	sterojonradi//src/osp/sag/aesso-ddi.sag	<u>b</u> rowse
Directories	Other flags		
Warnings			
Miscellaneous			
Miscelinieous			
General			
Libraries			
Miscellaneous			
Loaded Address			
🖉 🐼 Andes Assembler			
🖄 General			
🖉 🔊 NM (symbol listing)			
🖄 General			
🗸 🛞 Readelf (ELF info listing)			
🖄 General			
Ø Objdump (disassembly)			
🖄 General			
Objcopy (object content copy)			
🖉 General			
Size (section size listing)			

图 3-9 选择 LdSaG Tool > General

Andes C Linker > General

选择 "Andes C Linker > General",指定软件工程的链接脚本文件,如 图 3-10 所示。

- Do not use standard start files (-nostartfiles): 开启
- Linker Script (-T): \$(LDSAG_OUT)

图 3-10 选择 Andes C Linker > General

注!

此选项关联于 "LdSaG Tool > General" 选项,如果已配置 SaG 文件,此链接脚本文件由 SaG 文件产生,否则须手动指定。

Objcopy (object content copy) > General

选择 "Objcopy (object content copy) > General",指定软件工程产生 Binary 文件,如图 3-11 所示。

- Disable. (Do not auto-generate output file.): 关闭
- Create an output file in format: binary (Raw binary form)

🖄 nds32le-elf-mculib-v5 Configurations	Disable. (Do not auto-generate output file.)			
🗸 🛞 Andes C Compiler	Remove all symbol and relocation information. (-S)			
🖄 Preprocessor	Remove all debugging symbols _sections. (-g)			
🖄 Symbols	Remove all non-global symbols. (-x)			
🖄 Directories	Remove any compiler-generated symbols, (-X)			
🖉 Optimization	Create an output file in format binany (Raw binany form)			
🖉 Debugging				
🖄 Warnings	Other flags			
🖄 Miscellaneous				
🗸 🛞 Andes C Linker				
🖄 General				
🖉 Libraries				
Miscellaneous				
🖄 Loaded Address				
V 🛞 Andes Assembler				
🐸 General				
V 🛞 NM (symbol listing)				
B General				
Readelf (ELF info listing)				
General				
 Objdump (disassembly) Connect 				
General				
Concert Content copy)				
General General Science (Section 2)				
 Size (section size issung) Conservation 				
V IdeaG Tool				
General				

图 3-11 选择 Objcopy (object content copy) > General

3.4.3 配置目标

项目资源管理器视图中,右单击选定的软件工程,下拉菜单中选择 "Target Configuration",配置"Target Configuration"选项,指定软件工 程的 Chip Profile、Connection Configuration、Clean and Rebuild Project 等,如图 3-12 所示。

- Chip Profile: ADP-AE350-A25-GOWIN
- Connection Configuration
 - ICE
 - Bus 1 Port 4 [AICE-MINI+]
 - Auto
- Clean project: 建议开启
- Build project: 建议开启

ture Chan tout		
type filter text	Target Configuration	(2 + 2) +
 Resource Builders C/C++ Build Build Variables 	Configuration: Debug [Active]	lanage Configurations
Environment Logging Settings Target Configuration Tool Chain Editor > C/C++ General Project Natures Project References Refactoring History Run/Debug Settings Task Tags > Validation	Apply to All Configurations. Chip Profile ADP-AE350-A25-GOWIN	Browse
	Target Settings Connection Configuration O Simulator AndeSim v ICE ICE v Bus 1 Port 4 [AICE-MINI+] Auto	~
	Arguments Settings	
	ICE Misc Arguments Simulator Misc Arguments Memory Latency	
	Clean and Rebuild Project ☑ Clean project	
	Build project	

图 3-12 Target Configuration

3.4.4 构建软件工程

单击 RDS 软件工具栏 "**《**",构建软件工程,产生 Binary 文件,如图 3-13 所示。

图 3-13 构建软件	牛工程	
A C/C++ - ae350_demo/src/c	demo/main.c - AndeSight_RDS v5.1.1 — —	
<u>File Edit Source Refactor</u>	<u>N</u> avigate Se <u>a</u> rch <u>P</u> roject <u>R</u> un <u>W</u> indow <u>H</u> elp	
A 📬 🕶 🖶 🕤 🔦 🕶 🏜	▼ : ■ 🐁 🙀 🐐 ▼ 🗿 ▼ 🤮 🖋 ▼ 🌶 📴 🎟 🏷 🗢 ▼ 🖒 ▼ 🖒 ♥ 🖄 Quick Access :	} 🖻 🖬 🏘
Project E 🛛 🗖 🗖	Andes Project Creator 🕜 main.c 🛛	- 0
 ♀ ♀ ♀ ac350_demo > <l< td=""><td><pre>10/* 2 ***********************************</pre></td><td>Î</td></l<>	<pre>10/* 2 ***********************************</pre>	Î
< → #T № № 0 □ □ 2) □ ₩ № ∞ ▽	16 { 17 // 18 // User application codes 19 // 20 21 // Run UART demo	>
Dia Running Target	Console X TProperties Problems Prominal III Function Code Size III Static Stack Analysis 🔅 Call Hierarchy	
> 為 Targets		! 🗉 🕶 📑 🕶
	CDT Build Console [ae350_demo] Finished building: output/ae350_demo.hin	
	Invoking: Size (section size listing) riscv32-elf-size "ae350_demo.adx" tee output/.PHONY.size text code rodata data bss dec hex filename 10056 9088 968 0 720 10776 2a18 ae350_demo.adx Finished building: output/.PHONY.size	
		, v

3.4.5 下载软件工程

云源软件的下载工具"Programmer",下载 Binary 文件。

云源软件 IDE 或安装路径,打开 "Programmer",选择主菜单 "Edit > Configure Device",或单击工具栏 "孠",配置下载选项,如图 3-14 所示。

例如:

- Access Mode: External Flash Mode 5AT
- Operation: exFlash C Bin Erase, Program 5AT
- External Flash Options > Device: Generic Flash
- External Flash Options > Start Address: 0x600000
- FW/MCU/Binary Input Options > Firmware/Binary File: ae350_demo.bin

图 3-14 下载选项配置

🙀 Device configuration		?	\times
Device Operation			
Access Mode:	External Flash Mode 5AT 🔹		
Operation:	exFlash C Bin Erase, Program 5AT 🔹		
exFlash C Bin Erase, Program 5AT			
External Flash Options			
Device:	Generic Flash		•
Start Address:	rt Address: 0x600000		
FW/MCU/Binary Input Options			
Firmware/Binary File: space/ae350_demo/Debug/output/ae350_demo.bin			
	Save	Cance	el

单击"Save",完成下载选项配置。 单击工具栏"**季**",下载 Binary 文件。

3.4.6 调试软件工程

配置构建模式

修改 bsp\config\config.h,指定 BUILD_MODE 为"BUILD_LOAD", 重新构建软件工程,如图 3-15 所示。

图 3-15 配置构建模式

And And	es Project Creator 🕜 main.c 🕞 config.h 🛛	
19	/* AE350 core configurations */	^
20		
210	// Simulation select	
22	//#define CFG_SIMU // Do simulation on SID	
23		
24⊝	// Code coverage select	
25	//#define CFG_GCOV // Do code coverage support	
26		
27	// Li cache select	
28	#define CFG_CACHE_ENABLE	
29	// Ruild made coloct	
31	// build mode select	
320	/* /*	
33	* BUTLD LOAD : ae350-ilm.sag : debugging in TLM	
34	* : ae350-ddr.sag : debugging in DDR memory	
35	* BUILD BURN : ae350-ddr.sag : booting in Flash memory and running in DDR memory	
36	* BUILD XIP : ae350-xip.sag : booting and running in Flash memory	
37		
38	*/	
39	#define BUILD_MODE BUILD_LOAD	
40		
41		
42⊖	// The following is predefined settings	
43	// Please do not modify them	
44	#define BUILD_LOAD 1 // The program is loaded by GDB or eBIOS	
45	#define build bukk 2 // the program is burned to the flash, but run in KAM	a.t
40	#define bolto_AIP 5 // the program is burned to the flash, and run in flash (Xip linker sch	.pr
48	#if BUILD MODE == BUILD LOAD	
49	Hefine (F6 10AD	
15		× 1
		-

建立调试配置

项目资源管理器视图中,右单击选定的软件工程,下拉菜单中选择 "Debug As > Debug Configurations…",建立"MCU Program"模式的调 试配置,如图 3-16 和图 3-17 所示。

- Main > Project: ae350_demo
- Main > Program: Debug\ae350_demo.adx
- Startup > GDB Initialization Commands:
 - Reset and Hold
 - load
- Startup > Runtime Options: Set breakpoint at: main

图 3-16 建立调试配置

A Debug Configurations					- 0	×
Create, manage, and run config	urations				X	5.
📑 😰 🔕 🗎 🗙 📄 🗦 🗸	Name: ae350_demo Debug					
type filter text	📄 Main 🏇 Debugger 🕨 Sta	rtup 🦻 Source	Common 3	🕸 Exception Handling		
🐺 Application Program 🍰 Core Group	<u>P</u> roject:					^
✓ ∰ MCU Program	ae350_demo				<u>B</u> rowse	
💥 ae350_demo Debug	Program:					
Multi-Core Application F	Debug\ae350_demo.adx					١. ٦
Multi-Core MCU Progra			Variables	Search Project	Browse	i 11
a rarger Monitor			vanabies	Searc <u>ii</u> Project	b <u>r</u> owse	
	RTOS Awareness Debugging	: \${AUTO}			B <u>r</u> owse	
	Target Management Service					
	🗌 Flash Programming Before [ebugging				
	Automatically burn					
	Disable Memory Map					
						~
Filter matched 7 of 12 items				Re <u>v</u> ert	Apply	
?				<u>D</u> ebug	Clos	e

图 3-17 选择 Debug Configurations > Startup

A Debug Configurations – 🗆 X				
Create, manage, and run config	urations			
Image: Second system Image: Second system <th>Name: ae350_demo Debug Main * Debugger Startup I. GDB Initialization Commands Reset and Hold load </th>	Name: ae350_demo Debug Main * Debugger Startup I. GDB Initialization Commands Reset and Hold load			
< >> Filter matched 7 of 12 items	Reyert Apply			
?	<u>D</u> ebug Close			

开启调试会话

物理连接 Windows PC、AICE-MINI+、DK-START-GW5AT138 V2.0, 启动开发板。 选择 RDS 软件主菜单 "Debug Configurations > Debug" 或单击工具 栏 "*",开启调试会话,如图 3-18 所示。

例如:

- F: Terminate and Relaunch
- IP : Resume
- 3. Step Into
- 🕾 : Step Over
 - 🔹 📕 : Terminate

图 3-18 开启调试会话



