



# Gowin Software

## User Guide

SUG100-4.4.5E, 03/09/2026

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## Revision History

Date	Version	Description
06/17/2021	2.5E	<ul style="list-style-type: none"> <li>● Screenshots and their descriptions updated.</li> <li>● Synplify Pro removed.</li> </ul>
11/02/2021	2.6E	<ul style="list-style-type: none"> <li>● SSPI and MSPI dual-purpose pins updated.</li> <li>● The descriptions of -ireg_in_iob/-oreg_in_iob/-ioreg_in_iob updated.</li> <li>● MODE dual-purpose configuration removed.</li> <li>● Place &amp; Route BitStream: Power On Reset added.</li> <li>● The description of simulation files added.</li> </ul>
05/20/2022	2.7E	The description of Loading Rate updated.
07/28/2022	2.8E	<ul style="list-style-type: none"> <li>● Route Maxfan option added in Place &amp; Route.</li> <li>● The use of Library added.</li> </ul>
10/28/2022	2.9E	<ul style="list-style-type: none"> <li>● power_on_reset name updated.</li> <li>● Turn Off Bandgap option added in Bitstream.</li> <li>● DSim added.</li> <li>● Chapter 8 Appendix added.</li> </ul>
12/16/2022	3.0E	<ul style="list-style-type: none"> <li>● Device Version information added.</li> <li>● TclPre added in Synthesize.</li> <li>● The value Internal of Background Programming modified to GoConfig/UserLogic.</li> <li>● Generate Post-PnR VHDL Simulation Model File added in Place &amp; Route.</li> </ul>
03/31/2023	3.1E	<ul style="list-style-type: none"> <li>● The value GoConfig/UserLogic of Background Programming divided into GoConfig and UserLogic, and the related descriptions updated.</li> <li>● FloorPlanner and Timing Constraints Editor added to the toolbar.</li> <li>● The Tcl command -clock_route_order added.</li> </ul>
04/20/2023	3.2E	<ul style="list-style-type: none"> <li>● Place &amp; Route and Bitstream configurations updated.</li> <li>● Multi Boot and MSPI JUMP added in Bitstream configuration.</li> </ul>
05/25/2023	3.3E	<ul style="list-style-type: none"> <li>● Enable External Master Config Clock and Enable CMSER added in Bitstream configuration.</li> <li>● Global configuration added to set the VCCX value.</li> </ul>
06/30/2023	3.4E	The default value of Ram R/W Check option in Synthesis Configuration updated to unchecked.
08/18/2023	3.5E	<ul style="list-style-type: none"> <li>● For GW5A-25-MBGA121N, Use SSPI as regular IO option is checked and cannot be modified.</li> <li>● For GW5AT-138/GW5AST-138/GW5A-138 devices, the default values of Place input register to IOB, Place output register to IOB and Place inout register to IOB are modified to False.</li> <li>● For GW5AT-138/GW5AST-138/GW5A-138 devices, Replicate Resources option added to Place &amp; Route configuration.</li> </ul>
09/28/2023	3.6E	<ul style="list-style-type: none"> <li>● The Loading Rate values of GW5A(S)(T)-138 and GW5A(R)-25 updated.</li> <li>● The configuration option CMSER updated.</li> <li>● The MSPI JUMP option under the configuration option Feature sysControl updated.</li> </ul>
10/31/2023	3.7E	<ul style="list-style-type: none"> <li>● Figure 4-17 File Properties Dialog Box updated.</li> <li>● Tcl commands create_project and import_files added.</li> </ul>

Date	Version	Description
11/30/2023	3.8E	<ul style="list-style-type: none"> <li>● Program Device updated to Programmer.</li> <li>● A value of 2 added in Place option for Place &amp; Route configuration.</li> <li>● Loading Rate for LittleBee and Arora devices updated.</li> <li>● Tcl command run close added.</li> <li>● Output Base Name option added.</li> </ul>
02/02/2024	3.9E	<ul style="list-style-type: none"> <li>● GW2AN-9X and GW2AN-18X Loading Rate updated.</li> <li>● "Enable CMSER" updated to "Enable SEU Handler".</li> <li>● "Constraints" option added for configuring Frequency.</li> </ul>
03/29/2024	4.0E	<ul style="list-style-type: none"> <li>● GW5AT-60 Loading Rate values added.</li> <li>● Configuration option "Enable CTP" for Bitstream added.</li> </ul>
06/28/2024	4.1E	<ul style="list-style-type: none"> <li>● Tcl command open_project added.</li> <li>● Configuration option "VCC" added in Place &amp; Route.</li> <li>● Virtual input/output debugging tool added.</li> </ul>
08/09/2024	4.1.1E	<ul style="list-style-type: none"> <li>● The configuration option Place Option in Place &amp; Route now includes a new value of 3.</li> <li>● Descriptions of the open_project command updated.</li> </ul>
10/25/2024	4.2E	<ul style="list-style-type: none"> <li>● The configuration option Place Option in Place &amp; Route now includes a new value of 4.</li> <li>● A new value "GoConfig Mode1" added to the Background Programming configuration option for the devices Version C GW1N-2/GW1NR-2/GW1N-1P5.</li> <li>● A new configuration option "Incremental PnR" added to Place &amp; Route.</li> </ul>
12/31/2024	4.3E	<ul style="list-style-type: none"> <li>● A search function added to the Hierarchy window.</li> <li>● GoBert eye diagram analysis tool supported.</li> </ul>
03/07/2025	4.4E	<ul style="list-style-type: none"> <li>● The SPI Flash address access mode "Normal" updated to "Single" in BitStream configuration option.</li> </ul>
04/30/2025	4.4.1E	<ul style="list-style-type: none"> <li>● The interface dark mode added.</li> <li>● The search function added in the device selection window.</li> </ul>
06/27/2025	4.4.2E	A new configuration option and Tcl command added to specify the CSR file.
08/29/2025	4.4.3E	<ul style="list-style-type: none"> <li>● The right-click menu options for modules in the Hierarchy window updated in section 3.6.1 Right-click Menu.</li> <li>● A new configuration option "SerDes Retiming" added under Place &amp; Route in section 4.4.3 Synthesize.</li> <li>● Tcl command chapter removed.</li> </ul>
12/31/2025	4.4.4E	<ul style="list-style-type: none"> <li>● Updated sections 7.1 Functional Simulation Files and 7.2 Timing Simulation Files.</li> <li>● Updated the "Print BSRAM Initial Value" function for GW5A(S)(T)-138/GW5AT-75 devices.</li> <li>● Updated the batch data filling function of the Memory Initialization File Editor and the User Flash Initialization File Editor.</li> <li>● Added the "Co-Place IO Registers" configuration option to "Place &amp; Route".</li> </ul>
03/09/2026	4.4.5E	<ul style="list-style-type: none"> <li>● Updated the description in Section 7.1 Functional Simulation Files, adding prim_syn.vhd and prim_syn_a.vhd.</li> <li>● Added Table 4-2 Conditions for IBIS Generation Supported by Each Device in Section 4.3.3 Edit Project Configuration.</li> <li>● Added support for GW3A-20 devices.</li> </ul>

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# 1 About This Guide

## 1.1 Purpose

This manual describes Gowin Software installation and operation, and it aims to help you to be familiar with the using flow and improve design efficiency. The software screenshots in this manual are based on V1.9.12.02. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

## 1.2 Related Documents

The latest user guides are available on GOWINSEMI Website. You can find the related documents at [www.gowinsemi.com](http://www.gowinsemi.com):

- [SUG940, Gowin Design Timing Constraints Guide](#)
- [SUG935, Gowin Design Physical Constraints Guide](#)
- [SUG114, Gowin Analyzer Oscilloscope User Guide](#)
- [SUG282, Gowin Power Analyzer User Guide](#)
- [SUG502, Gowin Programmer User Guide](#)
- [UG285, Gowin BSRAM & SSRAM User Guide](#)
- [SUG283, Gowin Primitives User Guide](#)
- [UG286, Gowin Clock User Guide](#)
- [UG287, Gowin Digital Signal Processing \(DSP\) User Guide](#)
- [UG289, Gowin Programmable IO \(GPIO\) User Guide](#)
- [UG295, Gowin User Flash User Guide](#)
- [SUG1018, Arora V Design Physical Constraints User Guide](#)
- [UG299, Arora V Series Analog to Digital Converter \(ADC\) User Guide](#)
- [UG300, Arora V BSRAM & SSRAM User Guide](#)
- [UG304, Arora V Programmable IO \(GPIO\) User Guide](#)
- [UG305, Arora V Digital Signal Processing \(DSP\) User Guide](#)
- [UG306, Arora V Clock User Guide](#)

- [SUG1189, Gowin Virtual Input Output User Guide](#)
- [SUG1198, Gowin GoBert User Guide](#)

## 1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

**Table 1-1 Terminology and Abbreviations**

Terminology and Abbreviations	Meaning
CRC	Cyclic Redundancy Check
FloorPlanner	Physical Constraints Editor
FPGA	Field Programmable Gate Array
GAO	Gowin Analyzer Oscilloscope
GowinSynthesis	GowinSynthesis
GPA	Gowin Power Analyzer
GVIO	Gowin Virtual Input/Output
IP Core	Intellectual Property Core
PCIe	Peripheral Component Interconnect Express
PnR	Place & Route
Schematic Viewer	HDL Schematic Viewer
SEU Handler	Single-Event Upsets Handler
Tcl	Tool Command Language

## 1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: [www.gowinsemi.com](http://www.gowinsemi.com)

E-mail: [support@gowinsemi.com](mailto:support@gowinsemi.com)

# 2 Overview

## 2.1 Introduction

Gowin design system is an integrated circuit design and implementation tool specifically for GOWIN FPGA chips, and it has superior performance and easy to use. Gowin design system provides a comprehensive and optimized design for Gowin FPGA chips with the low-power and low-cost architecture, and it integrates the flow from RTL description to FPGA bitstream file generation, including design optimization, automatic design, and graphical interaction, etc.

### Functions

- The software system supports all functions of Gowin FPGA chips, covering the complete design flow from the functional description of the RTL circuit to the generation of FPGA bitstream file
- GowinSynthesis supports high-performance logic design and synthesis
- Supports automatic design and interactive graphical design in parallel
- Supports Centos6.8/7.0/7.3/7.5/8.2 (64 bits), Ubuntu18.04/20.04LTS, Win7/8/10/11 (32 bits/64 bits), Win XP (32 bits) systems
- Millions of gate-level software
- Supports VHDL, Verilog HDL and System Verilog languages
- Supports optimized architecture of Gowin products
- Supports original and high-performance algorithm PnR
- Precise timing analysis and timing report
- Clock analysis and control to ensure better timing performance
- Supports various timing and physical constraints
- Supports real-time monitoring of hardware circuit signals and storing them, along with timing waveform diagrams display
- Resource sharing can improve chip utilization and reduce cost

### Features

- Integrated design

- The design can be completed in stages or automatically as a package
- Supports command line mode or GUI mode
- You can use scripted design, and design any single module flexibly without affecting the integrated design throughout
- Can optimize design
  - Netlist optimization
  - Quick timing optimization analysis and design
  - Resource analysis and optimization
- Hierarchy design and analysis
  - Supports hierarchical netlist input and output
  - Supports flattened netlist input and output
  - Can hierarchically display, trace, and analyze netlist
- Flexible interactive graphic design
  - Simple and clear user interface
  - Displays projects, modules, tools and output
  - Design constraint input, selection and update
  - Quick timing analysis and report
  - Push button design

## 2.2 Supported Devices

Gowin Software supports the LittleBee family and Arora family chips. For the details of chip types, resources and packages, etc., you can visit Gowin official website.

- LittleBee family: [www.gowinsemi.com/en](http://www.gowinsemi.com/en)
- Arora family: [www.gowinsemi.com/en](http://www.gowinsemi.com/en)
- Arora V: <https://www.gowinsemi.com/en>

### **Note!**

The supported devices may vary according to the software version in use. Please refer to the software you use for more detailed device information.

## 2.3 Install and Start

The installation method in Windows system is the same; double-click the Gowin Software installation package and install according to the prompt. After installation, the shortcut will be created on the PC desktop by default. The installation method in the Linux system is to decompress the installation file.

You need to configure the license when you start Gowin Software for the first time after installation. The software license is a format contract

between the users and GOWINSEMI to define and limit the rights of users and the obligations of GOWINSEMI.

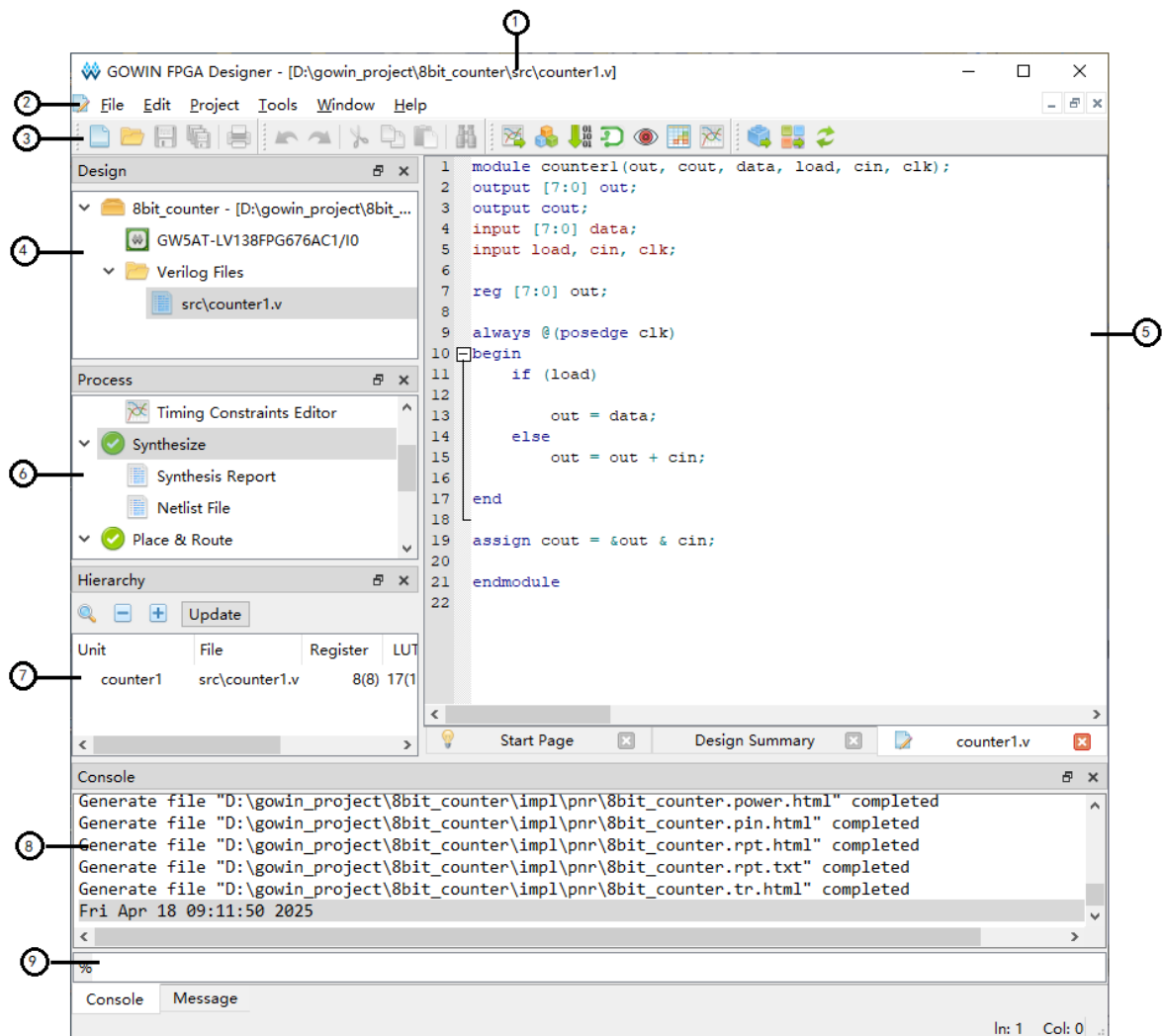
**Note!**

The installation address of Gowin Software does not support paths containing Chinese. For the details, see [SUG501, Gowin Software Quick Installation Guide](#).

# 3 Gowin Software GUI

Gowin Software GUI is as shown in Figure 3-1. It consists of the title bar, menu bar, tool bar, project area (Design), process area (Process), source file editing area, design hierarchy (Hierarchy), information output area and Tcl command editing area.

Figure 3-1 GUI



- |                            |                           |
|----------------------------|---------------------------|
| ① Title Bar                | ② Menu Bar                |
| ③ Tool Bar                 | ④ Project Area            |
| ⑤ Source File Editing Area | ⑥ Process Area            |
| ⑦ Design Hierarchy Area    | ⑧ Information Output Area |
| ⑨ Tcl Command Editing Area |                           |

## 3.1 Title Bar

Title bar shows the name of Gowin Software and the name of the currently opened file.

## 3.2 Menu Bar

The menu bar contains links to the tools and functionality that are commonly used in projects, including the File, Edit, Project, Tools, Window, and Help options. See the following for details.

### 3.2.1 File Bar

- Open Example Project...: Open an example project
- New... (Ctrl+N): Newly create
- Open... (Ctrl+O): Open an item
- Save ( Ctrl+S): Save the currently active item
- Save As...: Save the active item using a different file name
- Save All (Ctrl+Shift+S): Save all changed documents
- Close: Close an item
- Close All: Close all changed documents
- Close Project: Close current project
- Print Preview...: Print preview
- Print... (Ctrl+P): Print
- Recent Files: Show the files opened. You can click on the names of these files to re-open.
- Recent Projects: Show the projects opened. You can click on the names of these projects to re-open.
- Exit: Exit and close Gowin Software

### 3.2.2 Edit Bar

- Undo (Ctrl+Z): Undo your last operation
- Redo (Ctrl+Y): Redo your last operation
- Cut (Ctrl+X): Cut
- Copy (Ctrl+C): Copy
- Paste (Ctrl+V): Paste
- Select All (Ctrl+A): Select all

- Find & Replace (Ctrl+F): Find or replace key words
- Toggle Comment Selection (Ctrl+I): Add comments to the selected
- Increase Indent (Tab): Increase indent
- Decrease Indent (Shift+Tab): Decrease indent
- Macros
  - Start Record: Click Start Record, and the editing operations performed on editable files in the IDE will be recorded.
  - Stop Recording: Stop recording
  - Play Macro (Alt+R): Click Play Macro, and it will perform the recorded operations on the editable files.

### 3.2.3 Project Bar

- Archive Project: Archive project
- Restore Archived Project: Restore archived project
- Set Device: Set the device information of current project
- Configuration: Open configuration window
- Design Summary: Show details of current project

### 3.2.4 Tools Bar

- Start Page: Include Recent Projects, Quick Start, Tools, and User Manuals.
  - Recent Projects: Shows the recently opened projects, and up to 10 projects will be kept.
  - Quick Start: Include New Project..., Open Project..., and Open Example Project...
  - Tools: Include FloorPlanner, Timing Constraints Editor, and Programmer.
  - User Manuals: Manual for LittleBee, Manual for Arora, and Manual for Arora V.
- Gowin Analyzer Oscilloscope: Gowin analyzer oscilloscope
- Schematic Viewer: HDL design schematic viewer
- IP Core Generator: IP core generator
- Programmer: Programmer
- FloorPlanner: Physical constraints editor
- Timing Constraints Editor: Timing constraints editor
- DSIm: Simulation and Verification Cloud Platform
- GoBert: SerDes analysis tool
- Options: Includes Environment, Text Editor, and External Editor.

- Environment: Used to set IDE parameters, including Theme, Language, Toolbar Icon Size, and the default path of new project. here are two options for the theme: Classic and Dark. After setting the theme and language, you need to restart the IDE, then the settings will take effect.
- Text Editor: Used to set the text editor attributes, including font, font size, color, line numbers display, blank characters visualization, the current line and matching parentheses highlight.
- External Editor: Used to set the third-party text editor, and you can choose whether to always use the third-party editor to open the design file.

### 3.2.5 Window Bar



- Full Screen (F11): Display the IDE GUI in full screen
- Tile: Tile display
- Cascade: Cascade display
- Reset Layout: Used to restore initial settings
- Panels: Used to select whether to display the five panels, there are five sub-options available under this menu when a project is opened:  
Design, Hierarchy, Process, Message, and Console
- Start Page: Display start page in source file editing
- Design Summary: Display Design Summary page in source file editing area, including General and Target Device.
  - General: Project information, including project path and the synthesis tool used.
  - Target Device: Engineering device information, including version, package, speed grade, and core voltage.




















### 3.2.6 Help Bar

- View Help: View help documents of output information during compilation.
- Contact Us: Click to contact us
- Manage License...: Manage license, and you can refer to [SUG501. Gowin Software Quick Installation Guide](#).
- About...: Show software version and copyright information

## 3.3 Tool Bar

It provides quick access to some commonly used functions, and from left to right are:

-  (Ctrl+N): Create a new file or project
-  (Ctrl+O) : Open a file or project

-  (Ctrl+S) : Save a file or project
-  (Ctrl+Shift+S): Save all files or projects
-  (Ctrl+P): Print
-  (Ctrl+Z): Undo your last operation
-  (Ctrl+Y): Redo your last operation
-  (Ctrl+X): Cut
-  (Ctrl+C): Copy
-  (Ctrl+V): Paste
-  (Ctrl+F) : Find
- : Start Gowin Analyzer Oscilloscope; for the details, you can see [SUG114, Gowin Analyzer Oscilloscope User Guide](#).
- : Start IP core Generator
- : Start Programmer; for the details, you can see [SUG502, Gowin Programmer User Guide](#).
- : Open DSIm
- : Start Eye Diagram analysis tool
- : Start FloorPlanner; for the details, you can see [SUG935, Gowin Design Physical Constraints Guide](#).
- : Start Timing Constraints Editor; for the details, you can see [SUG940, Gowin Design Timing Constraints Guide](#).
- : Run Synthesis
- : Run Place & Route
- : Run Synthesis and Place & Route

### 3.4 Project Area (Design)

The project area shows projects and the related files. You can check or edit the project device information, user design files, user constraints files, and configuration files, etc.

### 3.5 Process Area (Process)


The process area provides FPGA design flow, including synthesis, place & route, and Programmer. You can also double-click timing constraints editor and physical constraints editor to edit the constraints files.

## 3.6 Hierarchy Area (Hierarchy)

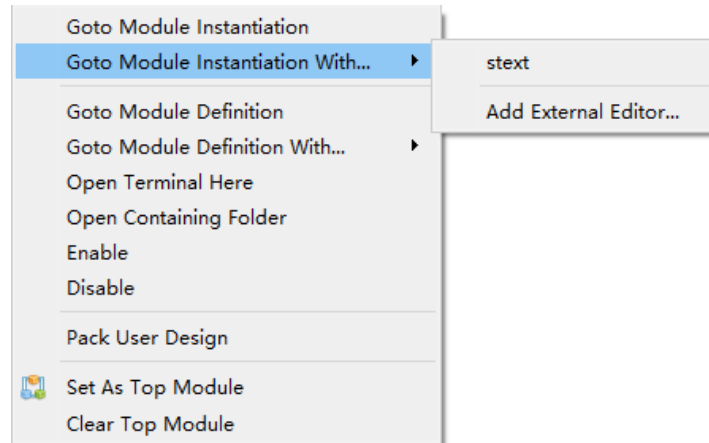
After loading the design files, software will parse the design files first. The hierarchy view shows the hierarchy of current project. In Hierarchy view, you can locate the definition and instance of a module in a design file. You can also set a module to top module. The Unit column shows module hierarchy of the design files, and the Files column shows the file where the module definition is. Additionally, the Hierarchy window allows you to search project design files by module name or file name. Currently, the Hierarchy supports parsing Verilog, VHDL, and System Verilog languages.

### 3.6.1 Right-click Menu

Functions supported in the right-click menu in the Hierarchy view are as follows:

- **Goto Module Instantiation:** Go to the module instance in the source file and open it with the editor built in Gowin Software. If you configure a third-party editor in "Tools > Options > External Editor" and "Always Use External Editor" is checked, you can open the source with a third-party editor by default via Goto Module Instantiation.
- **Goto Module Instantiation With...:** Go to the module instance in the source file. As shown in Figure 3-2, you can choose the "notepad" or "Add External Editor". If you select "Add External Editor", "External Editor" dialog box pops up for setting.
- **Goto Module Definition:** Go to the module in the source file and open it with the editor built in Gowin Software. If you configure a third-party editor in "Tools > Options > External Editor" and "Always Use External Editor" is checked, you can open the source with a third-party editor by default via Goto Module Instantiation.
- **Goto Module Definition With...:** Go to the module in the source file. As shown in Figure 3-2, you can choose the set editor or "Add External Editor". If you select "Add External Editor", "External Editor" dialog box pops up.
- **Open Terminal Here:** Open the folder containing the file.
- **Open Containing Folder:** Open a command-line window.
- **Enable:** Enable the project file.
- **Disable:** Disable the project file.
- **Pack User Design:** Pack the module and its sub-module.
- **Set As Top Module:** Set the module as top module; the module set as the top will be marked "" to indicate that the current module is the top module, and the original hierarchy remains.
- **Clear Top Module:** Clear the top module setting.

**Figure 3-2 Right-click Menu of Hierarchy**



If there is an error during hierarchy parse of the project files, the prompt "RTL Analysis Error" marked in red will pop up at the top right of the hierarchy view.

### 3.6.2 Resources Display

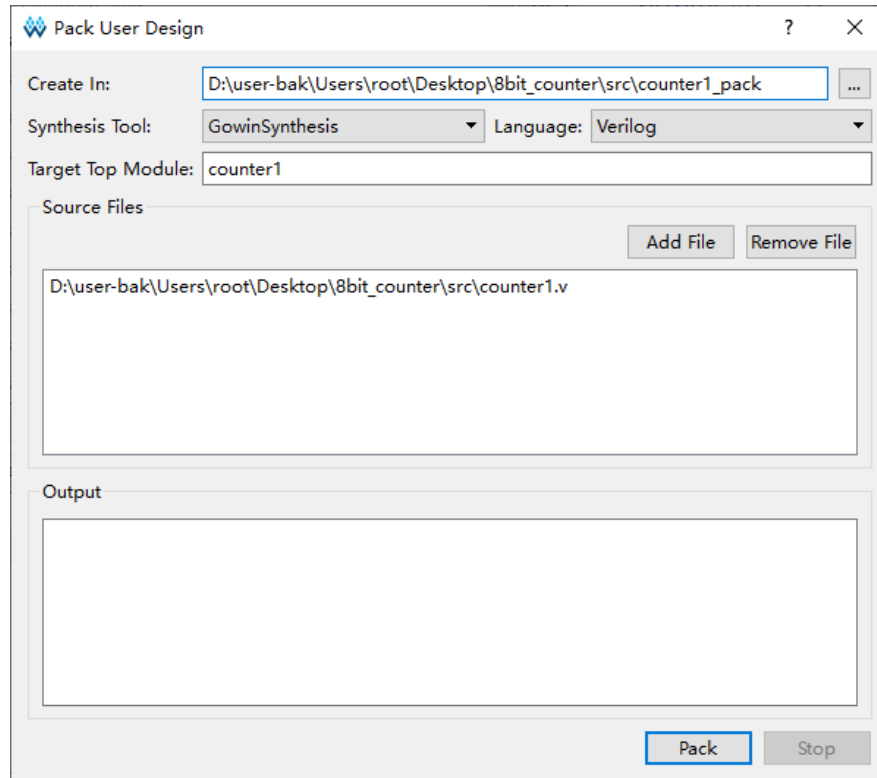
The Hierarchy view will automatically display the resources of the current project after synthesis, as shown in Figure 3-3. If a module is defined as a pack module in the design, its resource is not displayed, and its resource will be counted in its upper module. The resources used by each module will be displayed with two data. As shown in Figure 3-3, the LUT resource for module alltop is 2827 (6), where 6 represents the number of LUTs used by the module itself, and 2827 represents the total number of LUTs used by the module and its submodules.

**Figure 3-3 Resources Display in Hierarchy View**

Unit	File	Register	LUT	ALU	BSRAM	SSRAM
alltop	src/alltop.v	1804(0)	2827(6)	474(0)	9(0)	0(0)
rxuart(rcvuart)	src/rxuart.v	80(80)	93(93)	27(27)	0(0)	0(0)
txuart(tcuart)	src/txuart.v	43(43)	84(84)	0(0)	0(0)	0(0)
altbusmaster(slavedbus)	src/altbusmaster.v	1681(76)	2644(161)	447(0)	9(0)	0(0)
deppbyte(deppdrive)	src/deppbyte.v	51(51)	10(10)	0(0)	0(0)	0(0)
wbubus(busbdriver)	src/wbubus.v	660(20)	1017(11)	186(18)	6(0)	0(0)
icontrol(pic)	src/icontrol.v	27(27)	34(34)	0(0)	0(0)	0(0)
ziptimer(zipt_a)	src/ziptimer.v	65(65)	116(116)	0(0)	0(0)	0(0)
ziptimer(zipt_b)	src/ziptimer.v	33(33)	84(84)	0(0)	0(0)	0(0)
rtlight(thetime)	src/rtlight.v	153(153)	145(145)	90(90)	0(0)	0(0)
wbpwmaudio(theaudio)	src/wbpwmaudio.v	66(66)	11(11)	44(44)	0(0)	0(0)
spio(thesprio)	src/spio.v	22(22)	11(11)	0(0)	0(0)	0(0)
wbgpio(thegpio)	src/wbgpio.v	49(49)	17(17)	16(16)	0(0)	0(0)
wbqspiflashp(flashmem)	src/wbqspiflashp.v	272(156)	760(572)	30(24)	0(0)	0(0)
llqspi(lldriver)	src/llqspi.v	116(116)	188(188)	6(6)	0(0)	0(0)
wbicape6(fpga_cfg)	src/wbicape6.v	107(68)	195(150)	15(15)	1(0)	0(0)
wbicapesimple(spartancfg)	src/wbicapesimple_G.v	39(39)	45(45)	0(0)	1(1)	0(0)
wbscope(wbcfgscope)	src/wbscope.v	100(100)	83(83)	66(66)	2(2)	0(0)

### 3.6.3 Pack File

When you open a project, if you need to pack all/some source files, you can right-click the module to be packed in the Hierarchy view, and choose "Pack User Design" to generate a post-synthesis pack file. "Pack User Design" dialog box is as shown in Figure 3-4.

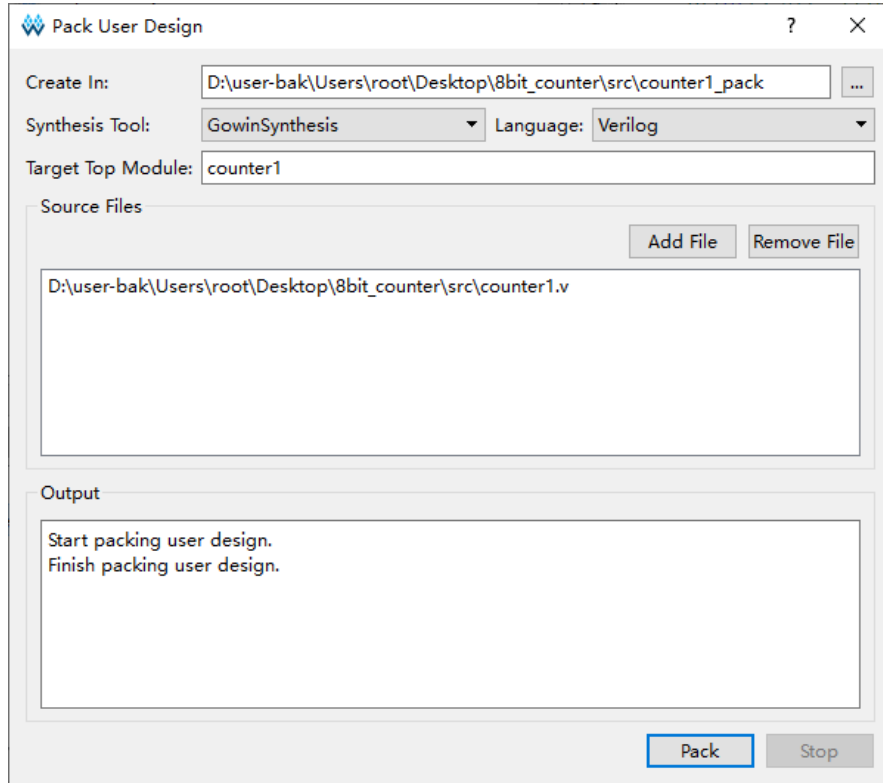
**Figure 3-4 Pack User Design Dialog Box**

The Pack User Design configurations are as follows:

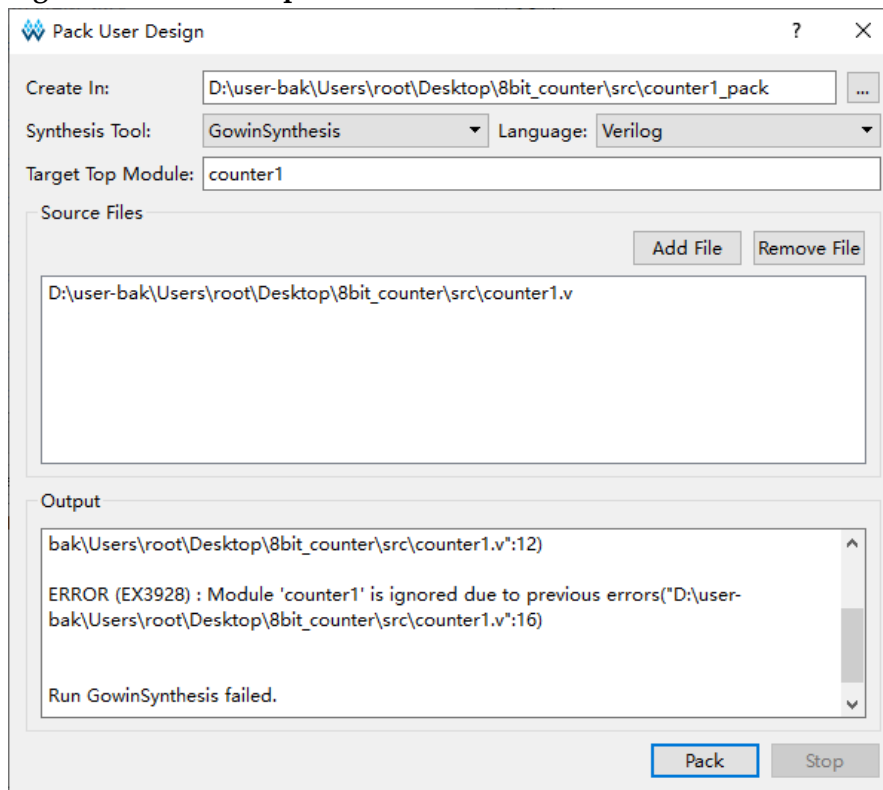
- Create In: The path of the generated pack files, it supports absolute path only, and the default path is \src\- Synthesis Tool: Select the synthesis tool; only GowinSynthesis is supported.
- Language: Select Verilog or VHDL, and the default is Verilog.
- Target Top Module: Top module to be packed. The default is the module selected in the Hierarchy view. You can change it.
- Source Files: List the source files of module and sub module selected in the Hierarchy view.
- Add File: Used to add a file to be packed
- Remove File: Used to remove a file that do not need to be packed
- Output window: Output information
- Pack: Run Pack
- Stop: Stop Pack

Information will be printed in the Output view, as shown in Figure 3-5. When pack starts, if there is an error, the error will be reported in the Output view, and the information of pack failure will be printed, as shown in Figure 3-6.

**Figure 3-5 Output Information in Pack User Design View**



**Figure 3-6 Error Prompt**



After pack, two files are generated under the target path. If Verilog selected, the two files are <topmodule\_name>\_gowin.vp and <topmodule\_name>\_sim.v. If VHDL selected, the two files are

<topmodule\_name>\_gowin.vhdp and <topmodule\_name>\_sim.v.  
 <topmodule\_name>\_gowin.vp and <topmodule\_name>\_gowin.vhdp are pack file and can be used by others. <topmodule\_name>\_sim.v is a flattened plain netlist that can be used for internal simulation.  
 <topmodule\_name>\_sim.v is a flattened plain netlist that can be used for internal simulation.

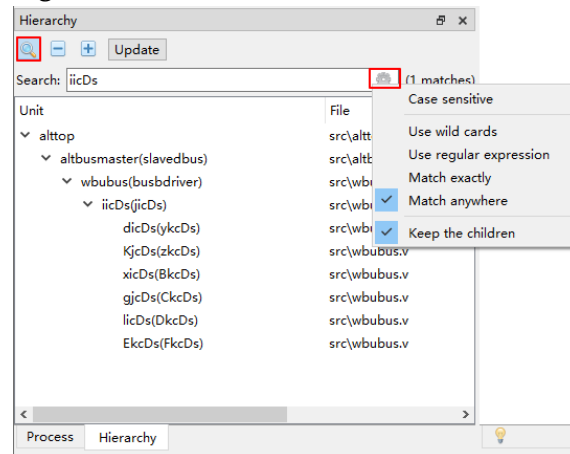
### Note!

In the project, if there are multiple modules that instantiate the same sub module, the files generated after packing these modules separately will have the definition of the sub module. If the generated files are used in the same project, it reports an error that the sub module is repeatedly defined, which needs to be avoided.

## 3.6.4 Search Function

When a project is open and contains many design files, you can click the search icon in the Hierarchy window to search by module name or file name. Various options are available during the search, such as "Use wild cards" or "Match exactly". The dialog box is as shown in Figure 3-7.

Figure 3-7 Search Function



## 3.7 Source File Editing Area

You can view, edit and highlight source files in the source file edit area.

The source file editing area shows different files, including new files or opened files, the generated files after synthesis or Place & Route, and it also shows "Start Page" and "Design Summary".

If the file is displayed in the editing area and a modification is performed on the file externally, "File Changed" will pop up in the file editing area. Select "Reload" to reload the file.

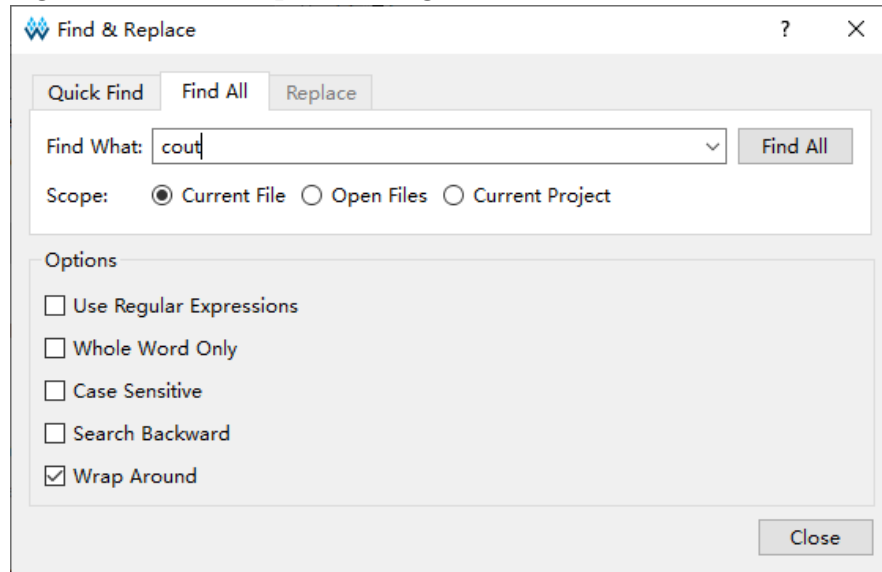
Click "File > Close", or click the icon "✕" in the file editing area to close current files.

Click "File > Close All" to close all the files in the file editing area.

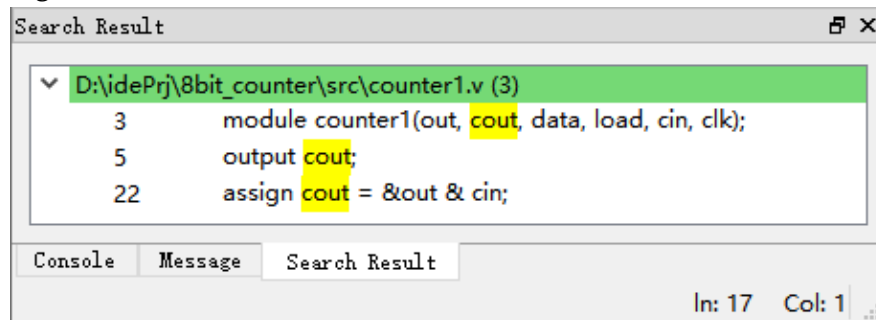
Open a file, and you can open "Find & Replace" dialog box by shortcut Ctrl+F or clicking "Find & Replace" in the toolbar. There are three options in "Find All": Current File, Open Files, and Current Project, as shown in Figure 3-8. After clicking "Find All", "Search Result" view will pop up and the

search content will be highlighted, and the total number of matches is displayed at the end of the first line, as shown in Figure 3-9.

**Figure 3-8 Find & Replace Dialog Box**



**Figure 3-9 Search Result View**

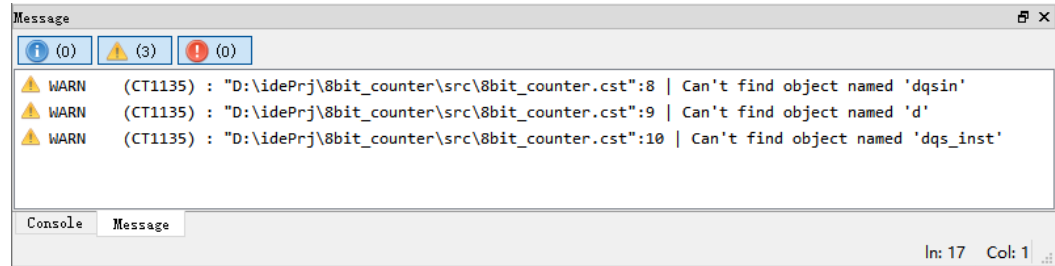


## 3.8 Information Output Area

The information output area displays the processing information when the software is running. You can view different outputs by manually switching between the tabs:

- Console page includes Tcl commands, warnings, errors, etc.
- Message page includes note, warning, error.

In Console page, right-click and select "Clear" to clear all the information in the tab. You can configure the message page to display note only, warning only or error only. The number of notes, warnings and errors will be recorded and shown on each of the corresponding tabs, as shown in Figure 3-10. Right-click and select "Clear" on "Message" page to clear the page information.

**Figure 3-10 Information Output Area**

After selecting an Error or Warning message reported by PnR, right-click and select "Help" or press the shortcut key "F1", the "GOWIN Help" of this error or warning will pop up, and the help information of this error or message will be described in details in the document. Some common warnings or errors are shown in Table 3-1, and help documents can be viewed by clicking "Help > View Help", which supports Chinese and English versions.

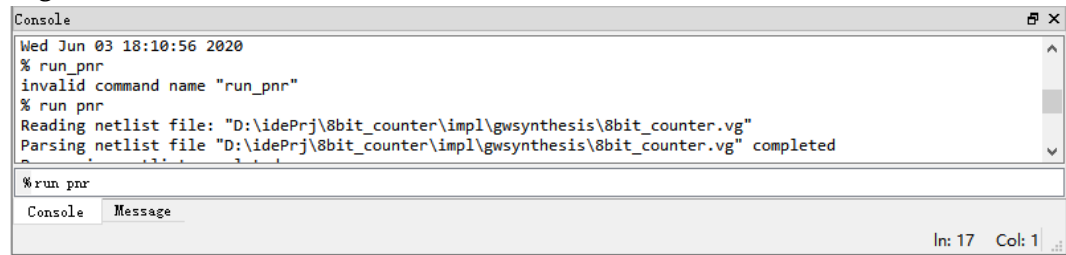
**Table 3-1 Common Warnings and Errors**

Name	Code	Description
Warning	WARN (PA1002): <file>:<line>   Invalid parameterized value <value>(<parameter>) specified for instance <instanceName>	The specified instance sets invalid parameters.
	WARN (PA1008): <file>:<line>   Object <name> is already defined	The net or port has already been defined.
	WARN (PA1001) : Dangling net <netName>(source:<instanceName>) in module <moduleName> has no destination	The net in the specified module has no destination.
	WARN (CT1098) : <file>:<line>   Group name <name> is already defined	The constraints group name has already been defined.
	WARN (CT1101) : <file>:<line>   Location column <number> is out of chip range(<maxColumn>)	The location column is out of chip range.
Error	ERROR (PA2000): <file>:<line>   Syntax error near token <name>	There is an error near token.
	ERROR (PA2001): <file>:<line>   Module <moduleName> is already defined	The module name has already been defined.
	ERROR (PA2017): The number(<value>) of <instType> in the design exceeds the resource limit(<maxValue>) of current device	The number of the devices in the design file exceeds the resource limit.
	ERROR (PA2025): No <instType> resource in current device	There are resources that are not supported by the chip in the design.
	ERROR (PA2054): <file>:<line>   <name> is already declared	The name has already been declared.

The Tcl editing window locates at the bottom of the Console page. You

can enter Tcl commands in the window and press the Enter key to execute, as shown in Figure 3-11. For the details of Tcl, please refer to [SUG1220, Gowin Software Tcl Commands User Guide](#).

**Figure 3-11 Tcl Commit Window**



```
Console
Wed Jun 03 18:10:56 2020
% run_pnr
invalid command name "run_pnr"
% run_pnr
Reading netlist file: "D:\idePrj\8bit_counter\impl\gwsynthesis\8bit_counter.vg"
Parsing netlist file "D:\idePrj\8bit_counter\impl\gwsynthesis\8bit_counter.vg" completed

%run_pnr
Console Message
In: 17 Col: 1
```

# 4 Gowin Software Usage

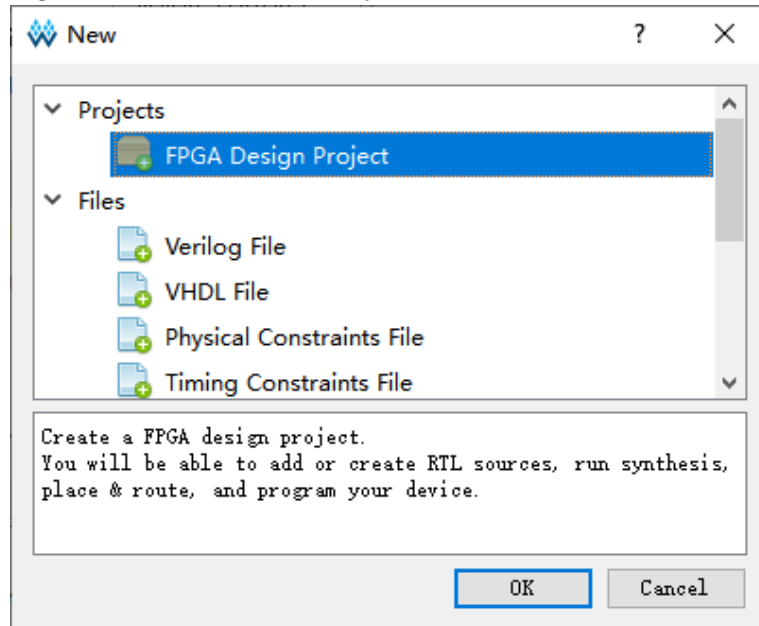
Gowin Software supports interface mode and command line mode. For command line mode, please refer to [SUG1220, Gowin Software Tcl Commands User Guide](#).

Take Gowin Software in Windows10 as an example to introduce how to use the software.

## 4.1 Create a New Project

1. From the File menu, choose "File> New..." to open the "New" dialog, as shown in Figure 4-1.

Figure 4-1 Create a New Project

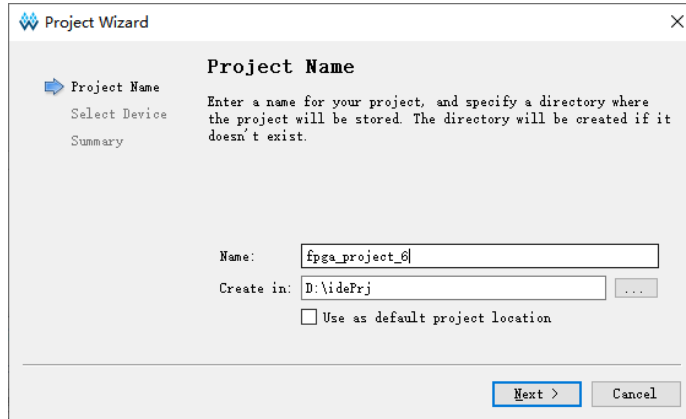


### Note!

There are three ways to open a "New" dialog:

- Use the "Ctrl+N" shortcut.
- Click the "New File or Project" icon in the toolbar.
- Click "Quick Start > New Project" on the Start Page.

2. Select "FPGA Design Project", and then click "OK" to open "Project Wizard", as shown in Figure 4-2.

**Figure 4-2 Project Wizard**

3. Create the project "Name" and "Create in", as shown in Figure 4-2.

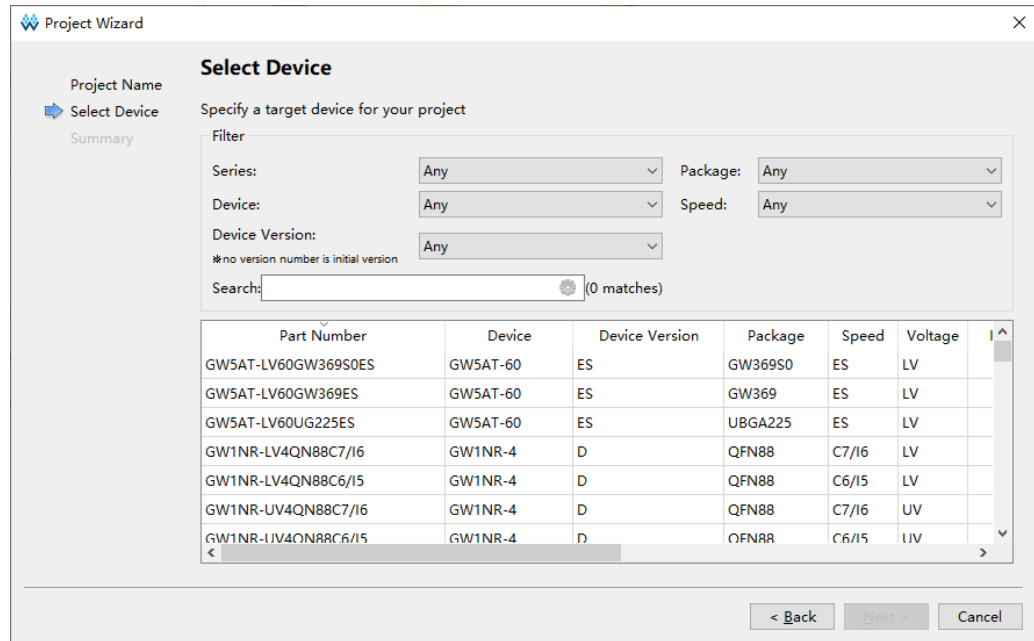
- a) Type the project name in the "Name" text box.
- b) Click the "..." icon to choose the project path.

If you select "Use as default project location", the project location will be set as the default, and all later projects you create will be saved to this location.

**Note!**

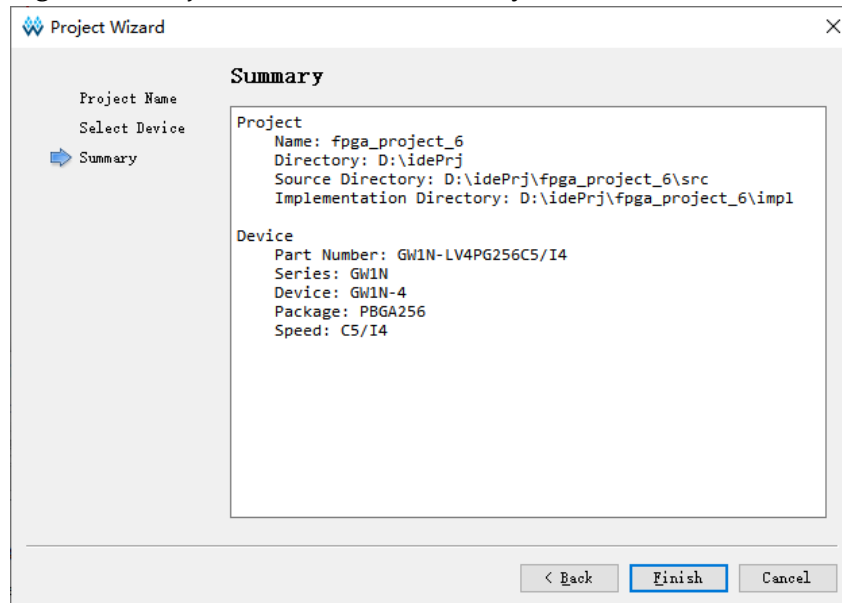
- The file path length is limited in Windows and Linux, with a limit of 260 characters in Windows and 4096 characters in Linux. If beyond the limit, you cannot delete or copy the file path.
  - The path separator is "\" in Windows; for example, E:\Gowin\ide.
4. Click "Next" to set the device, including Series, Device, Package, Speed, and Device Version. You can also search for devices using the "Search" button.
- You can select series in Series.
  - You can select device in Device.
  - You can select package in Package.
  - You can select speed in Speed.
  - You can select device version in Device Version.
  - You can select part number in Part Number, and it displays the detailed information; for devices without version, the version information column is blank, and the version of the same device is displayed in reverse order, as shown in Figure 4-3.

Figure 4-3 Select Device



- Click "Next" to open the project information Summary window, as shown in Figure 4-4 .

Figure 4-4 Project Information Summary




- Click "Finish", and the project now is created.

## 4.2 Open an Existing Project

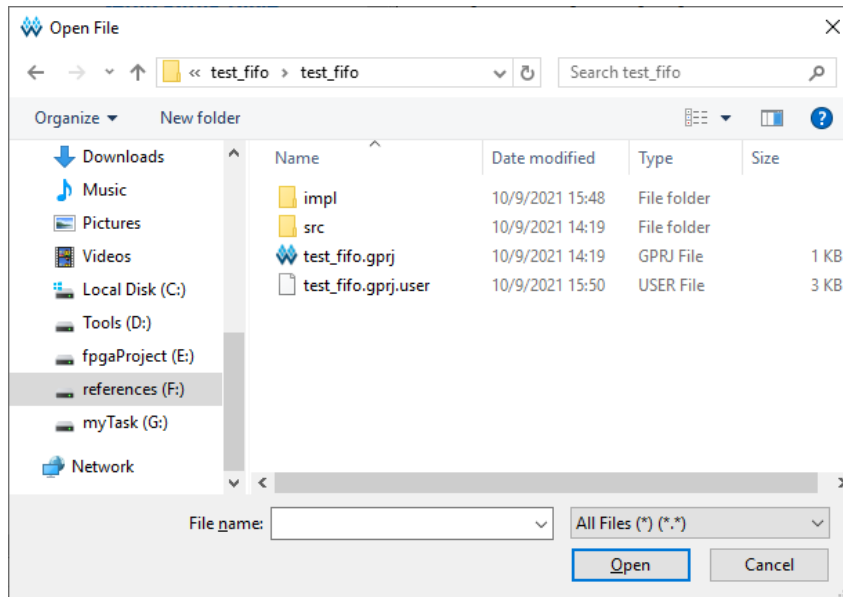
Use one of the following five methods to open an existing project.

### Open from Tool Bar

- You can click the " " icon in the tool bar to open the "Open File" dialog box, as shown in Figure 4-5.

2. Choose the project file (\*.gprj) and click "Open" to open it.

**Figure 4-5 Open an Existing Project**



### Open from Menu Bar

1. In the menu bar, select "File > Open ..." to open the "Open File" dialog box, as shown in Figure 4-5.
2. Choose the project file (\*.gprj) and click "Open" to open it.

### Open from Start Page

1. On the start page, click "Open Project..." to open "Open Project" dialog box.
2. Choose the project file (\*.gprj) and click "Open" to open it.

### Open from Recent Projects

In the menu bar, click "File > Recent Projects" to open your required project.

#### Note!

- You can also open the project in the "Start Page > Recent Projects" list.
- The "Recent Projects" list shows the recently opened projects.
- If the project has been deleted, the "Open Project" dialog box will pop up.

### Open from Project File

Find the \*.gprj file, and double-click on \*.gprj file to open the project automatically.

## 4.3 Edit a Project

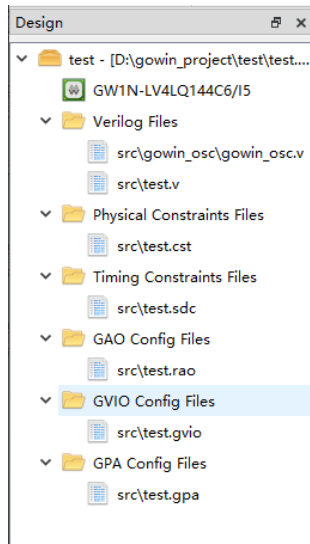
After creating or opening a project, you can edit the device information and the related files in the project design area, as shown in Figure 4-6.

The Project Design Area contains the following:

- The project path

- Part number
- The current project files, including user design files (Source Files), physical constraints files (.cst), timing constraints files (.sdc), GAO config files (.gao, .rao), GPA config files (.gpa), and virtual input and output configuration files (.gvio), etc.

**Figure 4-6 Project Design Area**



### 4.3.1 Edit a Project Device

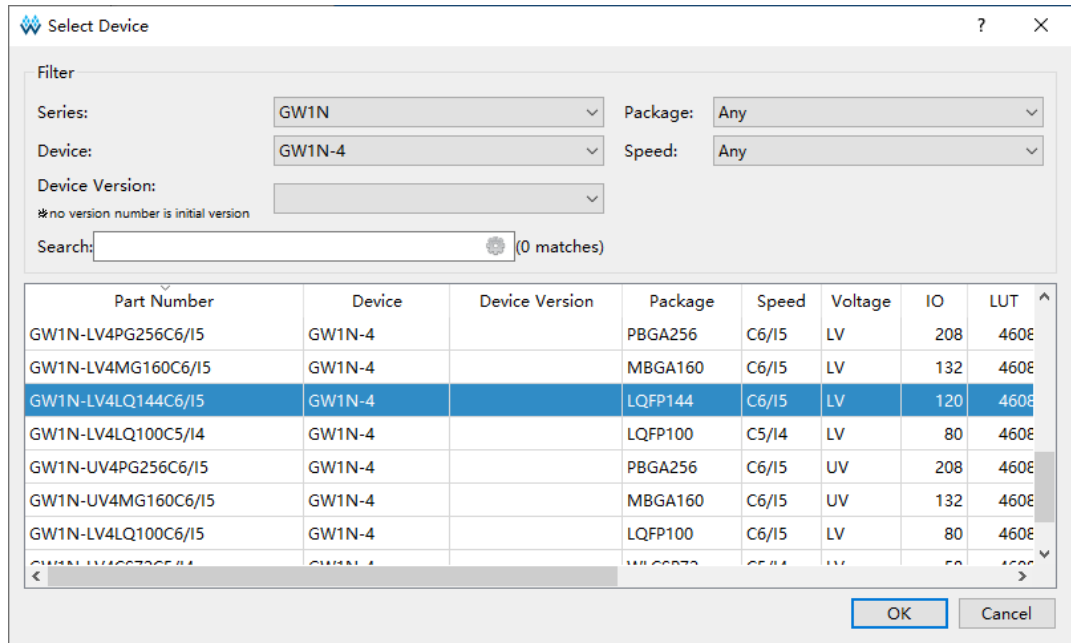
The chip information used in the current FPGA project can be edited in the project design view.

1. As shown in Figure 4-6, double-click "GW1N-LV4LQ144C6/I5" to open the "Select Device" dialog box, or choose "Set Device" from Project pull-down list, as shown in Figure 4-7.
2. In the "Select Device" dialog box, select part number from the "Part Number", then you can edit the device. The "Part Number" column displays detailed information about the selected chip, including device, device version, package, speed, voltage, and the resources such as IO/LUT/FF/ROM16/SSRAM/BSRAM/User Flash/DSP/PLL in the chip.

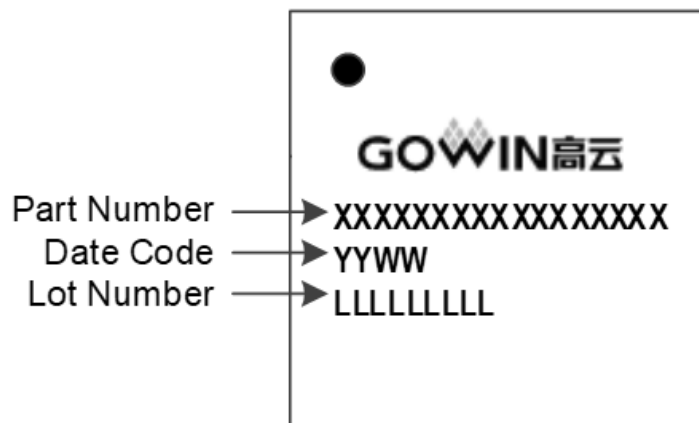
**Note!**

If the Device Version is empty, it means it is the initial version; the device version information will be marked after the date code on the chip, and date code is printed on the chip surface, as shown in Figure 4-8; the device selected in the "Part Number" column needs to be consistent with the device version used.

**Figure 4-7 Project Device Info.**




**Figure 4-8 Data Code Display**



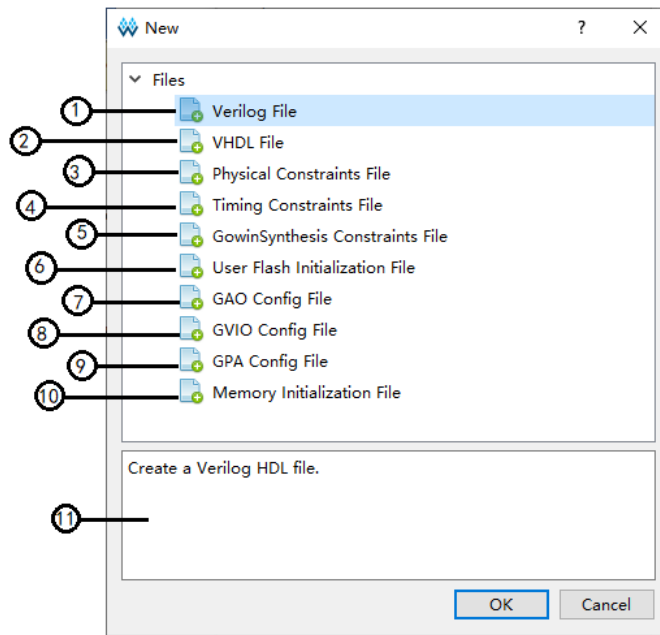
### 4.3.2 Edit a Project File

Files that need to be added in projects include RTL design files (Source Files), constraints files, and configuration files. Refer to the following descriptions to edit the project files.

#### Create Design and Constraints Files

1. Click " " in the tool bar, or select "File > New File..." in the menu bar to open the "New..." dialog box.
2. As shown in Figure 4-9, select a file.

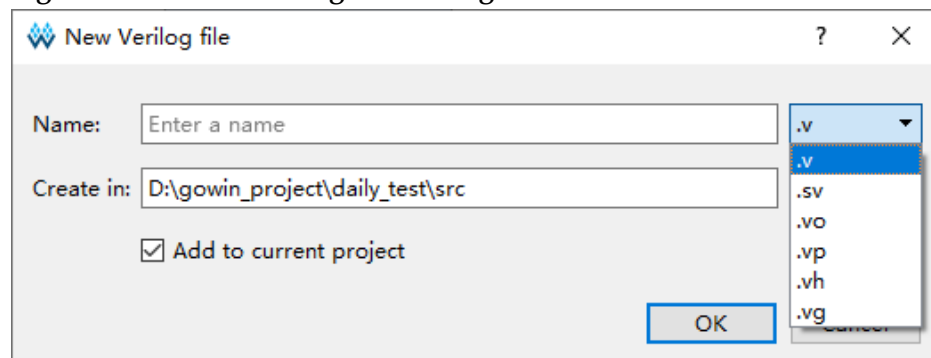
**Figure 4-9 Create a New File Dialog Box**



- |                                   |                                    |
|-----------------------------------|------------------------------------|
| ① User Verilog File               | ② User VHDL File                   |
| ③ Physical Constraints File       | ④ Timing Constraints File          |
| ⑤ GowinSynthesis Constraints File | ⑥ User Flash Initialization file   |
| ⑦ GAO Config File                 | ⑧ Virtual Input/Output Config File |
| ⑨ Power Analysis Config File      | ⑩ Memory Initialization File       |
| ⑪ File Description                |                                    |

3. Take creating a Verilog File for an instance. Select "Verilog File" to open the Verilog File dialog box, as shown in Figure 4-10. Check "Add to current project" by default, i.e. the new design file will be added to the current project by default.

**Figure 4-10 Create Verilog File Dialog Box**



4. Type the file name and click "OK".

## Create a Configuration File


1. Click " " in the tool bar, or select "File > New File..." in the menu bar to open the "New..." dialog box, as shown in Figure 4-9.
2. As shown in Figure 4-9, select a file. Take creating a GPA Config File for an instance. Select "GPA Config File" and to open New GPA Config File dialog box; type the file name, click "OK", and the new GPA profile will be automatically added to the project design area, as shown in Figure 4-11.
3. Double click on this configuration file in the project design area to open a window for editing, as shown in Figure 4-12.

Figure 4-11 New GPA Config File Dialog Box

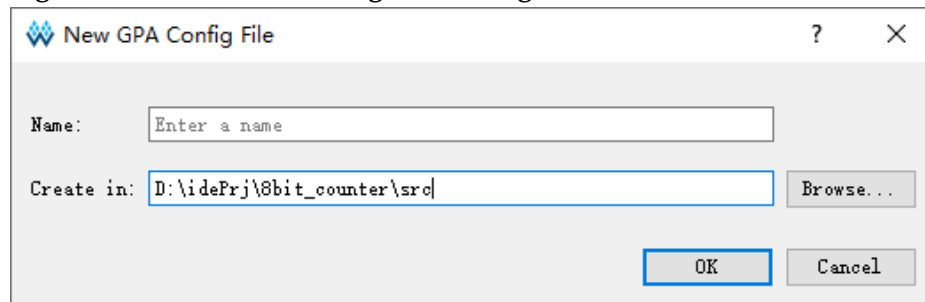
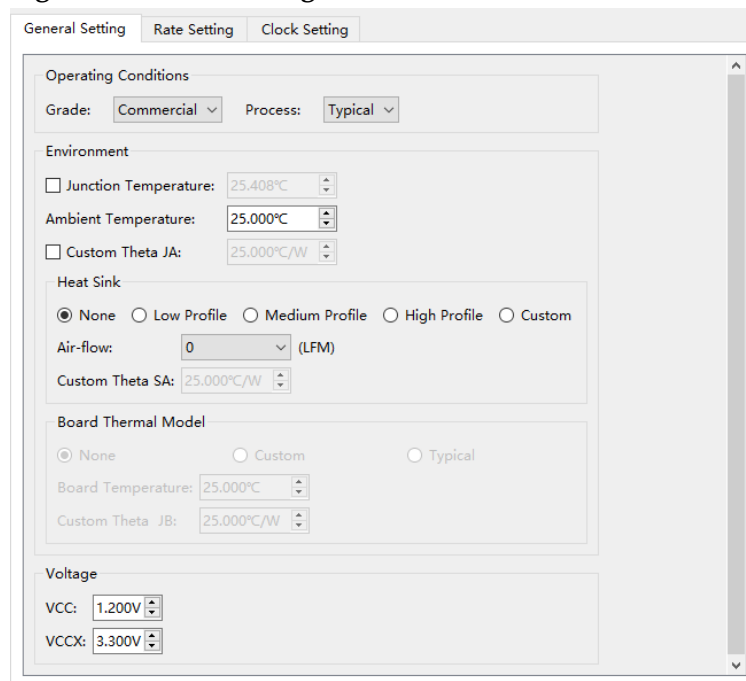


Figure 4-12 GPA Config File Window

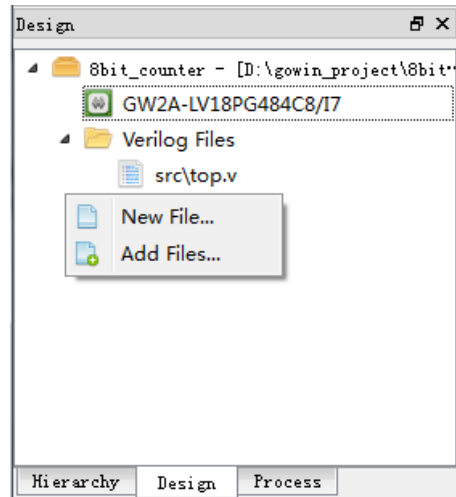


## Add Project Files

1. As shown in Figure 4-13, right-click in the blank of the project design area, select "Add Files..." to open the "Select Files" dialog box.

2. Select single or multiple project files to add. Gowin Software will automatically classify the files in the project design area. If the added files are not RTL design files, netlist files, constraints files, GPA configuration files, GAO configuration files or GVIO configuration files, "Other Files" will be added in the project design area.

**Figure 4-13 Right-click in Design View**

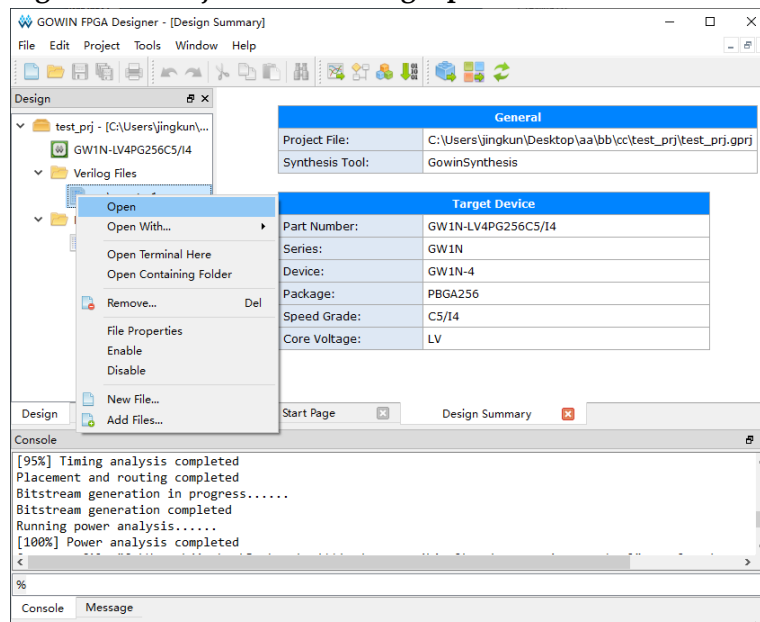


## Modify Project Files

Use the following two methods to open the project files, as shown in Figure 4-14.

1. Double-click any file in the project design area; the file will open in the source file editing area.
2. Right-click on the file that is to be modified and click "Open".

**Figure 4-14 Project Files Editing Options**



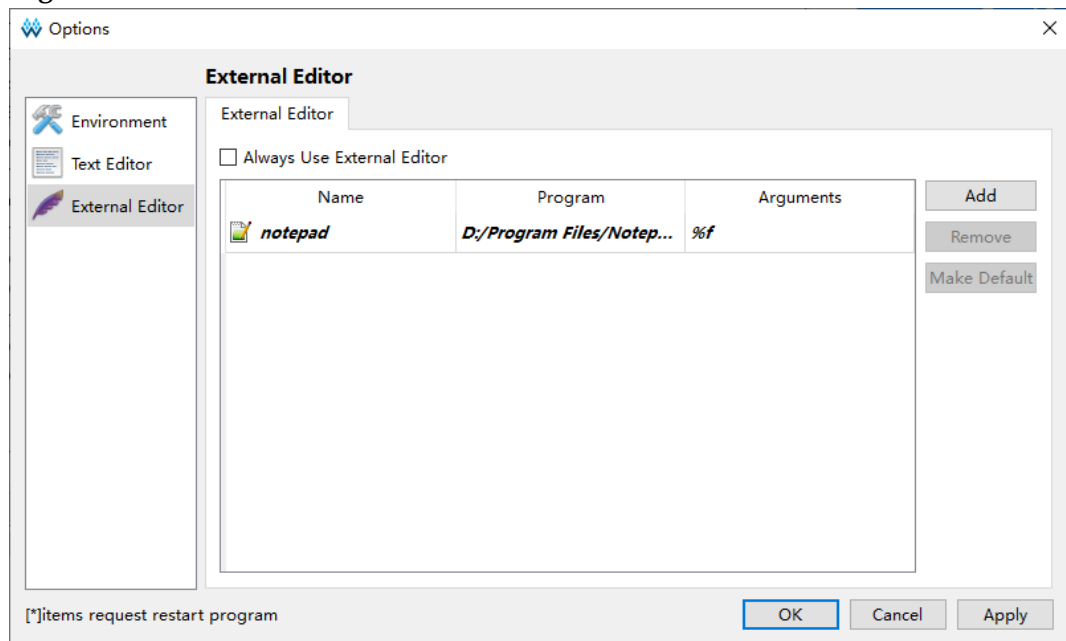
If you have configured a third-party text editor by clicking "Tools >

Options", select "Open With..." to open the design file with the third-party text editor. If you select "Add External Editor", you can add other external editor, as shown in Figure 4-15. If you check "Always Use External Editor", the external editor will always be used to open files. If you select "Open Containing Folder", you can open the folder. If you select "Open Terminal Here", you can use command line mode.

If you modify and save a file by an external editor, Gowin Software will generate a reload prompt.

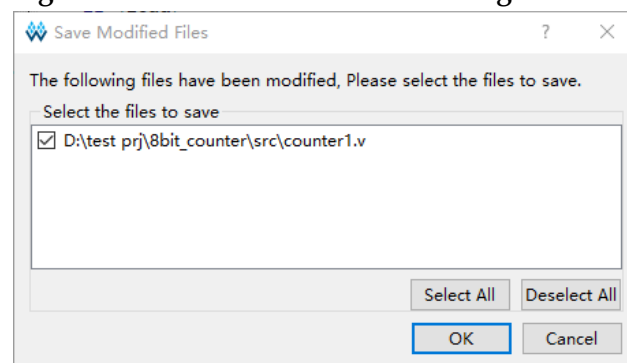
If you close the unsaved file after editing, Gowin Software will pop up a warning.

**Figure 4-15 External Editor**



After project files are modified, if you run Synthesize or Place & Route before saving these files, the "Save Modified Files" dialog box will pop up, as shown in Figure 4-16.

**Figure 4-16 Save Modified Files Dialog Box**



Click "OK"; the files will be saved and then perform previous operations automatically. Click "Cancel"; the files will not be saved and Synthesize or Place & Route will not be performed.

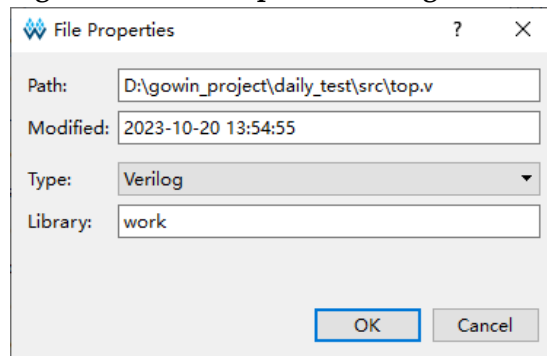
## Delete Project Files

1. Select the file in the project design area.
2. Right-click and select "Remove...", or directly press the Delete key to open the "Remove Files" dialog box. If you select the "Remove Permanently on Disk", the file is deleted from the current project and on disk. Otherwise, the file is deleted only from the current project.

## Edit Project File Attributes

Right-click any file in the project design area, select File Properties from the right-click list, and "File Properties" dialog box pops up, as shown in Figure 4-17. The Path, Modified time, Type, and Library information are displayed in the dialog box. The file type can be modified in the Type drop-down list. After clicking "OK", the file will automatically move to the selected type in the Design view. Library is used to specify the library used by VHDL files synthesis, and the default is work. If there are multiple libraries, you need to separate them with semicolon.

**Figure 4-17 File Properties Dialog Box**



If more than one Verilog file or VHDL file is selected, the "File Properties" dialog box does not display the path and modified time. If both Verilog and VHDL files are selected, the "File Properties" dialog box does not display the path, modified time, or Type.

The use of Library is as follows.

- If the top-level (or upper-level) entity in the design has the component of bottom entity, it does not need to care which library the bottom entity belongs to and it can use the default value work.
- If the top-level (or upper-level) entity in the design use "uut1:entity library name. bottom name", such as uut1:entity mb.sub1 to call the bottom entity, then the attribute library of the vhdL file where the bottom entity is located should be the library name (e.g. mb).
- If the package has a component of the bottom entity, the top-level (or upper-level) entity does not need to care which library the bottom entity belongs to when the bottom entity is called through the package, and it can use the default value work.
- If the package has a component of the bottom entity, the top-level (or upper-level) entity uses "uut: package library name. package name. bottom entity name, such as uut1: work.pack.sub1 to call bottom entity,

it does not need to care which library the bottom entity belongs to, and it can use the default value work.

### Enable Project Files

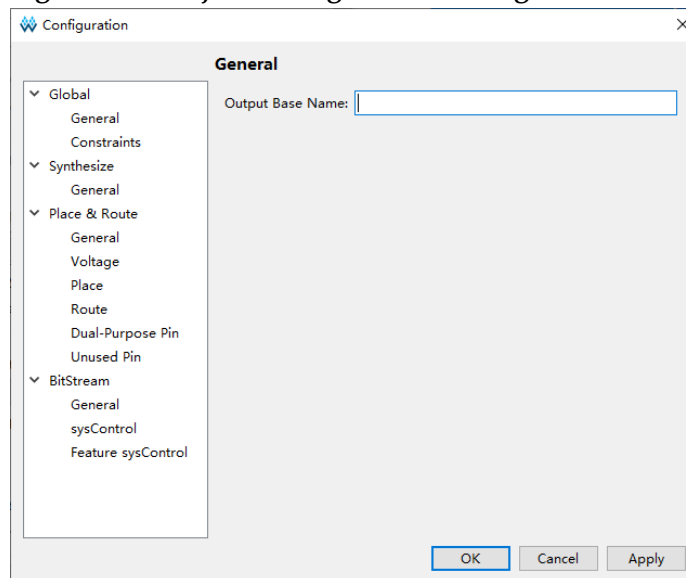
You can see the "Enable" and "Disable" options by right-clicking on any files in the project design area, as shown in Figure 4-14. The files are in the project compilation process when it is enabled, and out of project compilation process when it is disabled.

1. Set Enable/Disable by right-clicking, including single/batch files setting.
2. For constraints files or configuration files of the same type, only one file can be enabled; when you create or add a new file of the same type, the previous one will be disabled.

## 4.3.3 Edit Project Configuration

Right click "Synthesize" or "Place & Route" in the Project Design area to open the project configuration dialog box, as shown in Figure 4-18.

**Figure 4-18 Project Configuration Dialog Box**



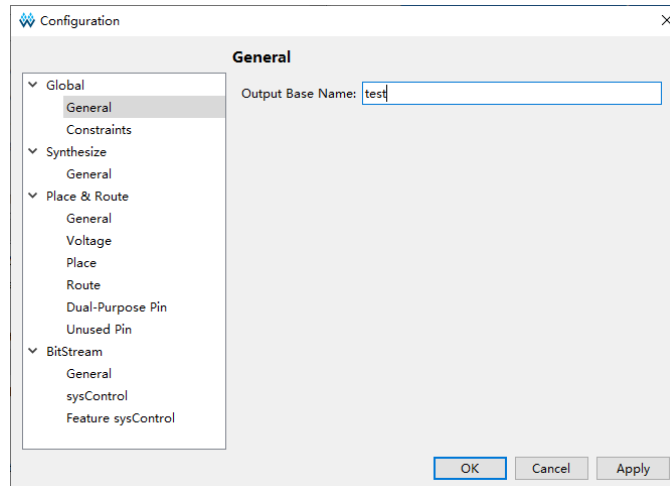
As shown in Figure 4-18, the configurable project options include "Global", "Synthesize", "Place & Route", and "BitStream". The details of the options are as follows.

### Global

Global configuration option includes General and Constraints.

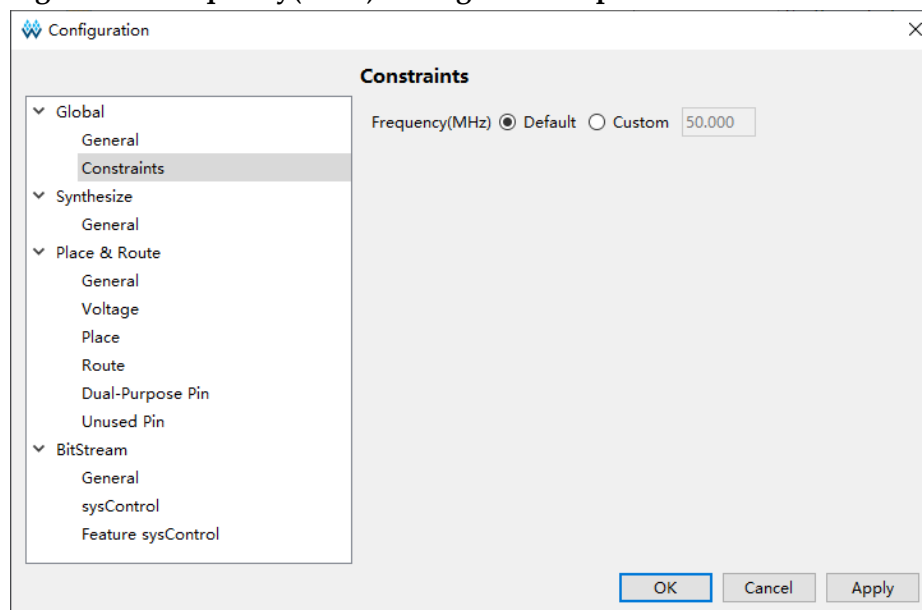
### General

The General configuration is as shown in Figure 4-19; it used to specify the base name of the output file, which defaults to the name of the current project.

**Figure 4-19 General Configuration Option**

## Constraints

The "Constraints" configuration is shown in Figure 4-20. This option allows users to set global frequency; if the frequency is specified in the timing constraint file, you can override the global frequency with timing constraint. The default is set to "Default" (For LittleBee family, the default is 50MHz, and for Arora family, the default is 100MHz).

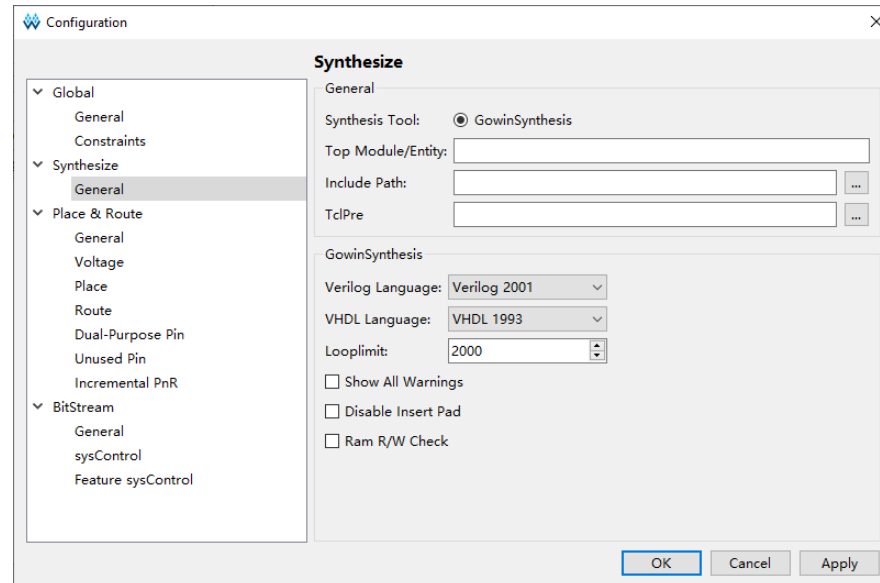
**Figure 4-20 Frequency(MHz) Configuration Option**

## Synthesize

### General

General configuration option is as shown in Figure 4-21.

The synthesis tool is GowinSynthesis; hovering the mouse over some options will display their explanations.

**Figure 4-21 GowinSynthesis Configuration Options**

The detailed descriptions are shown below.

- Top Module/Entity: Specify top module/entity.
- Include Path: Specify include path.
- TclPre: Management file that specifies the software version; when synthesizing, it automatically changes the version number and date, so the running design version can be easily found.
- Verilog Language: System Verilog 2017, Verilog 2001 and Verilog 95, and the default is Verilog 2001. This option is displayed on the interface only when a design file in VHDL format is detected in the current project.
- VHDL Language: VHDL 1993, VHDL 2008, and VHDL 2019; and the default is VHDL1993. The option is displayed in the interface only when VHDL format design files are detected in the current project.
- Looplimit: Set the loop limit value of the default editor in RTL, and the default Value is 2000.
- Show All Warnings: All warnings will be printed during synthesis if this option is checked, which is not checked by default.
- Disable Insert Pad: Whether to insert I/O buffer to the post-synthesis netlist, not checked by default.
- Ram R/W Check: If there is a read or write conflict in RAM, check this option and bypass logic will be inserted around RAM to prevent simulation mismatches. If this option is disabled, bypass logic will not be generated, unchecked by default.

**Note!**

For the details, see [SUG550, GowinSynthesis User Guide](#).

## Place & Route

Place & Route includes General, Voltage, Place, Route, Unused Pin, Dual-purpose Pin, and Incremental PnR. The detailed descriptions are shown in Table 4-1.

**Table 4-1 PnR Configuration Options**

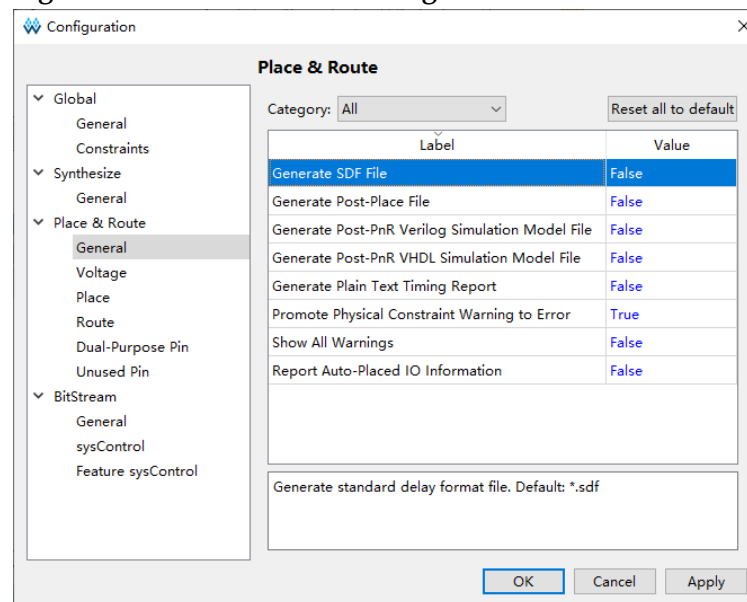
Option	Description
General	Set PnR parameters
Voltage	Set the voltage VCC and VCCX
Place	Set placement parameters
Route	Set route parameters
Unused Pin	Used to set different IO attributes for unused GPIOs
Dual-Purpose Pin	Used to configure the I/O corresponding to the package in the selected device, mainly for configuring dual-purpose pins.
Incremental PnR	Used to enable incremental compilation

Reset all to default: Reset all configurations on the page to the default values.

## General

The General configuration is as shown in Figure 4-22.

**Figure 4-22 Place & Route Configuration**



The descriptions of options in Figure 4-22 are as follows.

- **Generate SDF File:** Generate a standard delay format file with the extension .sdf for netlist timing simulation after PnR, and the default value is False. For the usage, see chapter [7Simulation Files](#).
- **Generate IBIS File:** Generate the file specified by the input/output

buffer information, with the extension .ibs, and the default is False.

The conditions for IBIS generation for each device are shown in the table below.

**Table 4-2 Conditions for IBIS Generation Supported by Each Device**

Device	IO Type	Drive
LittleBee Family	LVC MOS12/LVC MOS12D	2/4/6/8
	LVC MOS15/LVC MOS15D	4/8
	LVC MOS18/LVC MOS18D	4/8/12
	LVC MOS25/LVC MOS25D	4/8/12/16
	LVC MOS33/LVC MOS33D	4/8/12/16/24
Arora Family	LVC MOS12/LVC MOS12D LVC MOS15/LVC MOS15D LVC MOS18/LVC MOS18D LVC MOS25/LVC MOS25D LVC MOS33/LVC MOS33D LVDS25	All
GW5A(S)(T)-138/GW5AT-75 devices (package: UBGA324A)	LPDDR	8/12/16/24
	SSTL135/SSTL135D	8
GW5A(S)(T)-138/GW5AT-75 devices (package: PBGA676A/FCPBGA676A)	LPDDR	8/12/16/24

- **Generate Post-Place File:** Generate a file containing only BSRAM placement information, with the extension .posp, and the default value is False.
- **Generate Post-PNR Verilog Simulation Model File:** Generate a timing simulation model file in Verilog for timing simulation with .vo extension, and the default value is False.
- **Generate Post-PNR VHDL Simulation Model File:** Generate a timing simulation model file in VHDL language with .vho extension, and the default value is False.
- **Generate Plain Text Timing Report:** Generate a timing report in text format, with the extension .tr, and the default value is False.
- **Promote Physical Constraint Warning to Error:** Promote the physical constraint warning to an error, and the default value is True.
- **Show All Warnings:** Output all the Warning information when PNR is running, and the default value is False.
- **Report Auto-Placed IO Information:** Report the location information of auto-placed IO, and the default value is False.
- **Convert SDP32/36 to SDP16/18:** Convert 32/36-bit-wide primitives SDPB/SDPX9B/pROM/pROMX9 into two 16/18-bit-wide SDPB/SDPX9B/pROM/pROMX9 primitives. This option is supported only for Arora V devices. For other devices, this configuration option is

not displayed in the configuration interface. The default value is False.

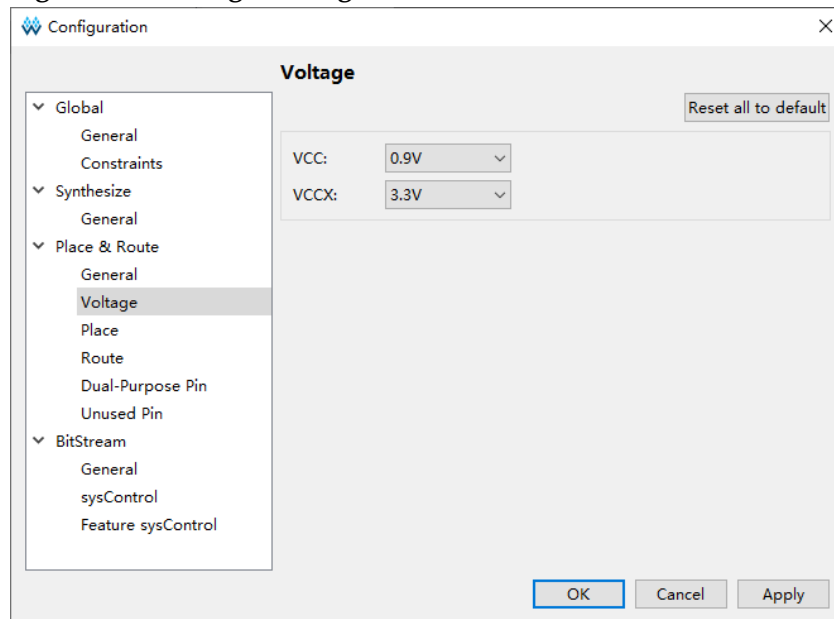
## Voltage

The Voltage configuration is shown in Figure 4-24. Through this option, you can set the VCC and VCCX. Different devices may have different VCC and VCCX settings. Click "Reset all to default", and the configured VCC and VCCX will be restored to the default value.

### Note!

- The VCC configuration affects the delay data of devices.
- The VCCX configuration affects the results of power consumption calculations.

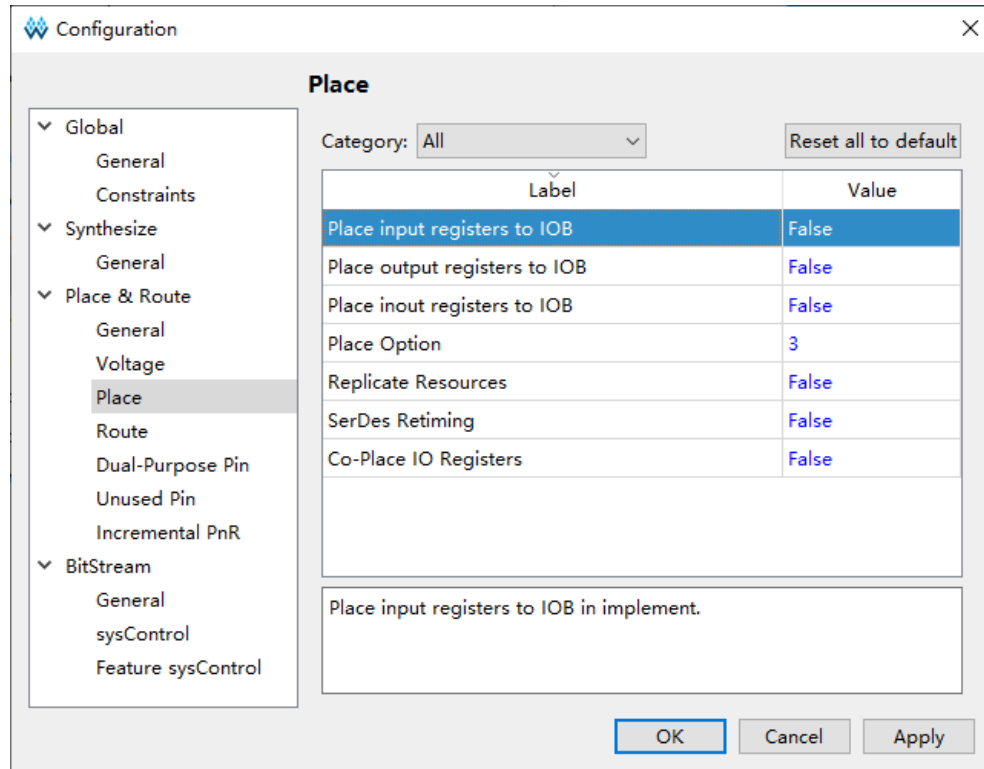
**Figure 4-23 Voltage Configuration**



## Place

The Place configuration is as shown in Figure 4-24.

Figure 4-24 Place Configuration



The descriptions of options in Figure 4-24 are as follows.

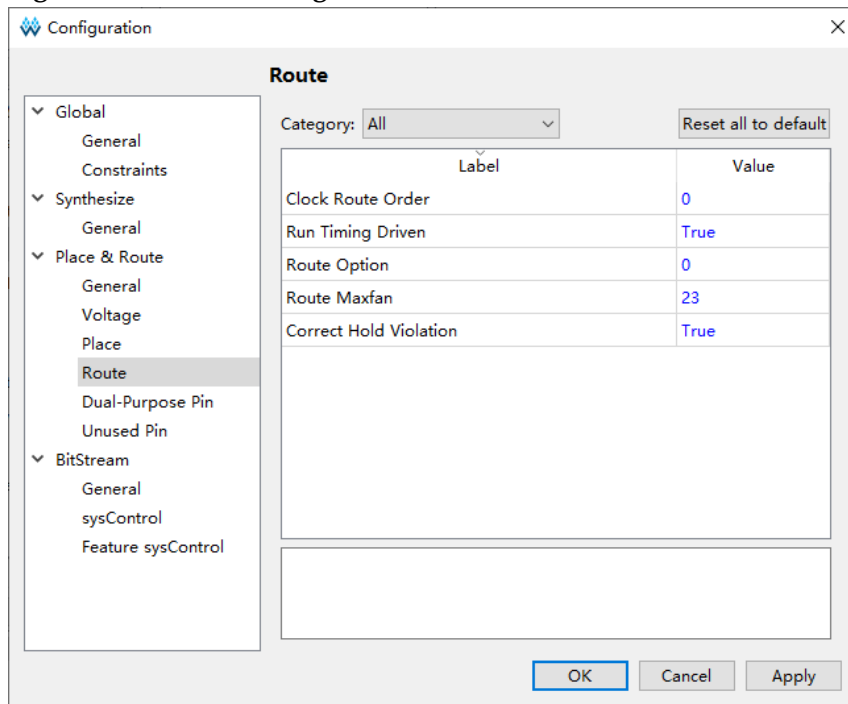
- Place input register to IOB: Place registers driven by input Buffer to IOB; for GW5A(S)(T)-138/GW5AT-75 devices, the default is False; for the other devices, the default value is True.
- Place output register to IOB: Place registers driven by output/tristate Buffer to IOB; for GW5A(S)(T)-138/GW5AT-75 devices, the default is False; for the other devices, the default value is True.
- Place inout register to IOB: Place registers driven by in/out Buffer to IOB; for GW5A(S)(T)-138 devices, the default is False; for the other devices, the default value is True.
- Place Option: Placement algorithm option. For Arora V devices, the available options are 0, 1, 2, 3, and 4. For other devices, the available options are 0, 1, and 2. The default value is 3 for GW3A-20, and 0 for all other devices.
- Replicate Resources: Replicate resources with high fanout to reduce fanout and get better timing results, and the default value is False. Only Arora V and GW3A-20 devices support this option, and it will not be displayed on the configuration interface of other devices.
- SerDes Retiming: Move logic resources closer to the SerDes node to balance timing. This configuration option is supported only by Arora V devices that contain SerDes resources. For other devices, the option is not displayed in the configuration interface, and the default value is False.

- **Co-Place IO Registers:** A placement algorithm for co-placing input and output registers. The default value is False.

## Route

The Route configuration is as shown in Figure 4-25.

**Figure 4-25 Route Configuration**



The descriptions of options in Figure 4-25 are as follows.

- **Clock Route Order:** Specify the route order for clock lines other than those generated by the clock primitive, and the values include 0 and 1, and the default is 0.
  - when it is 0, the order is based on the number of fanouts of net from highest to lowest.
  - when it is 1, the order is based on the frequency from highest to lowest.
- **Run Timing Driven:** Optimize route by Timing Driven, and the default value is True.
- **Route Option:** Route algorithm with the value of 0, 1 and 2. The default value is 2 for GW3A-20, and 0 for all other devices.
  - When it is 0, the default route algorithm is used.
  - When it is 1, the compilation speed is sacrificed to try to find a better route.
  - When it is 2, the route speed will be improved.
- **Route Maxfan:** Based on the route optimization, set the maximum fanout of route. The value should be an integer greater than 0 and less than or equal to 100, and a smaller value may cause route failure. This

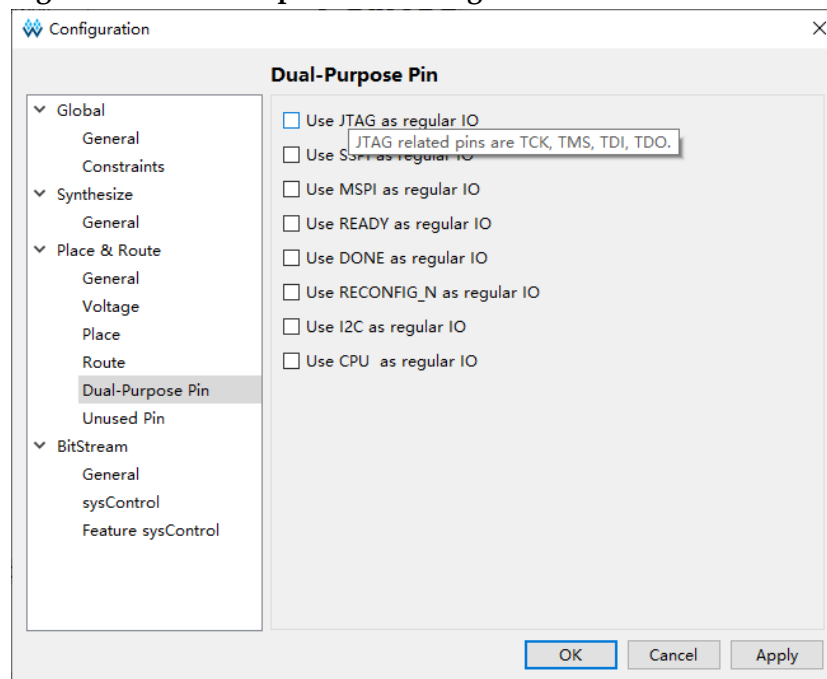
option does not control long wire and clk route. For GW1NZ-1/GW1N-2/GW1NR-2/GW1N-1P5, the default value of Route Maxfan is 10, and 23 for other devices.

- **Correct Hold Violation:** Automatic repair of timing Hold problems via routing, and the default is True.

### Dual-Purpose Pin

The Dual-purpose Pin is a configuration that conforms to Gowin device customization, and hovering the mouse over the option will display its explanation. The configuration is as shown in Figure 4-26.

**Figure 4-26 Dual-Purpose Pin Configuration**



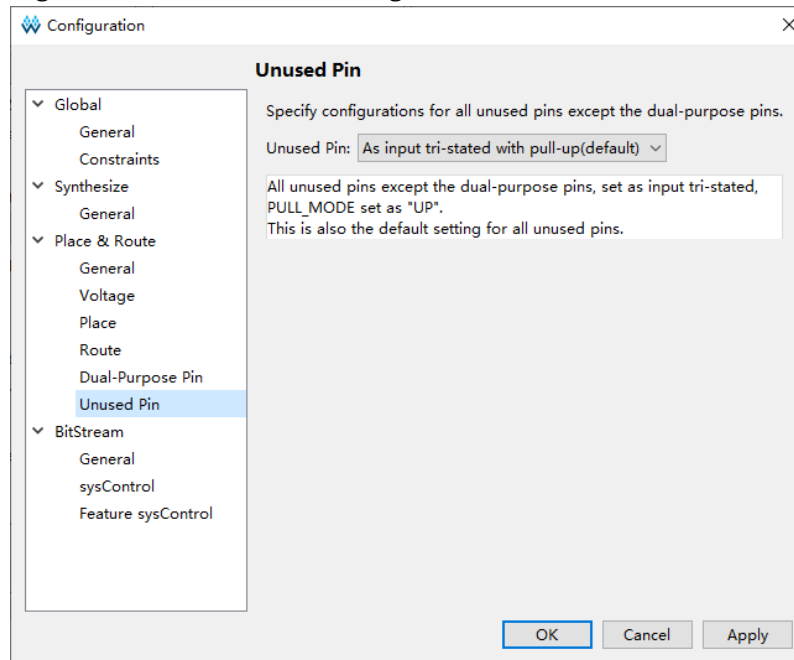
The dual-purpose pins are described as follows.

- **Use JTAG as regular IO:** Use relevant pins of JTAG as regular IO pins.
- **Use SSPI as regular IO:** Use relevant pins of SSPI as regular IO pins. For GW5A-25 MBGA121N, this option is checked by default and cannot be changed.
- **Use MSPI as regular IO:** Use relevant pins of MSPI as regular IO pins.
- **Use READY as regular IO:** Use the READY pin as regular IO pin.
- **Use DONE as regular IO:** Use the DONE pin as regular IO pin.
- **Use RECONFIG\_N as regular IO:** Use the RECONFIG\_N pin as regular IO pin.
- **Use I2C as regular IO:** Use relevant pins of I2C as regular IO.
- **Use CPU as regular IO:** Only Arora V and GW3A-20 devices support this option. Use relevant pins of CPU as regular IO.

### Unused Pin

The Unused Pin option allows users to set different IO attributes for unused GPIOs. There are two options: "As input tri-stated with pull-up (default)" and "As open drain driving ground", as shown in Figure 4-27.

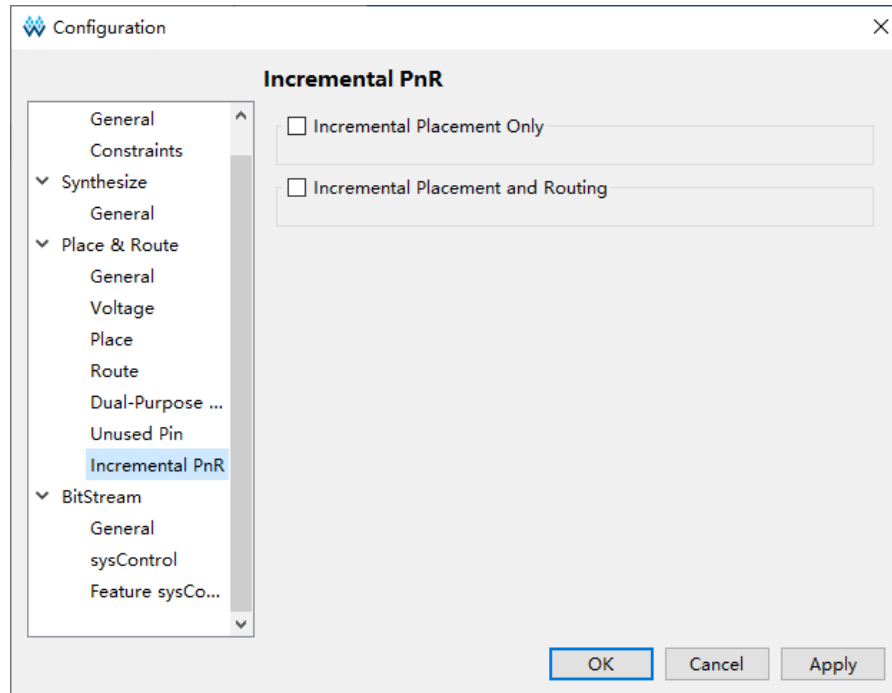
**Figure 4-27 Unused Pin Configuration**



- As input tri-stated with pull-up (default): Default option; all unused GPIOs will be configured as input tri-stated with weak pull-up.
- As open drain driving ground: All unused GPIOs are configured to output with OPEN\_DRAIN ON.

### Incremental PnR

The Incremental PnR can be used to enable incremental compilation, which can reuse the placement or routing results from the previous running, thereby reducing the time spent on re-PnR, and improving overall efficiency. The option configuration is as shown in Figure 4-28.

**Figure 4-28 Incremental PnR Configuration**

The descriptions for the options in Figure 4-28 are as follows:

**Incremental Placement Only:** Only increments placement information. By default, this option is unchecked. When it is checked, the following sub-options are displayed:

- **Auto:** Automatically select the existing incremental placement file (\*.p) in the project directory when redoing the placement. If no \*.p file exists in the project directory, a prompt will pop up.
- **Specify the previous placement file:** Manually specify the incremental placement file (\*.p).

**Incremental Placement and Routing:** Increments placement and routing information. By default, this option is unchecked. When it is checked, the following sub-options are displayed, and the "Incremental Placement Only" option becomes unavailable.

- **Auto:** Automatically select the existing incremental placement and routing file (\*.pr) in the project directory when redoing placement and routing. If no \*.pr file exists in the project directory, a prompt will pop up.
- **Specify the previous placement and routing file:** Manually specify the incremental placement and routing file (\*.pr).

#### **Note!**

Only Arora V and GW3A-20 devices support the incremental compilation. For other devices, this configuration option is not displayed in the configuration interface.

#### **BitStream**

You can configure the bitstream file format and frequency, etc. via BitStream. Hovering the mouse over the option will display its explanation. BitStream option includes General, sysControl, and Feature sysControl,

and the descriptions are as shown Table 4-3.

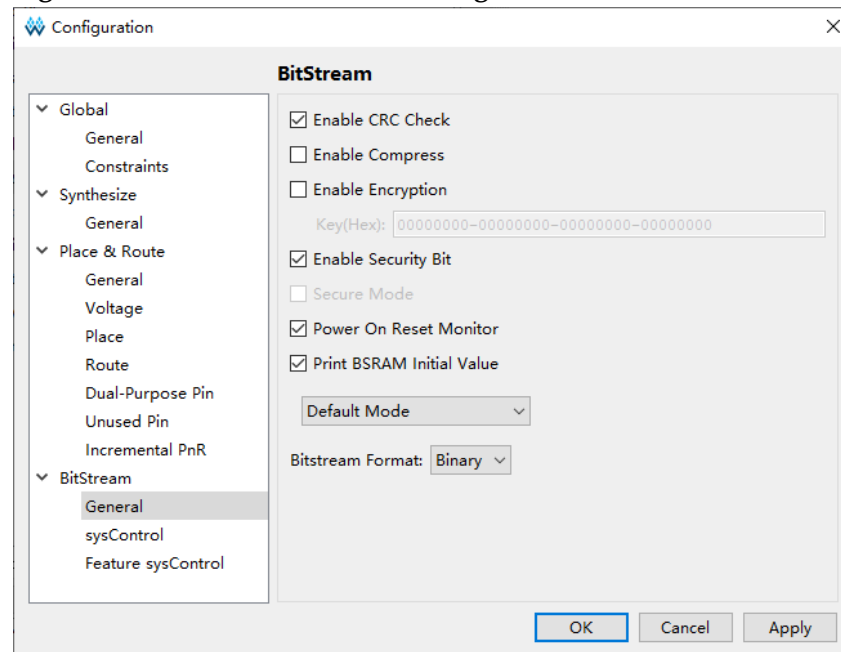
**Table 4-3 BitStream Configuration Options**

Option	Description
General	Set BitStream parameters
sysControl	Set BitStream system control parameters
Featruer sysControl	Set BitStream functional system control parameters

### General

The General configuration is as shown in Figure 4-29.

**Figure 4-29 Bitstream General Configuration**



The description for each parameter in Figure 4-29 is as follows.

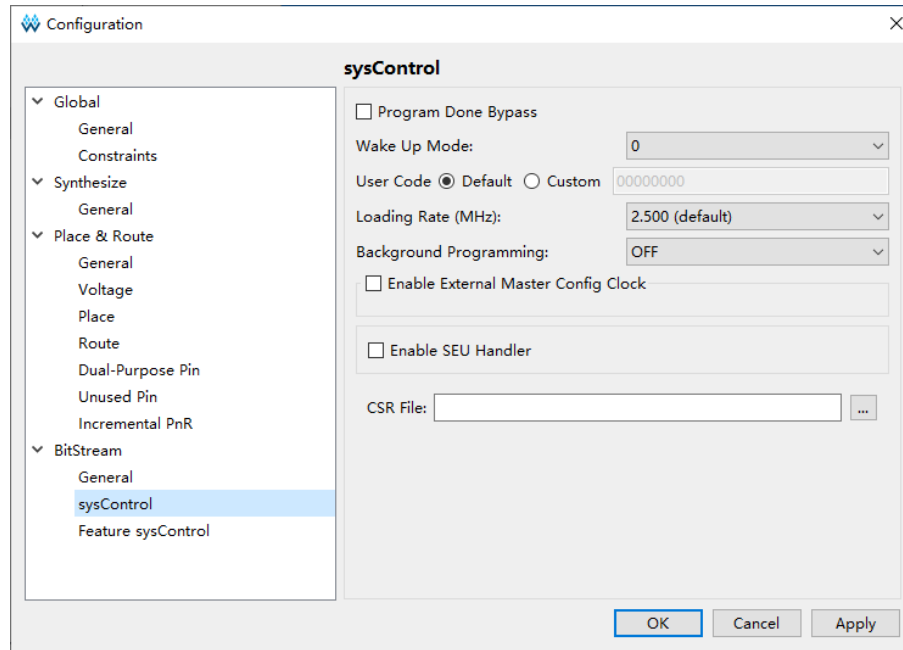
- **Enable CRC Check:** Enable CRC Check, checked by default.
- **Enable Compress:** Enable bitstream file compress, not checked by default.
- **Enable Encryption:** Encrypt the bitstream file, and only Arora Family devices support this option; for other devices, this option is not displayed on the interface, not checked by default.
- **Key (Hex):** Key (Hex) can be configured only when "Enable Encryption" is checked, and users can customize the secret key; only Arora Family devices support this option; for other devices, this option is not displayed on the interface. The key is 0 by default. When you check this option and run Place &Route, a key file with the extension .key will be generated.
- **Enable Security Bit:** Enable security bit, and add security bit to the bitstream file; after adding, the bitstream cannot be read back again,

checked by default.

- **Secure Mode:** Enable secure mode. Use JTAG pin as GPIO, and device can be programmed only once. This function is only supported by GW1NSER-4C, unchecked by default.
- **Power On Reset Monitor:** Power on reset monitoring, checked by default. When this option is checked, it will continuously monitor any possible voltage drop in the power rails. If the power rail voltage falls below the POR threshold, all RAM bits will be cleared and the used I/Os will be set to tri-state through internal weak pull-up resistors, and then the configuration and initialization will be completed in turn.
- **Turn Off Bandgap:** Turn off Bandgap, unchecked by default. Bandgap is used to provide constant voltage and current for some modules in the chip; turning off Bandgap can reduce device power. Only GW1N-1 supports this option; for the other devices, this option will not be displayed on the configuration interface.
- **Print BSRAM Initial Value:** Print the initial values of BSRAMs into the bitstream file and is enabled by default. For LittleBee and Arora families devices, enabling this option will allow the initial values of all BSRAM locations to be printed into the bitstream file, with unused BSRAM locations printed as 0. For Arora V and GW3A-20 devices, enabling this option will allow the initial values of all BSRAMs in the columns containing used BSRAM locations to be printed into the bitstream file, with unused BSRAM locations in those columns printed as 0. For GW5A(S)(T)-138/GW5AT-75 devices, if "MSPI JUMP Mode" or "Multi Boot Mode" is set to "Quad", and "Print BSRAM Initial Value" is checked, a drop-down menu with two options will be displayed, including "Default Mode" and "BSRAM Partial Print Mode", with "Default Mode" selected by default. When "Default Mode" is selected, the initial values of all BSRAM locations are printed into the bitstream file, and unused BSRAM locations are printed as 0; and when "BSRAM Partial Print Mode" is selected, the initial values of all BSRAMs in the columns containing used BSRAM locations are printed into the bitstream file, and unused BSRAM locations in those columns are printed as 0.
- **Bitstream Format:** Used to specify the bitstream file format, Text and Binary, and Binary by default. When the Text is selected, the \*.fs file in plain text format is generated; when the Binary is selected, a bitstream file in \*.fs, \*.bin, and \*.binx formats is generated. \*.bin and \*.binx are bitstream files in binary format, \*.binx file contains header annotation information, and \*.bin does not have header annotation information.

### **sysControl**

The sysControl configuration is as shown in Figure 4-30.

**Figure 4-30 sysControl Configuration**

The description for each parameter in Figure 4-30 is as follows.

- **Program Done Bypass:** When the Done Final signal is active, the external Done signal keeps low, so that the new bitstream can be forwarded after the bitstream is loaded.
- **Wake Up Mode:** Enable wake up mode, with the value of 0 and 1, and the default is 0.
  - When wake up mode is 0, DONE pin can be pulled up or down.
  - When wake up is 1,
    - a) If DONE pin is pulled up, download and run normally.
    - b) If DONE pin is pulled down, download normally; and DONE pin needs to be pulled up and keep TCK connected to the pulse signal to wake up chip.
- **User Code:** Users can customize User Code, and the defined value will be reflected in the generated bitstream file, and the User Code will be checked when the bitstream file is downloaded through the Programmer. The default value is Default (00000000).
- **Loading Rate:** In AutoBoot mode and MSPI mode, the rate of loading bitstream from Flash to SRAM. For GW1N-4/GW1NRF-4B/GW1NR-4, the default is 2.100MHz; for GW1NS-4/GW1NSR-4/GW1NSER-4C with speed grade C7/I6, the default is 2.6MHz; for GW5A(S)(T)-138/GW5A(R)-25, the default is 35.000MHz; for the other devices, the default is 2.500MHz. For the details, see [UG290, Gowin FPGA Products Programming and Configuration Guide](#); [UG714, Arora V 25K FPGA Product Programming and Configuration Guide](#); [UG704, Arora V 138K FPGA Product Programming and Configuration Guide](#). The loading rate and calculation method of different devices are

different.

- The loading rate of following packages only supports 2.500MHz.
  - a) GW1N-2:  
LQFP100X/LQFP144X/MBGA132X/WLCSP42H/MBGA49
  - b) GW1N-2 Version B:  
LQFP100X/LQFP144X/MBGA132X/MBGA121X
  - c) GW1N-2 Version C:  
LQFP100X/LQFP144X/MBGA132X/MBGA121X  
/MBGA49/QFN32X
  - d) GW1NR-2: MBGA49P/MBGA49PG/MBGA49G
  - e) GW1N-1P5: LQFP100X/QFN48X
- The loading rate and calculation of following devices is as shown in Table 4-4.
  - a) GW1NZ-1
  - b) GW1N-2/GW1N-1P5/GW1NR-2 except the above packages supporting 2.500MHz
  - c) GW1NSER-4C/GW1NS-4/GW1NSR-4/GW1NS-4C/  
GW1NSR-4C except the part number with speed grade C7/I6
  - d) GW1N-9/GW1NR-9
  - e) GW2A-18/GW2AR-18
  - f) GW2ANR-18 (Version C)
  - g) GW2A-55
  - h) GW2AN-55 (Version C)

**Table 4-4 Loading Rate and Formula (1)**

Loading Rate (MHz)	Formula
2.500 (default)	250 / 100
5.435	250 / 46
5.682	250 / 44
5.952	250 / 42
6.250	250 / 40
6.579	250 / 38
6.944	250 / 36
7.353	250 / 34
7.812	250 / 32
8.333	250 / 30
8.929	250 / 28
9.615	250 / 26
10.417	250 / 24
11.364	250 / 22

Loading Rate (MHz)	Formula
12.500	250 / 20
13.889	250 / 18
15.625	250 / 16
17.857	250 / 14
20.833	250 / 12
25.000	250 / 10
31.250	250 / 8
41.667	250 / 6
62.500	250 / 4

- The loading rate and calculation of following devices is as shown in Table 4-5.

#### GW1N-1/GW1N-1S/GW1NR-1

**Table 4-5 Loading Rate Value and Formula (2)**

Loading Rate (MHz)	Formula
2.500 (default)	240 / 96
2.553	240 / 94
2.609	240 / 92
2.667	240 / 90
2.727	240 / 88
2.791	240 / 86
2.857	240 / 84
2.927	240 / 82
3.000	240 / 80
3.077	240 / 78
3.158	240 / 76
3.243	240 / 74
3.333	240 / 72
3.429	240 / 70
3.529	240 / 68
3.636	240 / 66
3.750	240 / 64
3.871	240 / 62
4.000	240 / 60
4.138	240 / 58
4.286	240 / 56
4.444	240 / 54
4.615	240 / 52

Loading Rate (MHz)	Formula
4.800	240 / 50
5.000	240 / 48
5.217	240 / 46
5.455	240 / 44
5.714	240 / 42
6.000	240 / 40
6.316	240 / 38
6.667	240 / 36
7.059	240 / 34
7.500	240 / 32
8.000	240 / 30
8.571	240 / 28
9.231	240 / 26
10.000	240 / 24
10.909	240 / 22
12.000	240 / 20
13.333	240 / 18
15.000	240 / 16
17.143	240 / 14
20.000	240 / 12
24.000	240 / 10
30.000	240 / 8
40.000	240 / 6
60.000	240 / 4

- The loading rate and calculation of following devices is as shown in Table 4-6.

- a) GW2AN-9X
- b) GW2AN-18X

**Table 4-6 Loading Rate and Formula (3)**

Loading Rate (MHz)	Formula
2.500 (default)	200 / 80
1.562	200 / 128
1.587	200 / 126
1.613	200 / 124
1.639	200 / 122
1.667	200 / 120
1.695	200 / 118

Loading Rate (MHz)	Formula
1.724	200 / 116
1.754	200 / 114
1.786	200 / 112
1.818	200 / 110
1.852	200 / 108
1.887	200 / 106
1.923	200 / 104
1.961	200 / 102
2.000	200 / 100
2.041	200 / 98
2.083	200 / 96
2.128	200 / 94
2.174	200 / 92
2.222	200 / 90
2.273	200 / 88
2.326	200 / 86
2.381	200 / 84
2.439	200 / 82
2.564	200 / 78
2.632	200 / 76
2.703	200 / 74
2.778	200 / 72
2.857	200 / 70
2.941	200 / 68
3.030	200 / 66
3.125	200 / 64
3.226	200 / 62
3.333	200 / 60
3.448	200 / 58
3.571	200 / 56
3.704	200 / 54
3.846	200 / 52
4.000	200 / 50
4.167	200 / 48
4.348	200 / 46
4.545	200 / 44
4.762	200 / 42
5.000	200 / 40

Loading Rate (MHz)	Formula
5.263	200 / 38
5.556	200 / 36
5.882	200 / 34
6.250	200 / 32
6.667	200 / 30
7.143	200 / 28
7.692	200 / 26
8.333	200 / 24
9.091	200 / 22
10.000	200 / 20
11.111	200 / 18
12.500	200 / 16
14.286	200 / 14
16.667	200 / 12
20.000	200 / 10
25.000	200 / 8
33.333	200 / 6
50.000	200 / 4
100.000	200 / 2

- The loading rate and calculation of following devices is as shown in Table 4-7.

GW1N-4/GW1NRF-4B/GW1NR-4

**Table 4-7 Loading Rate and Formula (4)**

Loading Rate (MHz)	Formula
2.100 (default)	210 / 100
4.565	210 / 46
4.773	210 / 44
5.000	210 / 42
5.250	210 / 40
5.526	210 / 38
5.833	210 / 36
6.176	210 / 34
6.563	210 / 32
7.000	210 / 30
7.500	210 / 28
8.077	210 / 26
8.750	210 / 24

Loading Rate (MHz)	Formula
9.545	210 / 22
10.500	210 / 20
11.667	210 / 18
13.125	210 / 16
15.000	210 / 14
17.500	210 / 12
21.000	210 / 10
26.250	210 / 8
35.000	210 / 6
52.500	210 / 4

- The loading rate and calculation of following devices is as shown in Table 4-8.

GW1NSER-4C/GW1NS-4/GW1NSR-4/GW1NS-4C/  
GW1NSR-4C with speed grade C7/I6

**Table 4-8 Loading Rate and Formula (5)**

Loading Rate (MHz)	Formula
2.600	260 / 100
5.652	260 / 46
5.909	260 / 44
6.190	260 / 42
6.500	260 / 40
6.842	260 / 38
7.222	260 / 36
7.647	260 / 34
8.125	260 / 32
8.667	260 / 30
9.286	260 / 28
10.000	260 / 26
10.833	260 / 24
11.818	260 / 22
13.000	260 / 20
14.444	260 / 18
16.250	260 / 16
18.571	250 / 14
21.667	260 / 12
26.000	260 / 10
32.500	260 / 8

Loading Rate (MHz)	Formula
43.333	260 / 6
65.000	260 / 4

- The loading rate and calculation of following devices is as shown in Table 4-9.

GW5A(S)(T)-138/GW5A(R)-25/GW5AT-75

**Table 4-9 Loading Rate and Formula (6)**

Loading Rate (MHz)	Formula
35.000(default)	210 / 6
52.500	210 / 4
70.000	210 / 3
105.000	210 / 2

- The loading rate and calculation of following devices is as shown in Table 4-10.

GW5AT-60/GW5A(N)(R)T-15

GW3A-20

**Table 4-10 Loading Rate and Formula (7)**

Loading Rate (MHz)	Formula
2.500 (default)	210 / 84
1.667	210 / 126
1.694	210 / 124
1.721	210 / 122
1.750	210 / 120
1.780	210 / 118
1.810	210 / 116
1.842	210 / 114
1.875	210 / 112
1.909	210 / 110
1.944	210 / 108
1.981	210 / 106
2.019	210 / 104
2.059	210 / 102
2.100	210 / 100
2.143	210 / 98
2.188	210 / 96
2.234	210 / 94

Loading Rate (MHz)	Formula
2.283	210 / 92
2.333	210 / 90
2.386	210 / 88
2.442	210 / 86
2.561	210 / 82
2.625	210 / 80
2.692	210 / 78
2.763	210 / 76
2.838	210 / 74
2.917	210 / 72
3.000	210 / 70
3.088	210 / 68
3.182	210 / 66
3.281	210 / 64
3.387	210 / 62
3.500	210 / 60
3.621	210 / 58
3.750	210 / 56
3.889	210 / 54
4.038	210 / 52
4.200	210 / 50
4.375	210 / 48
4.565	210 / 46
4.773	210 / 44
5.000	210 / 42
5.250	210 / 40
5.526	210 / 38
5.833	210 / 36
6.176	210 / 34
6.563	210 / 32
7.000	210 / 30
7.500	210 / 28
8.077	210 / 26
8.750	210 / 24
9.545	210 / 22
10.500	210 / 20
11.667	210 / 18
13.125	210 / 16

Loading Rate (MHz)	Formula
15.000	210 / 14
17.500	210 / 12
21.000	210 / 10
26.250	210 / 8
35.000	210 / 6
52.500	210 / 4
70.000	210 / 3
105.000	210 / 2

- **Background Programming:** You can re-program Flash without interrupting the current FPGA running. If background programming value of the device is only OFF, the configuration option will not be displayed on the configuration interface.

Figure 4-31 Select I2C

Background Programming: I2C ▼  
I2C Slave Address(Hex): 00 (00~7F)

Figure 4-32 Select I2C/JTAG/SSPI/QSSPI

Background Programming: I2C/JTAG/SSPI/QSSPI ▼  
 HOTBOOT

The devices that support background programming and their values are shown in Table 4-11.

Table 4-11 Background Programming Value

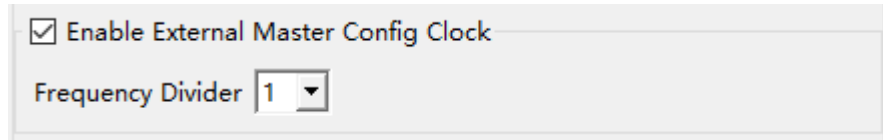
Device	Background Programming Value
<ul style="list-style-type: none"> <li>● GW1N-1P5/GW1N-2/GW1NR-2</li> <li>● Version B: GW1N-4/GW1NR-4, GW1NRF-4</li> <li>● Version D: GW1NR-4</li> <li>● GW1NS-4/GW1NSR-4</li> <li>● GW1N-9/GW1NR-9</li> <li>● GW1NZ-1</li> </ul>	OFF, JTAG; OFF by default
Version B: GW1N-1P5/GW1N-2/GW1NR-2	OFF, JTAG, I2C; OFF by default
Version C: GW1N-2/GW1NR-2/GW1N-1P5	OFF, GoConfig, GoConfig Mode1, JTAG, I2C; OFF by default
GW2AN-18X/GW2AN-9X	OFF, GoConfig, UserLogic, I2C/JTAG/SSPI/QSSPI; OFF by default
Arora V/GW3A-20	OFF, UserLogic, JTAG/SSPI/QSSPI, OFF by default

Background Programming values and using considerations are described as follows.

- OFF: Off Background Programming, if the device is GW2AN-18X or GW2AN-9X, "Use MSPI as regular" in the "Dual-Purpose Pin" dialog box is unchecked and non-configurable.
- JTAG: Use JTAG mode for background programming
- I2C: Use I2C mode for background programming: For GW1N-1P5/GW1N-2/GW1NR-2 devices in version B, "I2C Slave Address (Hex)" is used to set the address of the I2C device, with the value range of 00~7F, as shown in Figure 4-31. After selecting I2C, "Use JTAG as regular IO" in the "Dual-Purpose Pin" dialog box is unchecked and not configurable. For GW1N-2/GW1N-1P5/GW1NR-2 devices in version C, when using I2C mode for background programming, there is no option "I2C Slave Address (Hex)" in the configuration dialog box; and "Use RECONFIG as regular IO" is unchecked and non-configurable in the "Dual-Purpose Pin" dialog box.
- GoConfig: Use goConfig IP for background programming.
- UserLogic: Use internal logic for background programming.
- I2C/JTAG/SSPI/QSSPI: Use I2C/JTAG/SSPI/QSSPI mode for background programming.
- JTAG/SSPI/QSSPI: Use JTAG/SSPI/QSSPI mode for background programming.
- For GW2AN-18X/GW2AN-9X devices, when GoConfig, UserLogic, or I2C/JTAG/SSPI/QSSPI is selected, the option "HOTBOOT" will be displayed in the dialog box, optional and unchecked by default, as shown Figure 4-32.
- For GW5A(S)(T)-138/GW5A(R)-25/GW3A-20 devices, when UserLogic or JTAG/SSPI/QSSPI is selected, the option "HOTBOOT" will be displayed in the dialog box, optional and unchecked by default, as shown Figure 4-32.
- For GW1N-1P5/GW1N-2/GW1NR-2 in version B, if the I2C is included in the two switched configuration items, Synthesize and Place & Route will be changed to expired; for GW1N-2/GW1NR-2/GW1N-1P5 in version C, if the I2C is included in the two switched configuration items, only Place & Route will be changed to expired.
- For GW2AN-18X/GW2AN-9X, if the configuration items GoConfig and UserLogic are switched with I2C/JTAG/SSPI/QSSPI and OFF, Synthesize and Place & Route will be changed to expired, otherwise only Place & Route will be changed to expired.
- Enable External Master Config Clock: Enable the external master config clock, only Arora V and GW3A-20 devices support this option; for other devices, this option is not displayed on the configuration

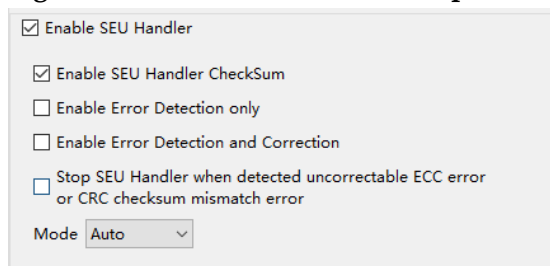
interface, unchecked by default. When this option is checked, the configuration option "Frequency Divider" will appear in the dialog box, as shown in Figure 4-33. For GW5A(S)(T)-138/GW5AT-75 devices, the values are 1, 2, 4, 8, and the default is 1. For GW5A(S)(R)-25/GW5AT-60/GW5A(N)(R)T-15/GW3A-20 devices, the values are 1 and even numbers from 2 to 1022; and there are totally 512 values, and the default is 1.

**Figure 4-33 Frequency Divider Option**

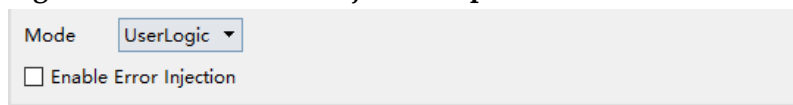


- **Enable SEU Handler:** Enable Single-Event Upsets Handler (SEU Handler). Only Arora V and GW3A-20 devices support this function, unchecked by default. When this option is checked, the configuration sub-options "Enable SEU Handler CheckSum", "Enable Error Detection only", "Enable Error Detection and Correction", "Stop SEU Handler when detected uncorrectable ECC error or CRC checksum mismatch error", "Mode", and "Enable Error Injection". Among them, "Enable Error Detection only" and "Enable Error Detection and Correction" cannot be checked at the same time, as shown in Figure 4-34.

**Figure 4-34 Enable SEU Handler Option**



**Figure 4-35 Enable Error Injection Option**



- **Enable SEU Handler CheckSum:** Enable Single-Event Upsets Handler, detection, calculation and comparison, unchecked by default.
- **Enable Error Detection only:** Enable error detection only, unchecked by default.
- **Enable Error Detection and Correction:** Enable error detection and correction, unchecked by default.
- **Stop SEU Handler when detected uncorrectable ECC error or CRC checksum mismatch error:** Stop SEU Handler when uncorrectable

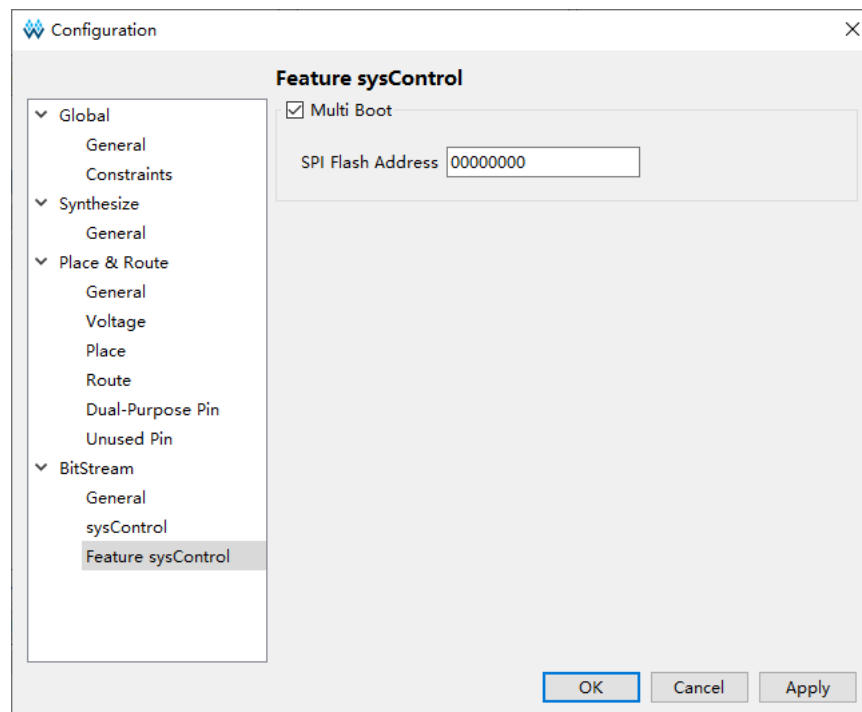
ECC error or CRC checksum mismatch error is detected, unchecked by default.

- Mode: Select SEU Handler start or stop mode; the values are Auto and UserLogic, and the default is Auto.
- Enable Error Injection: The option Enable Error Injection appears when UserLogic mode is selected, unchecked by default, as shown in Figure 4-35.
- CSR File: Used to specify the CSR file.

### **Feature sysControl**

For Gowin devices apart from Arora V devices, the Feature sysControl configuration is as shown in Figure 4-36.

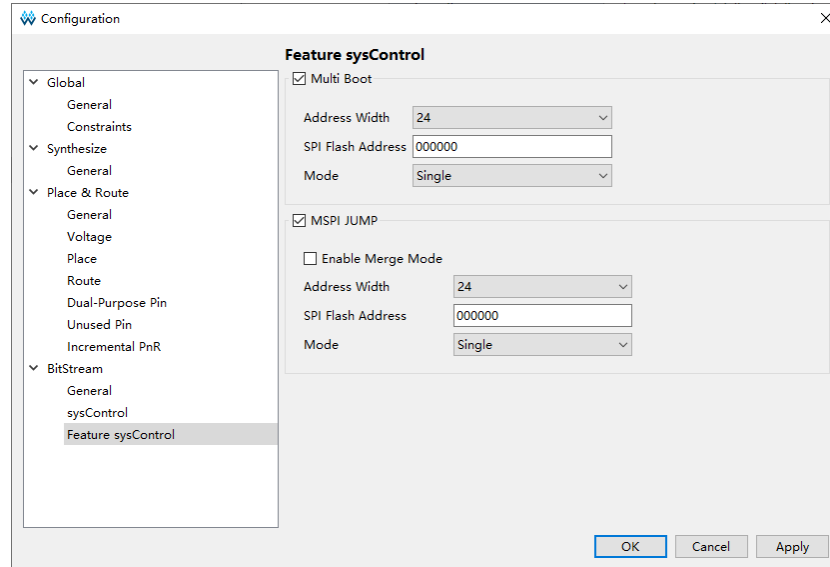
**Figure 4-36 Feature sysControl Configuration for Gowin Devices apart from Arora V Devices**



Multi Boot is checked by default, and the sub-configuration SPI Flash Address will appear.

- SPI Flash Address: Specify SPI Flash address. The SPI Flash address refers to the initial address to which the bitstream will be loaded for the next multiboot. For GW2AN-18X and GW2AN-9X, the default is 000000; for the devices other than Arora V devices, the default value is 00000000. For further details, see [SUG502, Gowin Programmer User Guide](#).

For Arora V and GW3A-20 devices, the Feature sysControl configuration is as shown in Figure 4-37.

**Figure 4-37 Feature sysControl Configuration for Arora V and GW3A-20 Devices**

Multi Boot is unchecked by default, and the following sub-configurations will be displayed when it is checked.

**Table 4-12 Sub-configurations**

Name	Description
Address Width	Configure SPI Flash address width; the values are 24 and 32, and the default is 24.
SPI Flash Address	Specify SPI Flash address. The SPI Flash address refers to the initial address to which the bitstream will be loaded for the next multiboot. The default is 000000; for further details, see <a href="#">SUG502, Gowin Programmer User Guide</a> .
Mode	Configure SPI Flash address access mode; the values are Single, Fast, Dual and Quad, and the default is Single.

MSPI JUMP is unchecked by default, and the following sub-configurations will be displayed when it is checked.

**Table 4-13 Sub-configurations**

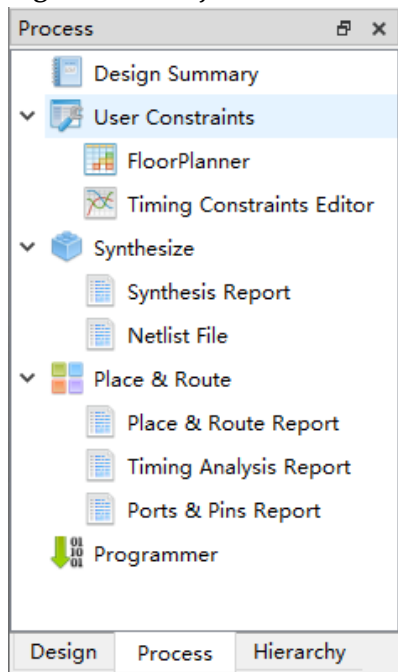
Name	Description
Enable Merge Mode	Using this option will merge the MSPI JUMP bitstream file into a general bitstream file, unchecked by default.
Address Width	Configure SPI Flash address width; the values are 24 and 32, and the default is 24.
SPI Flash Address	Specify SPI Flash address, and the default is 000000.
Mode	Configure SPI Flash address access mode; the values are Single, Fast, Dual and Quad, and the default is Single.

## 4.4 Manage a Project

The Process view provides the process of FPGA design flow, as shown in Figure 4-38. The Process View includes following operations.

- View design summary
- Start physical constraints editor
- Start timing constraints editor
- Run Synthesis
- View Synthesis report
- Run Place & Route
- View reports generated after Place & Route
- Start Programmer

**Figure 4-38 Project Process View**



### 4.4.1 Design Summary

A new project created, the software will analyze the project and provide a report of Design Summary, which will include the project file path, synthesis information and device information, as shown in Figure 4-39. There are three following ways to open the Design Summary:

- From the menu bar, select "Window > Design Summary".
- In the Process View, double-click "Design Summary".
- In the Process View, right-click "Design Summary", and select "Open".

**Figure 4-39 Project Summary**

General	
Project File:	D:\gowin_project\daily_test\daily_test.gprj
Synthesis Tool:	GowinSynthesis

Target Device	
Part Number:	GW1N-UV4PG256C6/I5
Series:	GW1N
Device:	GW1N-4
Device Version:	B
Package:	PBGA256
Speed Grade:	C6/I5
Core Voltage:	UV

**Note!**

For devices without version, the Device Version will not be displayed in the table.

## 4.4.2 User Constraints

User constraints provide quick access to open and create constraints files. User constraints include physical and timing constraints.

For the details, please refer to [SUG940, Gowin Design Timing Constraint User Guide](#), and [SUG935, Gowin Design Physical Constraints User Guide](#); [SUG1018, Arora V Design Physical Constraints User Guide](#).

## 4.4.3 Synthesize

GowinSynthesis is the synthesis tool developed by Gowin. It supports GOWINSEMI library files and their implementations. It supports System Verilog 2017, Verilog 2001, Verilog 95, VHDL 1993, VHDL 2008, and VHDL 2019.

Right-click "Synthesize" and select "Configuration" in the Project Design area to open the configuration dialog box, as shown in Figure 4-21.

Synthesize provides functions of running synthesis, setting synthesis parameters, and managing Netlist File and Synthesis Report. For the Synthesis Report, see [6.1 Synthesis Report](#).

Refer to the following steps to run Synthesize.

1. Configure synthesis, and you can refer to [4.3.3 Edit Project Configuration](#).
2. Run Synthesize
3. In the Process pane, double click "Synthesize" or right-click "Synthesize" and select "Run" to start synthesis of source files. If the synthesis is successful, the icon "✔" appears before Synthesize; if not, the icon "❗" appears.
4. After synthesis completed successfully, double click "Netlist Report", "Synthesis Report" or right-click and select "Open" to view the Netlist Report and synthesis report. The post-synthesis generated netlist file is \*.vg, and synthesis report file is \*\_syn.rpt.html.

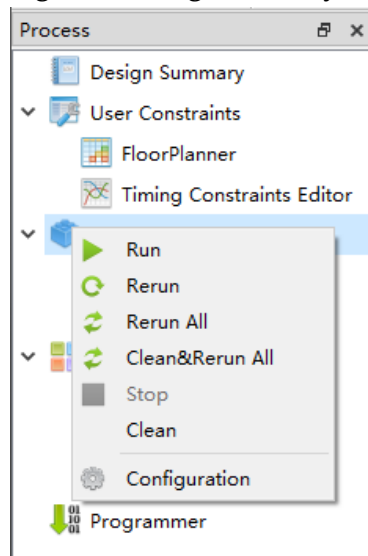
If the Synthesize icon is "❗" before synthesis, double click "Netlist File", "Synthesis Report" or right click to select "Open" to synthesize first,

and the netlist file or synthesis report can be opened after successful synthesis.

The right-click operations of Synthesize is as shown in Figure 4-40.

- Run: Only when the icon before Synthesize is "🏠" (Initial Status), "❗" (Failure Status), or "❓" (Expired Status), you can select Run to start synthesis of source files.
- Rerun: No matter what Synthesize status is, you can select Rerun to restart synthesis of source files.
- Rerun All: If this option selected, regardless of the status of "Place & Route" and "Synthesize", the source file will be synthesized and placed & routed again
- Clean & Rerun All: Clean the gwsynthesis and pnr folders under the project folder impl, and synthesize and place & route the source files again.
- Stop: Stop Synthesize
- Clean: Clean the generated folder after synthesis (a folder generated by GowinSynthesis is gwsynthesis). Click it and a prompt will pop up.
- Configuration: Configure Synthesis parameters

Figure 4-40 Right-click Synthesize



#### 4.4.4 Place & Route

Place and route provides the functions of running PnR, setting parameters, and managing the generated files.

##### Note!

Place & Route will be implemented after running Synthesize.

Refer to the following steps to run Place & Route.

1. Configure Place & Route, please refer to [4.3.3 Edit Project Configuration](#).

2. Run Place & Route, double-click "Place & Route", or right-click and select "Place & Route > Run" to generate bitstream files and related reports. If running successfully, the "✔" icon will appear before Place & Route. Otherwise, the "!" icon will appear;
3. After Place & Route has been run successfully, double-click on "View Post PnR Report" or right-click and select "Open" to view the report.
4. You can view four kinds of reports: Place & Route Report, Timing Analysis Report, Ports & Pins Report, and Power Analysis Report. These reports can not be edited. See [6.2 Place & Route Report](#), [6.3 Ports and Pins Report](#), [6.4 Timing Report](#), [6.5 Power Analysis Report](#) for the details.

**Note!**

- If the report is already opened and it is regenerated by running Place & Route again, a update prompt will pop up.
- Before running Place & Route, if the status icon before Place & Route is "🟦🟩🟨", double click the report or right-click and select "Open" to run Place & Route first. The report will be opened after Place & Route runs successfully.

Right-click operations of Place & Route are as follows.

- Run: You can select "Run" to start Place & Route only when the icon before Place & Route is "🟦🟩🟨", "!", or "?".
- Rerun: Regardless of the Place & Route status, you can select Rerun to rerun Place & Route.
- Rerun All: If this option selected, regardless of the status of "Place & Route" and "Synthesize", the source file will be Synthesize and placed & routed again.
- Clean & Rerun All: Clean the gwsynthesis and pnr folders under the project folder impl, and synthesize and place & route the source files again.
- Stop: Stop Place & Route
- Clean: Clean all the generated files after PnR; a prompt will pop up when you click this option. A Warning message will be reported if the deletion of a folder fails.
- Configuration: Configure Place & Route parameters.

## 4.4.5 Programmer

Bitstream files will be generated after Gowin Software has run placement and routing. Start Gowin FPGA programmer to download the bitstream files to the chip to realize user-required functions.

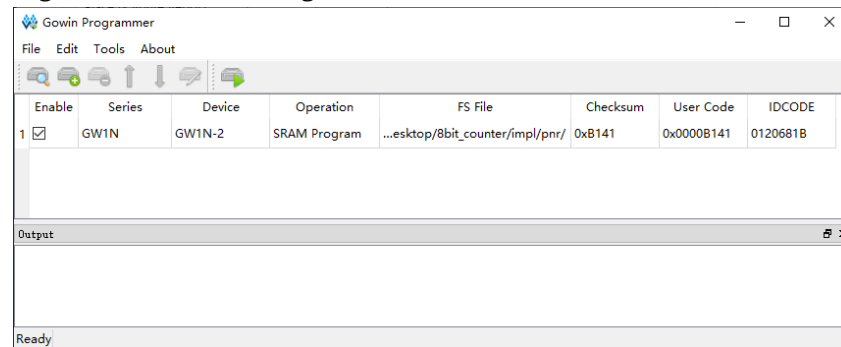
**Note!**

Programmer will be implemented after running Synthesize and Place & Route. If you do not run synthesize and Place & Route first, warnings will appear.

Double-click "Programmer" or right click and select "Run" to open Gowin FPGA Programmer, as shown in Figure 4-41.

**Note!**

The Programmer in the Linux installation package does not work with Linux Red Hat 5.10, only works with Red Hat 6 and above, and the Linux core version needs to be 2.18 and above.

**Figure 4-41 Gowin Programmer**

For the usage, please refer to [SUG502, Gowin Programmer User Guide](#).

## 4.5 Archive and Restore a Project

Gowin Software can archive project and restore archived project. Use "Archive Project" and "Restore Archived Project" under "Project" in the menu bar to archive or restore archived project.

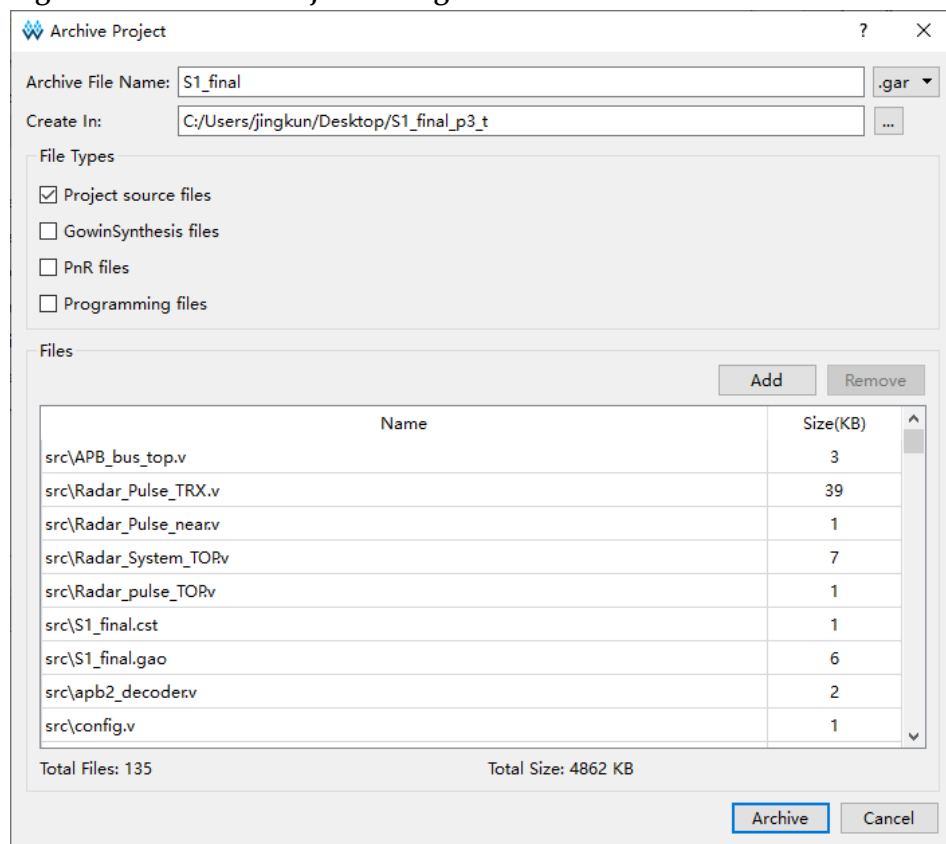
### 4.5.1 Archive a Project

A dialog box will pop up when you click "Project > Archive Project", as shown in Figure 4-42; an explanation is displayed when your mouse hover over an option.

- Archive File Name is the archived file name. The default name is the same as the current archived project name with extension .gar.
- Create In is the path for the archived file, and the default is the current project path.
- The File Types include Project source files (checked by default), GowinSynthesis files, PnR files and Programming files.
  - Project source files: Includes all the files under the path /src where the project is located.
  - GowinSynthesis files: Includes project files (\*.prj), netlist files (\*.vg), synthesis reports (\*\_syn.rpt.html), resource statistics files (\*\_syn\_rsc.xml) generated synthesis under the path /impl/gwsynthesis where the project is located.
  - PnR files: Includes the files generated by PnR under the path /impl/pnr where the project is located.
  - Programming files: Includes the bitstream file \*.fs, \*.bin and \*.binx generated by PnR under the path /impl/pnr where the project is located.

- When a file type is checked, the source file, path and size of the current project are displayed below.
- Add and Remove can be used to add and remove archived files.
- After clicking Archive, a prompt box will pop up if the files in the project are not saved.
- After archiving, a prompt will pop up, indicating the success or failure of the archiving.
- When the archiving is completed, two files will be generated under the "Create In" path: the archived project \*.gar and the archived file \*.garlog. The file with .gar suffix compresses and stores all the archived files. The log file with \*.garlog suffix is used for checking which files are archived and whether the archiving is successful.

**Figure 4-42 Archive Project Dialog Box**



## 4.5.2 Restore Archived Project


Restore Archived Project dialog will pop up when you clicks Project in the menu bar, as shown in Figure 4-43 .

**Figure 4-43 Restore Archived Project Dialog Box**

Click the button on the right side of Archived File to select the archived file to restore. After selecting, "Destination Folder" is automatically updated to the path where the archive file is. Click "OK" and a dialog box will pop up.

## 4.6 Exit Software

There are two ways to exit Gowin Software.

1. Select "File > Exit" from the File menu.
2. Click the " " icon on the upper right of the IDE.

### Note!

- If files are not saved, IDE will prompt you to save the files first.
- Save, Save All, and Save As... are only available for text editing.
- Project configuration modification and project files addition and deletion will not be saved to project configuration files in time; they will be saved automatically when you close the software.
- If the software is running, you cannot exit software by clicking.

# 5 Tools Integrated in Gowin Software

## 5.1 Physical Constraints Editor

Gowin FloorPlanner is designed in-house by Gowin, and it supports reading and editing the attributes and locations of I/O, Primitive, Block (BSRAM and DSP), and Group, etc. It also supports the generation of new placement and constraints files according to your configuration. These files define the I/O attributes, primitives and locations, etc. Gowin FloorPlanner, supporting Gowin all FPGA products, provides an editing way to improve design efficiency, and it also supports timing optimization.

FloorPlanner can be started using two methods.

1. If no FPGA project is created, you can select "Tools > FloorPlanner" directly from the menu bar. You will need to add netlist files and devices information by selecting "File > New".
2. If an FPGA project is already created, run "Synthesize", and then double-click "FloorPlanner" directly in the Process View. The Floorplanner will then load the project files directly. The FloorPlanner includes Summary, Netlist, Chip Array, Package View, as shown in Figure 5-1 and Figure 5-2.

**Note!**

- For more details, see [SUG935, Gowin Design Physical Constraints Guide](#); [SUG1018, Arora V Design Physical Constraints User Guide](#).
- The FloorPlanner also supports timing optimization.

Figure 5-1 Chip Array View

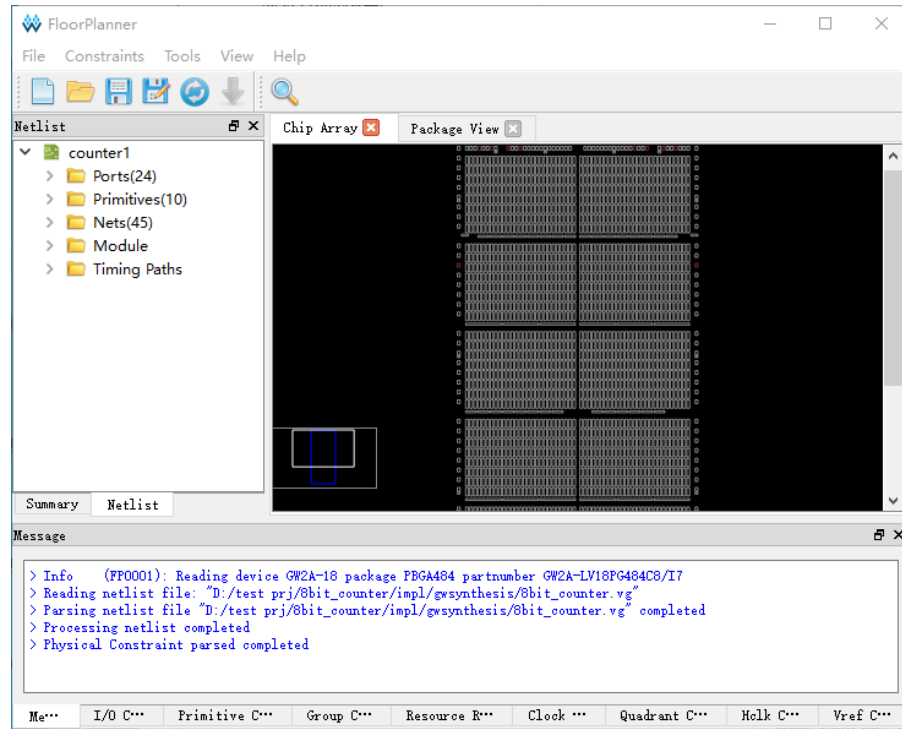
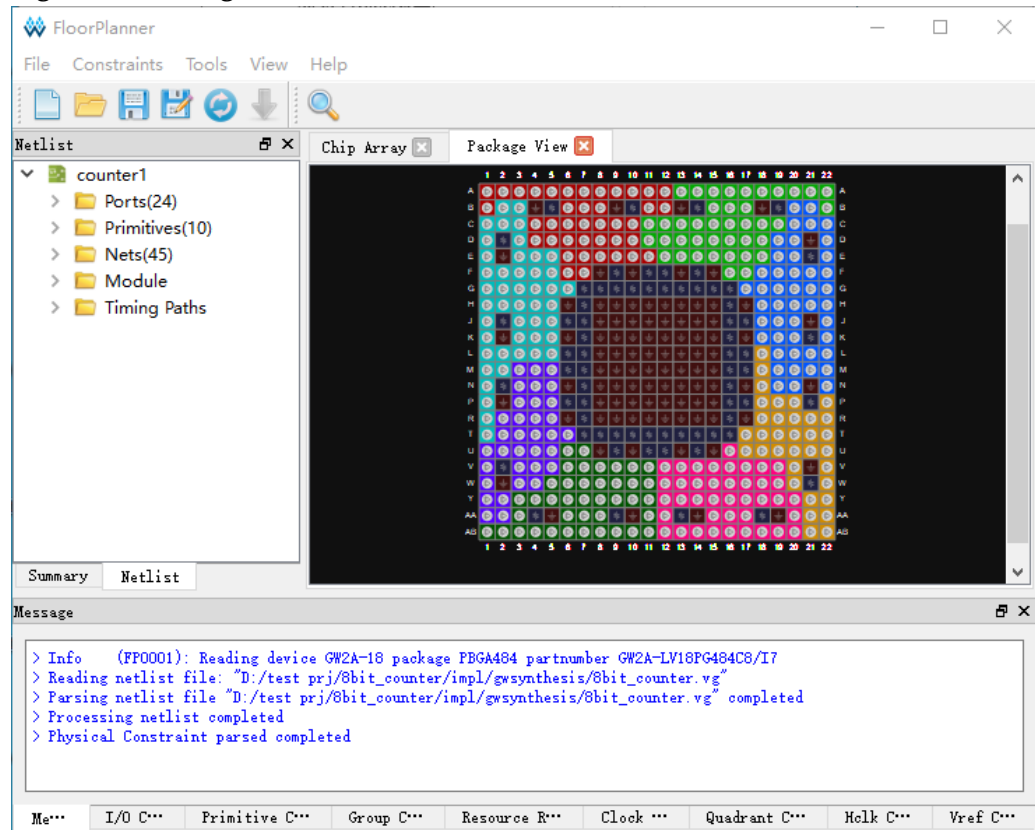


Figure 5-2 Package View



## 5.2 Timing Constraint Editor

The Gowin Timing Constraints Editor is designed in-house by Gowin,

and supports multiple timing constraints commands, including clock constraints, I/O constraints, path constraints, and clock report editing. The Timing Constraints Editor allows an easy and quick timing constraint editing for Gowin all FPGA products.

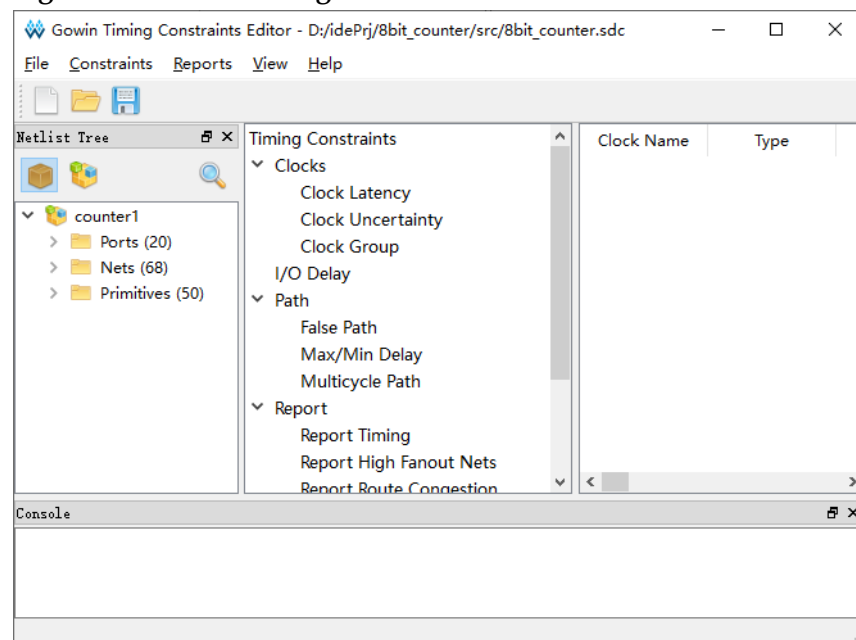
Timing Constraints Editor can be started using two methods:

1. If no FPGA project is created, you can select "Tools > Timing Constraints Editor" from the menu bar. Add netlist files by selecting "File > New".
2. If an FPGA project is already created, Run "Synthesize", double-click "Timing Constraints Editor", and the Timing Constraints Editor will load project files directly, as shown in Figure 5-3.

#### Note!

For the details, see [SUG940, Gowin Design Timing Constraint User Guide](#).

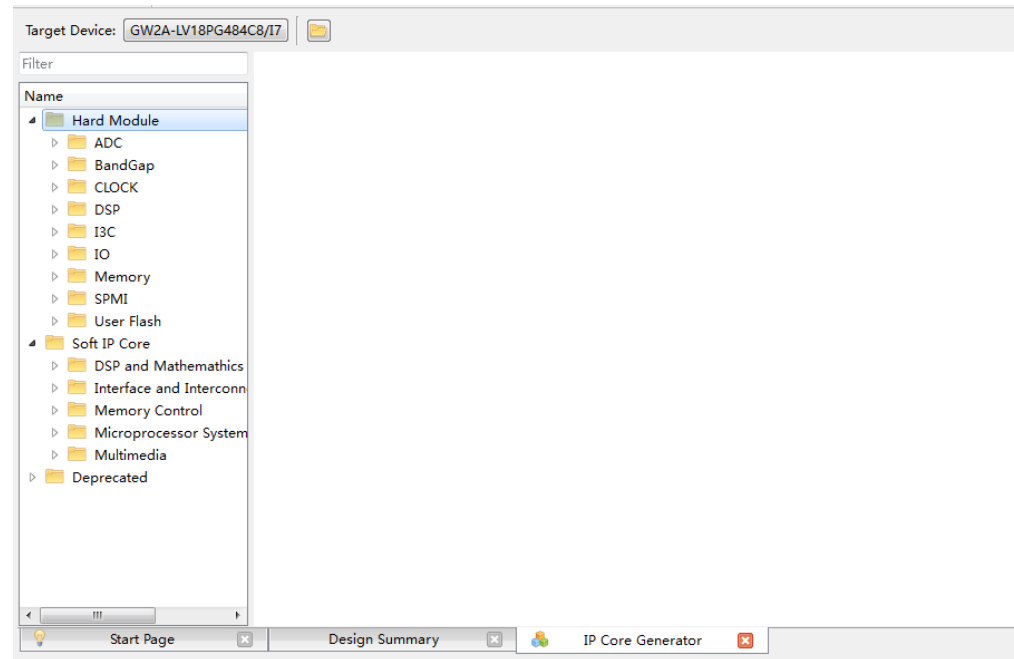
**Figure 5-3 Create Timing Constraints**



## 5.3 IP Core Generator

The IP Core Generator in Gowin Software is mainly used to generate hard and soft IPs, which you can call to implement the required functions. As shown in Figure 5-4, its main functions are as follows.

- Supports Soft IP core, Hard module information preview
- Supports customized Soft IP core and Hard module.
- Supports Hard module instance generation.
- Can save configuration automatically.
- Supports IP generation code language selection.
- Some Soft IP can generate incentive file automatically.
- Can display available IPs by selecting device.

**Figure 5-4 IP Core Generator**

Start the IP Core Generator by selecting "IP Core Generator" from the Tools menu. For the details, you can see following manuals.

- For the details of ADC, BANDGAP, I3C and SPMI, you can see [SUG283, Gowin Primitives User Guide](#); [UG299, Arora V Series Analog to Digital Converter \(ADC\) User Guide](#).
- For the details of CLOCK, you can see [UG286, Gowin Clock User Guide](#); [UG306, Arora V Clock User Guide](#).
- For the details of DSP, you can see [UG287, Gowin Digital Signal Processing User Guide](#); [UG305, Arora V Digital Signal Processing \(DSP\) User Guide](#).
- For the details of IO Logic, you can see [UG289, Gowin Programmable IO \(GPIO\) User Guide](#); [UG300, Arora V BSRAM & SSRAM User Guide](#).
- For the details of BSRAM & SSRAM, you can see [UG285, Gowin BSRAM & SSRAM User Guide](#); [UG300, Arora V BSRAM & SSRAM User Guide](#).
- For the details of User Flash, you can see [UG295, Gowin User Flash User Guide](#).
- For the soft IPs reference design, you can click this [link](#).

**Note!**

The grayed out Hard Module or Soft IP Core is not supported by the current device.

## 5.4 Gowin Analyzer Oscilloscope

The Gowin Analyzer Oscilloscope (GAO) is a digital signal analyzer that is designed in-house by Gowin. It helps you to analyze signal timing in design more easily, and quickly perform system analysis and fault locating,

thereby improving design efficiency.

GAO supports RTL-level signal capture and netlist-level signal capture after synthesis, and provides standard version (Standard) and simplified version (Lite). Standard GAO can support up to 16 AOs, each of which can be configured with one or more trigger ports, supporting multi-level static or dynamic trigger expressions. Lite GAO is easy to configure, and you do not need to set trigger conditions, and it also can capture the initial value of the signal, which is convenient for you to analyze the state of power-on. After signal capture, the waveform can be exported, supporting \*.csv, \*.vcd and \*.prn file formats. \*.csv and \*.prn files can be directly used in matlab and other third-party simulation tools, and \*.vcd file can be directly used in ModelSim.

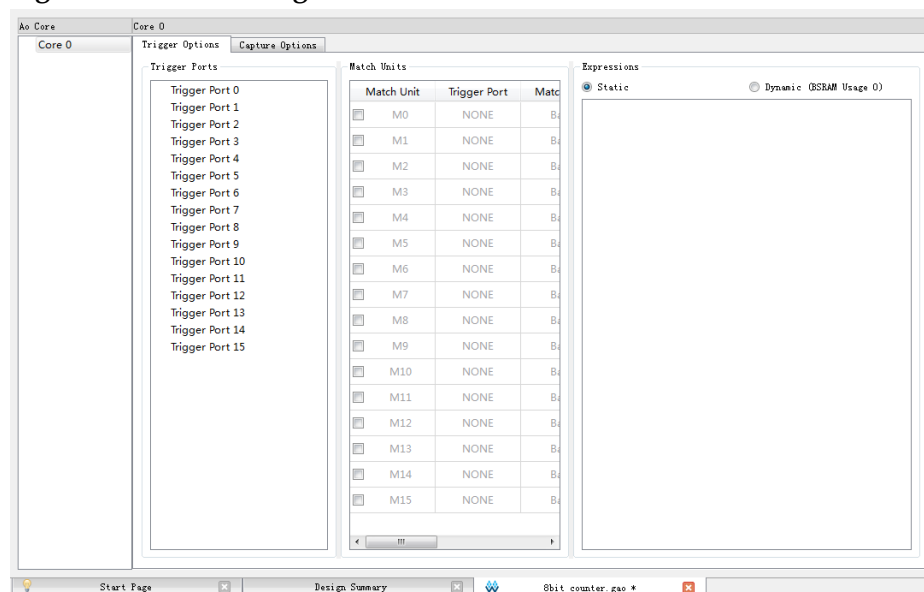
**Note!**

Matlab and ModelSim tools require a third-party license.

The GAO includes Gowin GAO configuration and the Gowin Analyzer Oscilloscope. Gowin GAO configuration is mainly used to insert position information into the design, which is predominantly based on the sampling clock, trigger unit, and trigger expression; Gowin Analyzer Oscilloscope connects software and target hardware through the JTAG interface, and visually displays the data of the sampled signal set by GAO Config File with the waveform.

Before starting GAO configuration, create the GAO config file in the Project Area to open the GAO configuration view, taking standard version as an example, as shown in Figure 5-5.

**Figure 5-5 GAO Config File View**

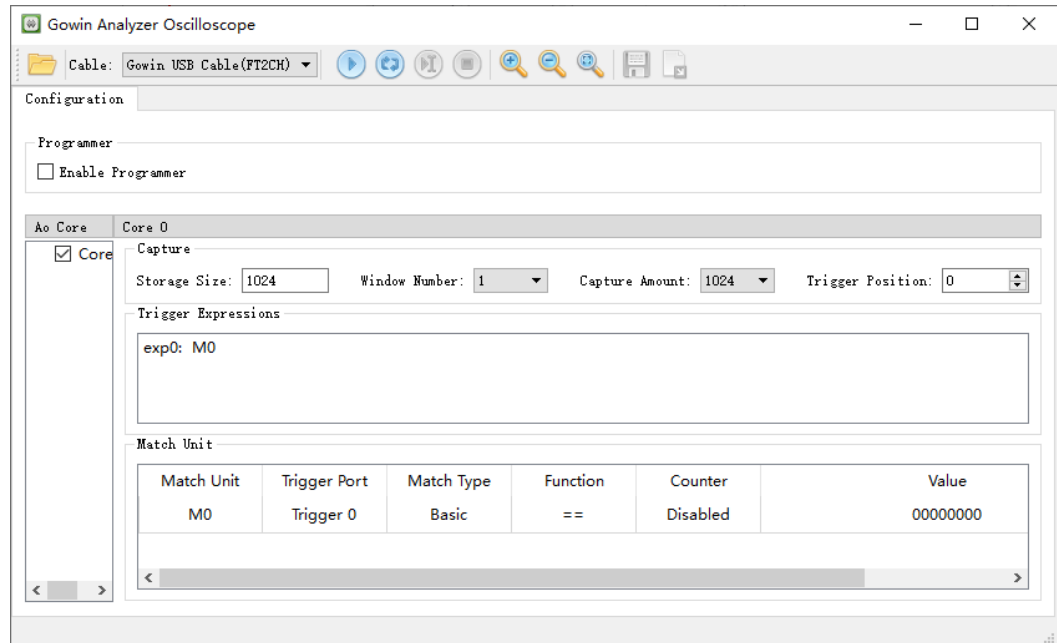


After the configuration file is created, select "Tools > Gowin Analyzer Oscilloscope" from the menu bar to open the Gowin Analyzer Oscilloscope, as shown in Figure 5-6.

**Note!**

For the details, see [SUG114, Gowin Analyzer Oscilloscope User Guide](#).

Figure 5-6 GAO View



## 5.5 Gowin Power Analyzer

Gowin Power Analyzer (GPA) helps to analyze the power consumption of your design and provides many configuration options. You can configure the parameters according to the actual design. GPA automatically estimates the power consumption and generates a power consumption analysis report according to the parameters.

Based on the new configuration file (.gpa), follow the below steps to start the GPA.

1. In the Design area, select "File> New..." to open a "New" dialog box.
2. Select "GPA Config File" and type a Name in the pop-up dialog box.
3. Click "OK", and the new GPA config file will be displayed in the Project Design View.
4. Double click on the file name to open the GPA Config view, as shown in Figure 5-7.

### Note!

For the details, see [SUG282, Gowin Power Analysis User Guide](#).

**Figure 5-7 GPA Config File View**

The screenshot shows the 'GPA Config File View' dialog box with three tabs: 'General Setting', 'Rate Setting', and 'Clock Setting'. The 'General Setting' tab is active. The dialog is organized into several sections:

- Operating Conditions:** Grade: Commercial (dropdown), Process: Typical (dropdown).
- Environment:**
  - Junction Temperature: 25.408°C (spin box)
  - Ambient Temperature: 25.000°C (spin box)
  - Custom Theta JA: 25.000°C/W (spin box)
- Heat Sink:**
  - None (selected), Low Profile, Medium Profile, High Profile, Custom (radio buttons)
  - Air-flow: 0 (dropdown), (LFM)
  - Custom Theta SA: 25.000°C/W (spin box)
- Board Thermal Model:**
  - None (selected), Custom, Typical (radio buttons)
  - Board Temperature: 25.000°C (spin box)
  - Custom Theta JB: 25.000°C/W (spin box)
- Voltage:**
  - VCC: 1.200V (spin box)
  - VCCX: 3.300V (spin box)

## 5.6 Memory Initialization File Editor

The Memory Initialization File is an ASCII file with an .mi suffix. You can generate the corresponding Initialization File according to your design to specify the initial value for the memory of each address. The Memory Initialization File editor can be used to open and edit the existed .mi file.

Each line in the Memory Initialization File correlates with one memory. The number of lines is the number of memories and also the memory address depth. The number of columns represents each memory bit; that is, the memory data width. The address decreases from top to bottom with the most significant bit first for each line.

Gowin memory initialization file is based on .mi file. For the details, see [UG285, Gowin BSRAM & SSRAM User Guide](#). The steps are as follows:

1. In the Design area, select "File> New..." to open a "New" dialog box.
2. Select "Memory Initialization File", as shown in Figure 5-8. Click "OK" and type the initialization file name in the pop-up "New File" dialog box, and then click "OK". The Initialization File Configuration View is as shown in Figure 5-9.

3. Start the file initialization view as shown in Figure 5-10. Type the initial value on the left side and configure the initialization file format and depth/width and view on the right side.
4. On the right side, configure the depth and width for the initialization file and the format for the address and initial values in the left table.
  - The depth and width values should be same as the Block Memory or Shadow Memory address depth and data width set in the IP Core Generator. If the address depth and data width in the initialization file are greater than the values set in the IP Core Generator, the IP Core Generator will prompt an error message. If the depth and width values are less than the address depth and data width set in the IP Core Generator, the value of the unassigned address will be initialized to 0 by default. Click "Update" after configuration.
  - The display format of the addresses and values on the left in the table can be configured as binary, hexadecimal, and address-hexadecimal, etc.
5. Type the initial value and set the view in the left table.
  - Right-click the table header to configure the number of columns, which can be configured as 1, 8, or 16, as shown in Figure 5-11.
  - The initial values in the table can be entered manually by double-clicking a cell or configured by right-clicking. Right-click the target cell and select "Fill with 0", which sets all bits of the initial value to 0; "Fill with 1", which sets all bits of the initial value to 1; or "Custom Fill", which allows the user to enter values as required, as shown in Figure 5-12. Selecting "Custom Fill" enables batch filling of repeated sequence or incrementing/decrementing data, as shown in Figure 5-13.
6. Save the file.

Figure 5-8 New Dialog Box

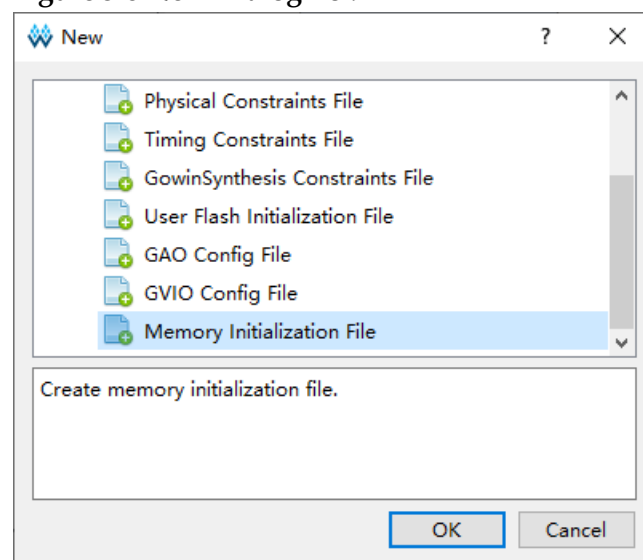


Figure 5-9 New File Dialog Box

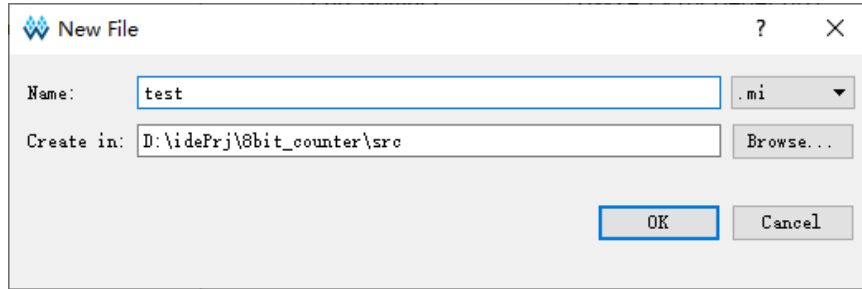


Figure 5-10 Initialization File Configuration View

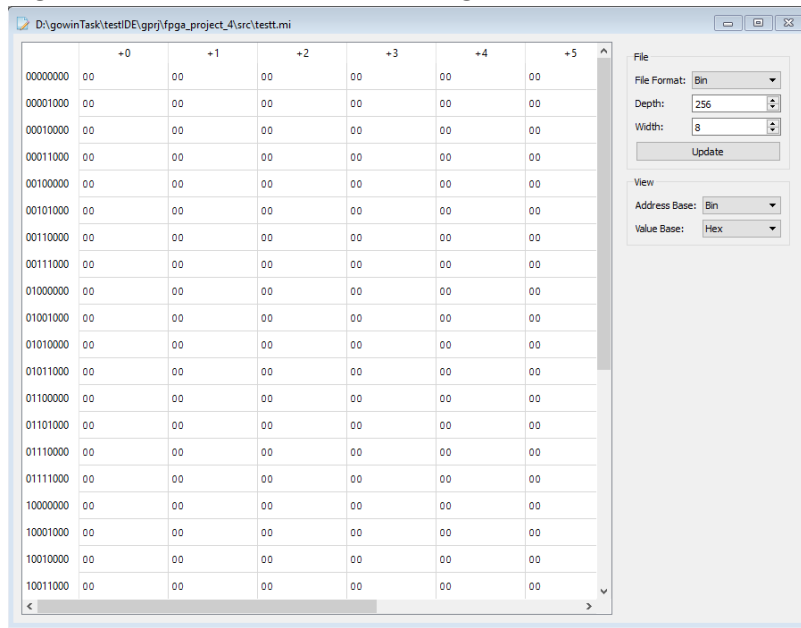


Figure 5-11 Column Setting

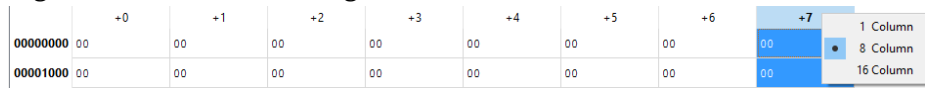
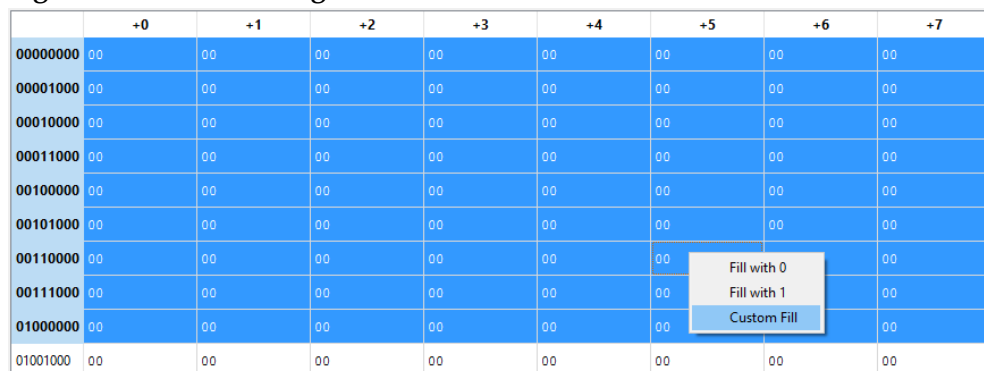
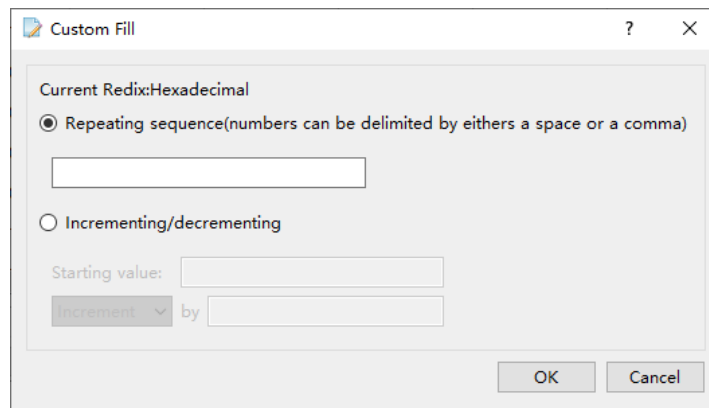


Figure 5-12 Batch Setting



**Figure 5-13 Batch Filling of Repeated Sequence or Incrementing/Decrementing Data**



## 5.7 User Flash Initialization File Editor

User Flash Initialization file is an ASCII file with an .fi suffix. You can generate the corresponding Initialization File according to your design to specify the initial value for the User Flash of each address. The User Flash Initialization File editor can be used to open and edit the existed .fi file.

The name of User Flash initialization file is \*.fi(file\_name.fi). Each line in the Memory Initialization File correlates with one memory. The number of lines is the number of memories that needs to be initialized. The contents in the header bracket represent the ordinate address and the abscissa address respectively, separated by a semicolon. The contents after the brackets in each line represent the data initialized by the memory, and the data supports binary and hexadecimal, MSB first. The following are examples of the .fi file format.

### 5.7.1 Bin File

Bin file is a text file that consists of the 0 and 1.

```
//Copyright (C)2014-2024 Gowin Semiconductor Corporation.
```

```
//All rights reserved.
```

```
//File Title: User Flash Initialization File
```

```
//Tool Version: V1.9.10(64-bit)
```

```
//Part Number: GW1N-LV4PG256C6/I5
```

```
//Device-package: GW1N-4-PBGA256
```

```
//Device Version: D
```

```
//Flash Type: FLASH256K
```

```
//File Format: Bin
```

```
//Created Time: 2024-06-28 14:31:12
```

```
[0:0] 00000000000100000001000100010000
```

```
[1:1] 00000000000100010001000000000001
```

## 5.7.2 Hex File

The Hex file is similar to the Bin file. It consists of hexadecimal numbers 0~F.

```
//Copyright (C)2014-2024 Gowin Semiconductor Corporation.  
//All rights reserved.  
//File Title: User Flash Initialization File  
//Tool Version: V1.9.10(64-bit)  
//Part Number: GW1N-LV4PG256C6/I5  
//Device-package: GW1N-4-PBGA256  
//Device Version: D  
//Flash Type: FLASH256K  
//File Format: Hex  
//Created Time: 2024-06-28 14:41:24  
[0:0] 00101110  
[1:1] 00111001
```

Based on the new configuration file (. fi), and you can follow the below steps to use the initialization file editor.

1. In the Design area, select "File> New..." to open a "New" dialog box.
2. Select "User Flash Initialization File", as shown in Figure 5-14. Click "OK" and type the initialization file name in the pop-up "New File" dialog box, and then click "OK", as shown in Figure 5-15. The devices supported by User Flash Initialization File Editor are the same as the devices supported by User Flash Primitives. If the device you selected does not support User Flash, "Current device do not support flash" will pop up at the bottom of "New File" Dialog box after you click "OK".

Figure 5-14 New Dialog Box

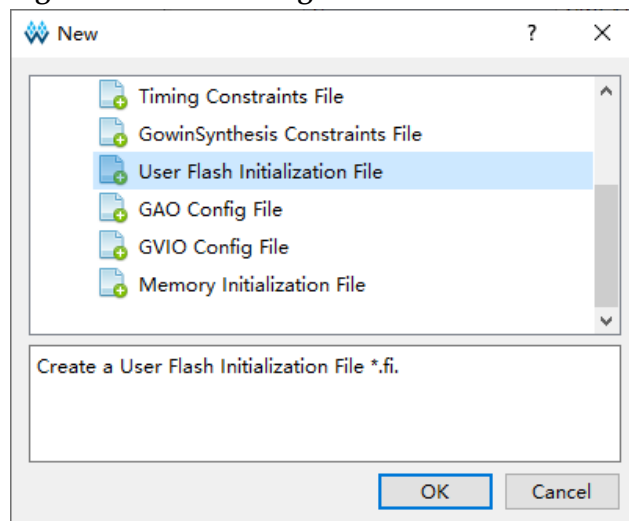
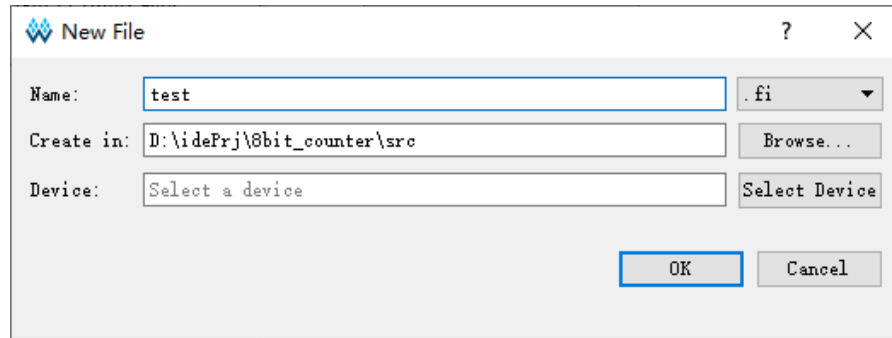
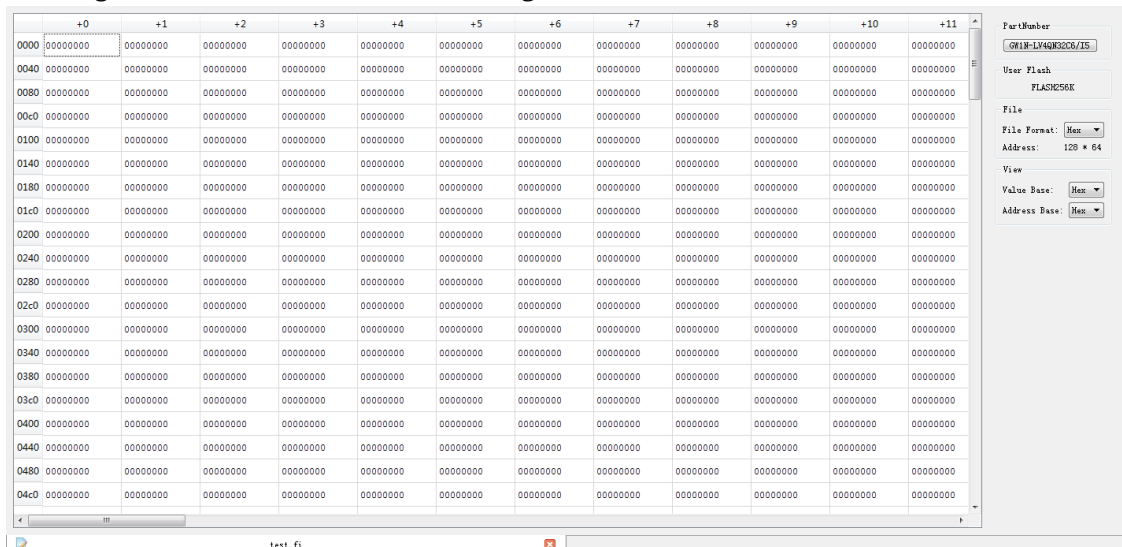


Figure 5-15 New File Dialog Box



3. Start the file initialization view as shown in Figure 5-16. Enter the initial value on the left side and configure the initialization file format and view on the right side; Part Number and User Flash are also displayed on the right.

Figure 5-16 Initialization File Configuration View



4. On the right side, configure Part Number, file format, address and value.
  - Click "Part Number", then "Select Device" dialog box will pop up; you can select the other part number.
  - The format of address and value can be configured as binary, octal, decimal, hexadecimal, etc.

5. Enter the initial values in the table on the left side of the configuration window. In addition, the table view format can be configured in the left table. The initial values in the table can be entered manually by double-clicking a cell or configured by right-clicking. Right-click the target cell and select "Fill with 0", which sets all bits of the initial value to 0; "Fill with 1", which sets all bits of the initial value to 1; or "Fill Custom", which allows the user to enter values as required, as shown in Figure 5-17. Selecting "Custom Fill" enables batch filling of repeated sequence or incrementing/decrementing data, as shown in Figure 5-13.

Figure 5-17 Batch Setting

	+0	+1	+2	+3	+4	+5	+6	+7	+8	+9	+10	+11
0000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
0040	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
0080	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
00c0	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
0100	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
0140	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
0180	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
01c0	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000

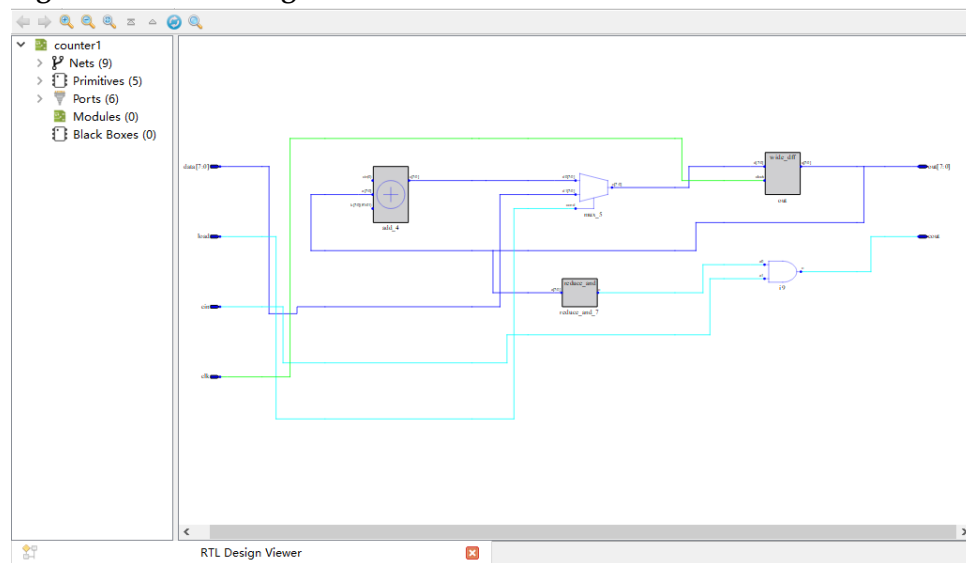
6. Save the file.

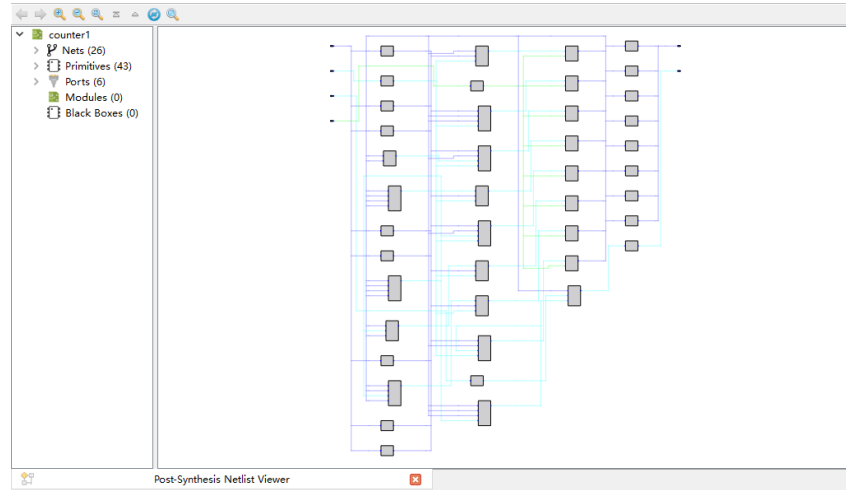
## 5.8 Schematic Viewer










You can understand the design logic by Schematic Viewer, which is helpful to the later modification. Schematic Viewer includes RTL Design Viewer, Post-Synthesis Netlist Viewer. Schematic Viewer uses common component symbols to build circuits, including adders, multipliers, registers, and gates, non-gates, and inverters, etc.

You can click "Tools > Schematic Viewer > RTL Design Viewer/ Post-Synthesis Netlist Viewer to open GUI, as shown in Figure 5-18 and Figure 5-19.

Figure 5-18 RTL Design Viewer



**Figure 5-19 Post-Synthesis Netlist Viewer**

Schematic Viewer displays backward "", forward "", zoom in "", zoom out "", zoom "", top view "", upper level view "", reload "", and search "". The design hierarchy is displayed on the left side, including Modules, Ports, Nets, Primitives, and Black Boxes.

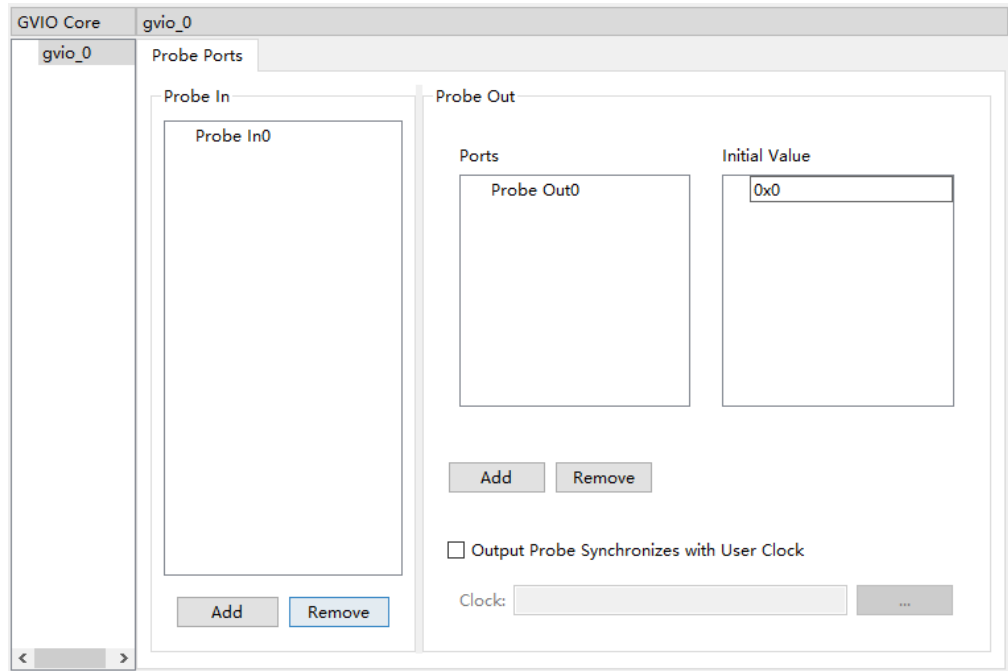
**Note!**

For the details, you can see [SUG755, Gowin HDL Schematic Viewer User Guide](#).

## 5.9 Virtual Input/Output Debugging Tool

Gowin Virtual Input/Output Core (GVIO) is a customizable core that can monitor and drive internal FPGA signals in real time. Its input ports are used to monitor FPGA signals, functioning like virtual LEDs, while its output ports are used to drive FPGA signals, functioning like virtual switches.

Before launching the GVIO configuration file window, you need to create a new GVIO configuration file in the project area and then open the configuration file window, as shown in Figure 5-20.

**Figure 5-20 GVIO Configuration File Window****Note!**

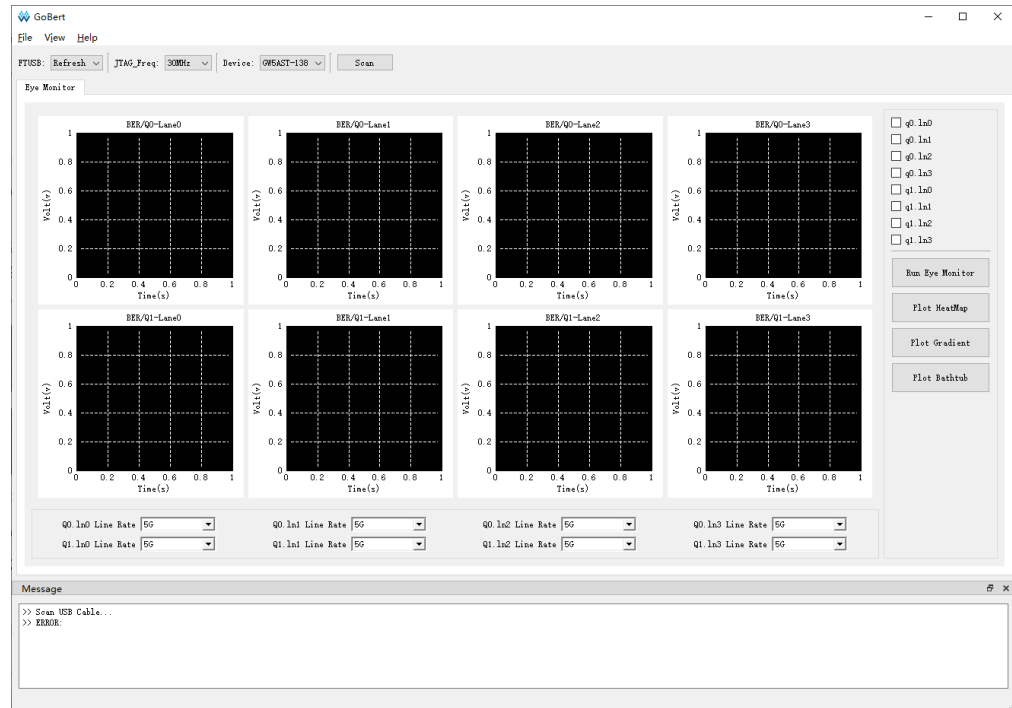
For configuration and usage instructions of the Virtual Input/Output Core, see [SUG1189, Gowin Virtual Input Output User Guide](#).

## 5.10 Eye Diagram Analysis Tool GoBert

GoBert is a tool designed in-house by Gowin Semiconductor for analyzing the eye diagrams of SerDes RX signals. It helps users evaluate SerDes reception quality, thereby enhancing the performance and reliability of their designs. When using GoBert to test signal reception quality, users need to load their functional application onto the development board. Once the functional application is operating normally, the eye diagram testing can be initiated.

Click the "Tools" option on the menu bar or the "👁️" button on the toolbar of Gowin Software to launch the GoBert window, as shown in Figure 5-21.

Figure 5-21 GoBert Window



**Note!**

For the configuration and usage of the eye diagram analysis tool GoBert, you can see [SUG1198, Gowin GoBert User Guide](#).

# 6 Output Files

In the process of FPGA design, in addition to bitstream file, Gowin Software can also generate multiple reports for reference by different operating parameters. They are synthesis, place & route, ports, timing and power reports. In addition, you can right-click Place & Route to modify the configuration to generate pins constraints, timing simulation files, etc.

## 6.1 Synthesis Report

GowinSynthesis will generate synthesis reports and netlist files after synthesis.

The report named \*\_syn.rpt.html is generated, including Synthesis Message, Synthesis Details, Resource, and Timing, as shown in Figure 6-1.

Figure 6-1 GowinSynthesis Report

Top Level Module	counter1
Synthesis Process	<p>Running parser: CPU time = 0h 0m 0.109s, Elapsed time = 0h 0m 0.121s, Peak memory usage = 74.734MB</p> <p>Running netlist conversion: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 0MB</p> <p>Running device independent optimization: Optimizing Phase 0: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Optimizing Phase 1: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Optimizing Phase 2: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB</p> <p>Running inference: Inferring Phase 0: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Inferring Phase 1: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Inferring Phase 2: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Inferring Phase 3: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB</p> <p>Running technical mapping: Tech-Mapping Phase 0: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Tech-Mapping Phase 1: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Tech-Mapping Phase 2: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Tech-Mapping Phase 3: CPU time = 0h 0m 0.046s, Elapsed time = 0h 0m 0.095s, Peak memory usage = 87.988MB Tech-Mapping Phase 4: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 87.988MB</p>

The details are as follows.

- Synthesis Message: Includes design file, constraint file, software version, device, report creation time and legal statement, etc.

- Synthesis Details: Includes top module of the design file, the synthesis running time and CPU running time, as well as the memory peak at each stage, and total CPU running time as well as memory peak.
- Resource: Includes resource statistics and device utilization statistics.
- Timing: Includes Clock Summary, Max Frequency Summary, Detail Timing Paths Informations.

## 6.2 Place & Route Report

The Place & Route Report describes the resource, memory consumption, time consumption, etc. occupied by the user design, with the suffix .rpt.html, and you can check \*.rpt.html file for further details.

Double-click "Place & Route Report" in the Process View to open the Place & Route report, as shown in Figure 6-2.

Figure 6-2 Place & Route Report

The screenshot displays the Place & Route Report interface. On the left, a navigation pane lists sections: PnR Messages, PnR Details, Resource, Resource Usage Summary, I/O Bank Usage Summary, Global Clock Usage Summary, Global Clock Signals, Pinout by Port Name, and All Package Pins. The main content area is divided into two sections: PnR Details and Resource.

**PnR Details**

Place & Route Process	Running placement: Placement Phase 0: CPU time = 0h 0m 0.004s, Elapsed time = 0h Placement Phase 1: CPU time = 0h 0m 0.263s, Elapsed time = 0h Placement Phase 2: CPU time = 0h 0m 0.002s, Elapsed time = 0h Placement Phase 3: CPU time = 0h 0m 0.8s, Elapsed time = 0h 0r Total Placement: CPU time = 0h 0m 1s, Elapsed time = 0h 0m 1s Running routing: Routing Phase 0: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s Routing Phase 1: CPU time = 0h 0m 0.189s, Elapsed time = 0h 0m Routing Phase 2: CPU time = 0h 0m 0.082s, Elapsed time = 0h 0m Total Routing: CPU time = 0h 0m 0.271s, Elapsed time = 0h 0m 0. Generate output files: CPU time = 0h 0m 2s, Elapsed time = 0h 0m 2s
Total Time and Memory Usage	CPU time = 0h 0m 3s, Elapsed time = 0h 0m 3s, Peak memory usag

**Resource**

**Resource Usage Summary:**

Resource	Usage	Utilization
Logic	10/20736	1%
--LUT,ALU,ROM16	10(3 LUT, 7 ALU, 0 ROM16)	-
--SSRAM(RAM16)	0	-
Register	8/16683	1%
--Logic Register as Latch	0/15552	0%

The details are as follows.

- PnR Messages: Includes report name, path and name of design, physical constraints file, timing constraints file, software version, device information, report creation time and declaration.
- PnR Details:
  - The time used in each stage of place and the total time of place, including the time of GAO place if there is GAO in the project.
  - The time used in each stage of route and the total time of route, including the time of GAO route if there is GAO in the project.
  - The time used to generate the output file.
- Resource:
  - Resource Usage Summary: Device resources utilization in user design.

- I/O BANK0 Usage Summary: I/O BANK0 in user design
- Global Clock Usage Summary: Global clock used
- Global Clock Signals: Clock signals used in the user design
- Pinout by Port Name: Pinout in the user design
- All Package Pins: Details of all the pins in the device package

If the project has a GAO, it also includes the GAO Resource Usage Summary.

## 6.3 Ports and Pins Report

The Ports and Pins Report is the ports and pins files after placement. It includes ports type, attributes, and locations, etc. The generated file is saved with .pin.html suffix, and you can view .html file for details.

Double-click "Ports & Pins Report" in the Process View to open the report, as shown in Figure 6-3.

Figure 6-3 Ports & Pins Report

The screenshot shows a window titled "Pin Details" with a left-hand navigation pane containing a tree view with the following items:

- Pin Messages
- Pin Details
  - Pinout by Port Name
  - All Package Pins

The main content area displays two tables:

**Pinout by Port Name:**

Port Name	Diff Pair	Loc./Bank	Constraint	Dir.	Site	IO Type	Drive	Pull Mode	PCI
clk		L1/7	N	in	IOL25[A]	LVC MOS18	OFF	DOWN	OFF
cout[0]		M2/7	N	out	IOL25[B]	LVC MOS18	8	NONE	OFF
cout[1]		F6/8	N	out	IOL3[A]	LVC MOS18	8	NONE	OFF
cout[2]		G7/8	N	out	IOL3[B]	LVC MOS18	8	NONE	OFF
cout[3]		D3/8	N	out	IOL2[A]	LVC MOS18	8	NONE	OFF
cout[4]		D4/8	N	out	IOL2[B]	LVC MOS18	8	NONE	OFF
cout[5]		A2/0	N	out	IOT2[B]	LVC MOS18	8	NONE	OFF
cout[6]		E6/0	N	out	IOT3[A]	LVC MOS18	8	NONE	OFF
cout[7]		F5/8	N	out	IOL4[B]	LVC MOS18	8	NONE	OFF

**All Package Pins:**

Loc./Bank	Signal	Dir.	Site	IO Type	Drive	Pull Mode	PCI Clamp	Hysteresis	Open
B1/0	-	out	IOT2[A]	LVC MOS18	8	NONE	OFF	OFF	ON
A2/0	cout[5]	out	IOT2[B]	LVC MOS18	8	NONE	OFF	OFF	OFF
E6/0	cout[6]	out	IOT3[A]	LVC MOS18	8	NONE	OFF	OFF	OFF
F7/0	-	out	IOT3[B]	LVC MOS18	8	NONE	OFF	OFF	ON
B2/0	-	out	IOT4[A]	LVC MOS18	8	NONE	OFF	OFF	ON
A3/0	-	out	IOT4[B]	LVC MOS18	8	NONE	OFF	OFF	ON

The details are as follows:

- Pin Messages: Includes report name, path and name of design, physical constraints file, timing constraints file, software version, device information, report creation time and declaration.
- Pin Details:
  - Pinout by Port Name: Pinout in the user design
  - All Package Pins: Details of all the pins in the device package

**Note!**

For devices other than GW1N-1P5/GW1N-2/GW1NR-2 and GW2AN-18X/GW2AN-9X, if no Bank  $V_{CCIO}$  constraint is added, the voltage values corresponding to some single-ended input port IO Type may not match the value of Bank  $V_{CCIO}$  in the ports report, which is normal. For example, the IO Type in the report is LVCMOS18, which corresponds to a voltage value of 1.8, but the Bank  $V_{CCIO}$  is 1.2

## 6.4 Timing Report

The timing report performs a thorough analysis of the timing model in the circuit netlist, calculates the timing path delays in the circuit, and determines whether they are met the requirements. The Timing report includes setup check, holdup check, restoring and removal time check, Min. clock pulse check, max. fanout path, Place & Route congestion report, etc. by default, and provides the Max. frequency report.

Double-click "Timing Analysis Report" in the Process View to open the timing analysis report for the project, as shown in Figure 6-4.

### Note!

For the details, see [SUG940, Gowin Design Timing Constraints User Guide](#).

Figure 6-4 Timing Report

The screenshot shows the Timing Analysis Report interface. On the left is a sidebar with a tree view of report sections. The main content area is titled "Timing Summaries" and contains three summary tables.

**Timing Messages**

- ▶ Timing Summaries
  - STA Tool Run Summary
  - Clock Summary
  - Max Frequency Summary
  - Total Negative Slack Summary
- ▶ Timing Details
  - ▶ Path Slacks Table
    - Setup Paths Table
    - Hold Paths Table
    - Recovery Paths Table
    - Removal Paths Table
  - Minimum Pulse Width Table
  - ▶ Timing Report By Analysis Type
    - Setup Analysis Report
    - Hold Analysis Report
    - Recovery Analysis Report
    - Removal Analysis Report
    - Minimum Pulse Width Report

## 6.5 Power Analysis Report

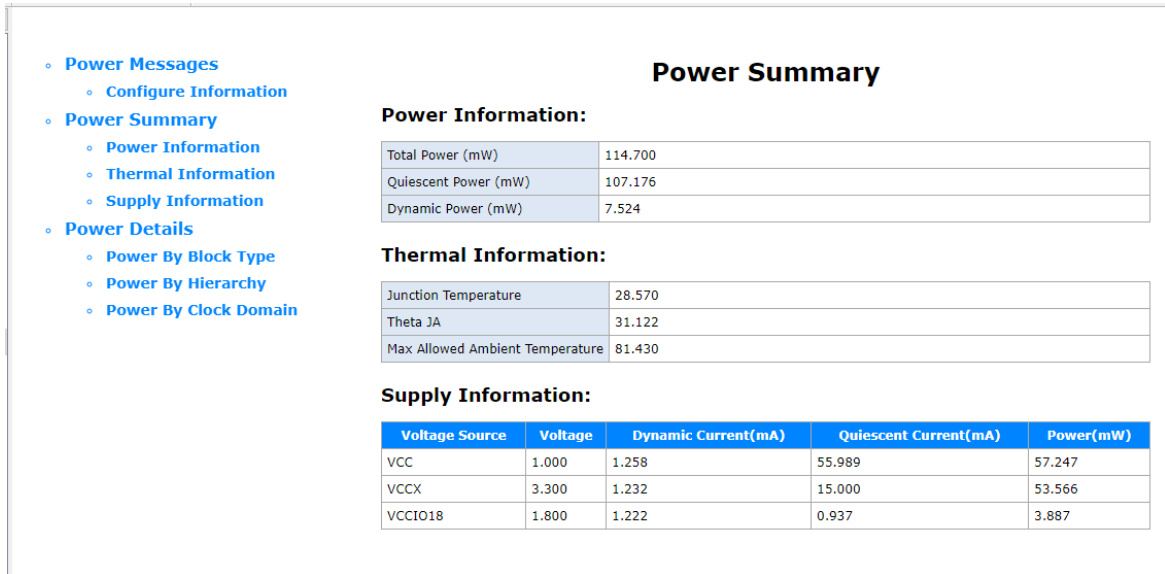
The Power Analysis Report mainly includes the power consumption estimation for your design. It is designed to help you evaluate the basic power consumption of your design.

Double-click "Power Analysis Report" in the Process View to open the analysis report, as shown in Figure 6-5.

### Note!

For the details, see [SUG282, Gowin Power Analyzer User Guide](#)

Figure 6-5 Power Analysis Report



# 7 Simulation Files

Gowin Software provides input files for simulation. Simulation includes functional simulation and timing simulation. Functional simulation, also known as pre simulation, is to verify whether the circuit meets the design requirements, and it is characterized by not considering the circuit gate delay and net delay.

Timing simulation, also known as post simulation or post PnR simulation, is the process of verifying whether a circuit can meet the design under certain timing conditions and whether there are timing violations, taking into account the effects of the circuit path delay and gate delay after the circuit has been mapped to a specific process environment.

## 7.1 Functional Simulation Files

Functional simulation includes functional simulation of the user RTL design before synthesis and functional simulation of the synthesized logic netlist. The required simulation files are described below using a design written in Verilog as an example.

For RTL design functional simulation, the required files include the user RTL design files before synthesis, the stimulus file (testbench) `*tb.v`, and the functional simulation library file `prim_sim.v`. If the RTL design contains soft IP cores, since soft IP cores are provided in encrypted form, the `.vo/.vho` files generated by the soft IP cores must be used for functional simulation. These `.vo / .vho` files are generated in the soft IP directory `src\ipName` under the `src` directory of the current project.

For post-synthesis netlist functional simulation, the required files include the synthesized netlist file (`*.vg`), the stimulus file (testbench) `*tb.v`, and the functional simulation library file `prim_sim.v`. If the `.vg` file contains encrypted content, the configuration option "Generate Post-PNR Verilog Simulation Model File" on the "Configuration > Place & Route > General" page must be enabled to generate a plaintext `.vo` file, which is then used to replace the `.vg` file for functional simulation.

The installation directories of the primitive simulation library files are listed in the table below.

**Table 7-1 Installation Directories of Primitive Simulation Library Files**

Supported Devices	Simulation Library File Name	Simulation Library Directory	File Description
Arora V Devices	prim_sim.v	IDE/simlib/gw5a	Verilog-based functional simulation library file
	prim_sim.vhd	IDE/simlib/gw5a	VHDL-based functional simulation library file
	prim_syn.vhd	IDE/simlib/gw5a	
	prim_tsim.v	IDE/simlib/gw5a	Verilog-based timing simulation library file
GW3A-20	prim_sim.v	IDE/simlib/gw3a	Verilog-based functional simulation library file
	prim_sim.vhd	IDE/simlib/gw3a	VHDL-based functional simulation library file
	prim_syn.vhd	IDE/simlib/gw3a	
GW1AN-5, GW1AN-3	prim_sim.v	IDE/simlib/gw1a	Verilog-based functional simulation library file
	prim_sim.vhd	IDE/simlib/gw1a	VHDL-based functional simulation library file
	prim_syn.vhd	IDE/simlib/gw1a	
GW1A(N)-1S, GW1A(N)-1	prim_sim_a.v	IDE/simlib/gw1a	Verilog-based functional simulation library file
	prim_sim_a.vhd	IDE/simlib/gw1a	VHDL-based functional simulation library file
	prim_syn_a.vhd	IDE/simlib/gw1a	
GW1N Family Devices	prim_sim.v	IDE/simlib/gw1n	Verilog-based functional simulation library file
	prim_sim.vhd	IDE/simlib/gw1n	VHDL-based functional simulation library file
	prim_syn.vhd	IDE/simlib/gw1n	
	prim_tsim.v	IDE/simlib/gw1n	Verilog-based timing simulation library file
GW2A Family Devices	prim_sim.v	IDE/simlib/gw2a	Verilog-based functional simulation library file
	prim_sim.vhd	IDE/simlib/gw2a	VHDL-based functional simulation library file
	prim_syn.vhd	IDE/simlib/gw2a	
	prim_tsim.v	IDE/simlib/gw2a	Verilog-based timing simulation library file

## 7.2 Timing Simulation Files

Taking timing simulation of a design described in Verilog as an example, the files required for timing simulation include: the Verilog simulation logic netlist file (\*.vo) generated by the software, the corresponding delay file (\*.sdf), the corresponding stimulus file (\*.tb.v), and the timing simulation library file prim\_tsim.v.

- The .vo file is generated by enabling the "Generate Post-PNR Verilog Simulation Model File" option on the "Configuration > Place & Route > General" page and then running Place & Route. The file is located in the impl/pnr/ directory under the project path.

- The .sdf file is generated by enabling the "Generate SDF File" option on the "Configuration > Place & Route > General" page and then running Place & Route. The file is also located in the impl/pnr/ directory under the project path.

For detailed configuration settings, refer to the General in section 4.3.3 Edit Project Configuration.

**Note!**

The time precision of the delay data in the SDF file is 1 ps.

# 8 Appendix

## 8.1 File Description

Gowin Software supports adding physical constraints, timing constraints, and other files during the project design, and a variety of execution files are generated in the overall design; this section will introduce these files supported by Gowin Software as shown below.

**Table 8-1 Source Files**

File Type	Definition	Function
.gsc	Synthesis constraints file	Constraint files for the GowinSynthesis
.ipc	IP configuration file	IP Core Generator can load an .ipc file to recreate the IP after modifying the configuration
.cst	Physical constraints file	Used to add physical constraints to the design
.sdc	Timing constraints file	Used to add timing constraints to the design
.fi	User Flash initialization file	Initialization assignment to User Flash; you can select to load it when downloading the bitstream through the Programmer.
.rao	RTL-level GAO configuration file	Capture the RTL signal before synthesis
.gao	Post-synthesis GAO configuration file	Capture the Netlist signal after synthesis
.gvio	Virtual Input/Output Configuration File	Used to real-time monitor and drive internal FPGA signals
.gpa	Power analysis configuration file	Used to analyze the power analysis of the design
.mi	Memory initialization file	Initialization assignment of memory; you can use this initialization file when generating the memory through IP Core Generator.
.v	Verilog source file	Verilog description file containing circuit structure and function
.sv	System Verilog source file	System Verilog description file containing circuit structure and function
.vhd	VHDL source file	VHDL description file containing circuit

File Type	Definition	Function
		structure and function

**Table 8-2 Execution Files**

File Type	Definition	Function
.vg	Post-synthesis netlist file	The post-synthesis netlist file using GowinSynthesis
_syn.rpt.html	Synthesis report file	Used to view information such as resource utilization and timing analysis after synthesis
.fs	Bitstream file	Used by Gowin Programmer to download
.bin	Bitstream files in bin format	Used by Gowin Programmer to download
.ekey	key file	Used to decrypt the encrypted BitStream files during download using Gowin Programmer
.vo	Timing simulation model file in verilog post PnR	Used for Verilog model file with the flatten structure for timing simulation
.vho	Timing simulation model file in vhdl post PnR	Used for VHDL model file with the flatten structure for timing simulation
.sdf	Standard delay format file	Used for netlist timing simulation after PnR
.ibs	Input/output buffer information specified files	-
.tr	Timing report in text format	-
.rpt.txt	PnR report in text format	-
.rpt.html	PnR report in html format	-
.tr.html	Timing analysis report in html format	-
.pin.html	Port attributes report in html format	-
.power.html	Power analysis report in html format	-
.p	Incremental placement file	Used for incremental placement
.pr	Incremental placement and routing file	Used for incremental placement and routing

## 8.2 File and Folder Naming Rules

Gowin folders and files naming rules: The names cannot contain ? " / \ < > \* | : characters; folder names can not contain spaces, file names can contain spaces but spaces cannot appear at the beginning and end of the name.

For the file path filling in the dialog box of each component of Gowin

Software, it will be judged according to the above rules, and a pop-up window will be displayed if it does not comply with the rules.

## **8.3 Security Declaration**

During installation and use, Gowin Software does not collect any information from users or access network data ports in the background; all data and information are kept locally, and no automatic updates are made to the software.

