GW5AST series of FPGA Products

Package & Pinout User Guide

UG1102-1.0.8E, 08/15/2025

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Revision History

Date	Version	Description
04/20/2023	1.0E	Initial version published.
07/06/2023	1.0.1E	The info. of PG676A package for GW5AST-138 devices added.
09/12/2023	1.0.2E	The info. of UG324 package for GW5AST-138 devices added.
09/22/2023	1.0.3E	“Figure 3-3 View of GW5AST-138 PG676A Pins Distribution (Top View)” in “Chapter 3 View of Pin Distribution” updated.
02/02/2024	1.0.4E	● The quantity of GW5AST-138 pins updated. ● The note of “Table 2-3 Quantity of GW5AST-138 Pins” added.
07/05/2024	1.0.5E	The names of voltage pins updated.
07/19/2024	1.0.6E	● The information of UG324 package for GW5AST-138 devices removed. ● The ddd value in “Figure 4-6 Recommended PCB Layout PG676A” updated.
03/14/2025	1.0.7E	The names of power supply pins updated.
08/15/2025	1.0.8E	The “A” dimension of the package line for PG676A package updated.

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1 About This Guide

1.1 Purpose

This manual introduces Gowin GW5AST series of FPGA products package and provides pin definitions, lists of pin numbers, pin distribution views, and package diagrams.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- DS1239, GW5AST series of FPGA Products Data Sheet
- UG986, GW5AST-138 Pinout

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FPG	FCPBGA Package
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable Input/Output
FPG	PBGA Package
UG	UBGA Package

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

Gowin GW5AST series of FPGA products are the 5 series products of Arora family with abundant internal resources, a new-architecture and high-performance DSP supporting AI operations, high-speed LVDS interfaces, and abundant BSRAM resources. At the same time, GW5AST series integrate self-developed DDR3, 12.5Gbps SerDes supporting multiple protocols, and provide a variety of packages. They are suitable for applications such as low power, high performance and compatibility design.

Gowin provides a new generation of FPGA hardware development environment that supports GW5AST series of products, capable of fulfilling one-stop work such as FPGA synthesis, placement & routing, bitstream generation and download, etc.

2.1 PB-Free Package

GW5AST series of FPGA products are PB free in line with the EU RoHS environmental directives. The substances used in the GW5AST series of FPGA products are in full compliance with the IPC-1752 standards.

2.2 Package and Max. User I/O Information

Table 2-1 Package, Max. User I/O Information, and LVDS Pairs

Package	Pitch (mm)	Size (mm)	E-pad Size (mm)	GW5AST-138
FPG676A (Flip Chip)	1.0	27 x 27	-	312 (150)
PG484A	1.0	23 x 23	-	287 (143)
PG676A	1.0	27 x 27	-	312 (150)

Note!

For package type abbreviations employed in this manual, see 1.3 Terminology and Abbreviations.

2.3 Power Pins

Table 2-2 GW5AST Power Pins

VCC	VCCIO0	VCCIO1	VCCIO2
VCCIO3	VCCIO4	VCCIO5	VCCIO6
VCCIO7	VCCIO10	VCCX	VSS
VDDAQ0	VDDAQ1	VDDHAQ0	VDDHAQ1
VCCLDO	VDDAM	VDDDM	VDDXM
VDDTQ0	VDDTQ1	-	-

2.4 Pin Quantity

2.4.1 Quantity of GW5AST-138 Pins

Table 2-3 Quantity of GW5AST-138 Pins

Pin Type		GW5AST-138		
		FPG676A (Flip Chip)	PG484A	PG676A
Single-ended IO/Differential Pair/LVDS [1]	BANK0 (Q0)	0/0/0	0/0/0	0/0/0
	BANK1 (Q1)	0/0/0	0/0/0	0/0/0
	BANK2	50/24/24	50/24/24	50/24/24
	BANK3	50/24/24	50/24/24	50/24/24
	BANK4	50/24/24	50/24/24	50/24/24
	BANK5	50/24/24	35/17/17	50/24/24
	BANK6	50/24/24	50/24/24	50/24/24
	BANK7	50/24/24	50/24/24	50/24/24
	BANK10	12/6/6	12/6/6	12/6/6
Max. User I/O[2]		311	296	311
Differential Pair		150	143	150
True LVDS Output		150	143	150
VCCIO0		0	0	0
VCCIO1		0	0	0
VCCIO2		6	6	6
VCCIO3		6	6	6
VCCIO4		6	6	6
VCCIO5		6	5	6
VCCIO6		6	6	6
VCCIO7		6	6	6
VCCIO10		2	2	2
VCCX		3	3	3
VCC		13	14	13
VCCLDO		6	6	6

Pin Type	GW5AST-138		
	FPG676A (Flip Chip)	PG484A	PG676A
VDDHAQ1	1	1	0
VDDHAQ0	1	1	0
VDDHAQ0_VDDHAQ1	0	0	2
VDDAQ1_VDDDQ1	3	0	0
VDDAQ0_VDDDQ0	3	0	0
VDDAQ0	0	3	3
VDDAQ1	0	0	3
VDDTQ1	2	0	2
VDDTQ0	2	2	2
VDDAM	0	0	1
VDDDM	0	0	1
VDDAM	0	0	1
VDDDM	0	0	1
VDDAM_VDDDM	4	0	0
VDDXM	1	0	1
VSS	120	88	120
MODE0	1	1	1
MODE1	1	1	1
MODE2	1	1	1
NC	102	8	103

Note!

- [1] Single-ended/Differential I/O quantity includes CLK pins and download pins.
- [2] RECONFIG_N pin cannot be multiplexed as I/O.

2.5 I/O BANK Introduction

GW5AST-138 has six GPIO Banks (Bank2~7), two SerDes Banks and a Bank for configuration (Bank 10). Bank 10 can also be used as an I/O Bank. See *DS1239, GW5AST series of FPGA Products Data Sheet > 2.3 Input/Output Blocks* for details.

This manual provides the pin distribution view of GW5AST series of FPGA products. For details, please refer to Chapter 3 View of Pin Distribution. The I/O Banks that form GW5AST series of FPGA products are marked with different colors.

Various symbols and colors are used for the user I/O, power, and ground. The various symbols and colors used for the various pins are defined as follows:

- "  " denotes the I/O in BANK2.
- "  " denotes the I/O in BANK3.

- "  " denotes the I/O in BANK4.
- "  " denotes the I/O in BANK5.
- "  " denotes the I/O in BANK6.
- "  " denotes the I/O in BANK7.
- "  " denotes the I/O in BANK10.
- "  " denotes the DIO in SerDes Bank Q0, SerDes Bank Q1, MIPI, and ADC.
- "  " denotes VCC, VCCX, and VCCIO.
- "  " denotes VSS.
- "  " denotes NC.

3 View of Pin Distribution

3.1 View of GW5AST-138 Pins Distribution

3.1.1 View of FPG676A (Flip Chip) Pins Distribution

Figure 3-1 View of GW5AST-138 FPG676A (Flip Chip) Pins Distribution (Top View)

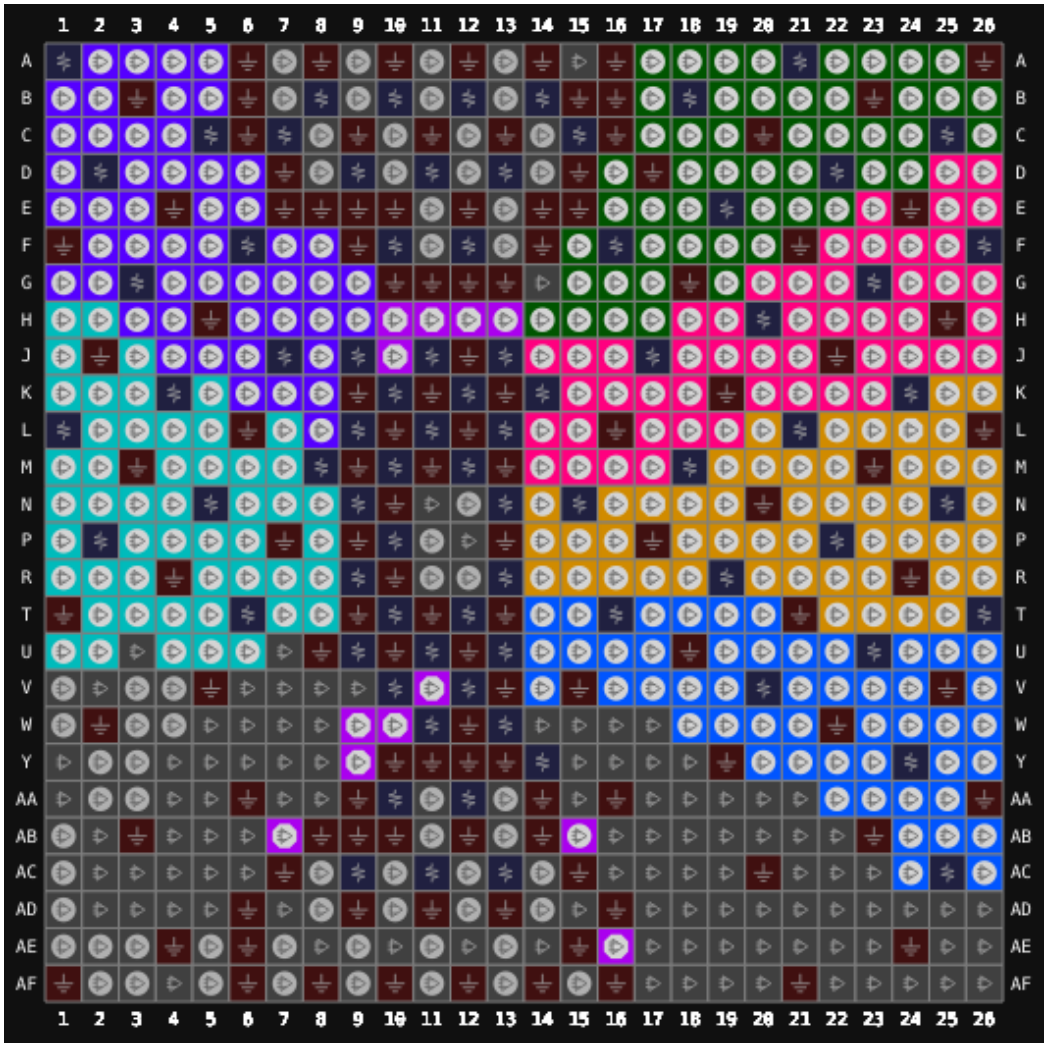


Table 3-1 Other Pins in GW5AST-138 FPG676A (Flip Chip)

VCCIO2	V20,U23,T26,Y24,AC25,T16
VCCIO3	R19,K24,N25,N15,P22,L21
VCCIO4	F26,M18,J17,H20,G23,K14
VCCIO5	C25,D22,F16,A21,B18,E19
VCCIO6	J7,D2,F6,C5,A1,G3
VCCIO7	M8,K4,P2,T6,L1,N5
VCCIO10	W11,Y14
VCCX	N9,L9,J9
VCC	L11,V10,P10,L13,K12,V12,K10,T12,M10,T10,J11,J13,U11
VCCLDO	C15,B8,B14,C7,B12,B10
VDDHAQ1	R9
VDDHAQ0	U9
VDDAQ1_VDDDQ1	AC9,AC13,AC11
VDDAQ0_VDDDQ0	D11,D9,D13
VDDTQ1	AA12,AA10
VDDTQ0	F10,F12
VDDXM	M12
VDDAM_VDDDM	N13,R13,U13,W13
VSS	M11,AE15,B15,A10,A12,A14,A16,A26,A6,A8,AA14,AA16,AA26,AA6,AB10,AB12,AB14,AB23,AB3,AA9,AB8,AC15,AC20,AC7,AD11,AD13,AD6,AD9,AD16,AE24,AE4,AE6,AF1,AF10,AF12,AF14,AF16,AF21,AF6,AF8,B16,B23,B3,B6,C11,C13,C16,C20,C6,C9,D15,D17,D7,E10,E12,E14,E24,E4,E7,E8,E9,F1,F14,F21,F9,G10,G11,AB9,G13,Y12,G18,G12,H25,H5,J12,J2,J22,K11,K13,K19,K9,L10,L12,L16,L26,L6,M13,M23,M3,M9,N10,N20,P13,P17,P7,P9,R10,R24,R4,T1,T11,T13,T21,T9,U10,U12,U18,U8,V15,V25,V5,E15,W12,W2,W22,Y11,Y10,Y13,Y19,V13

3.1.2 View of PG484A Pins Distribution

Figure 3-2 View of GW5AST-138 PG484A Pins Distribution (Top View)

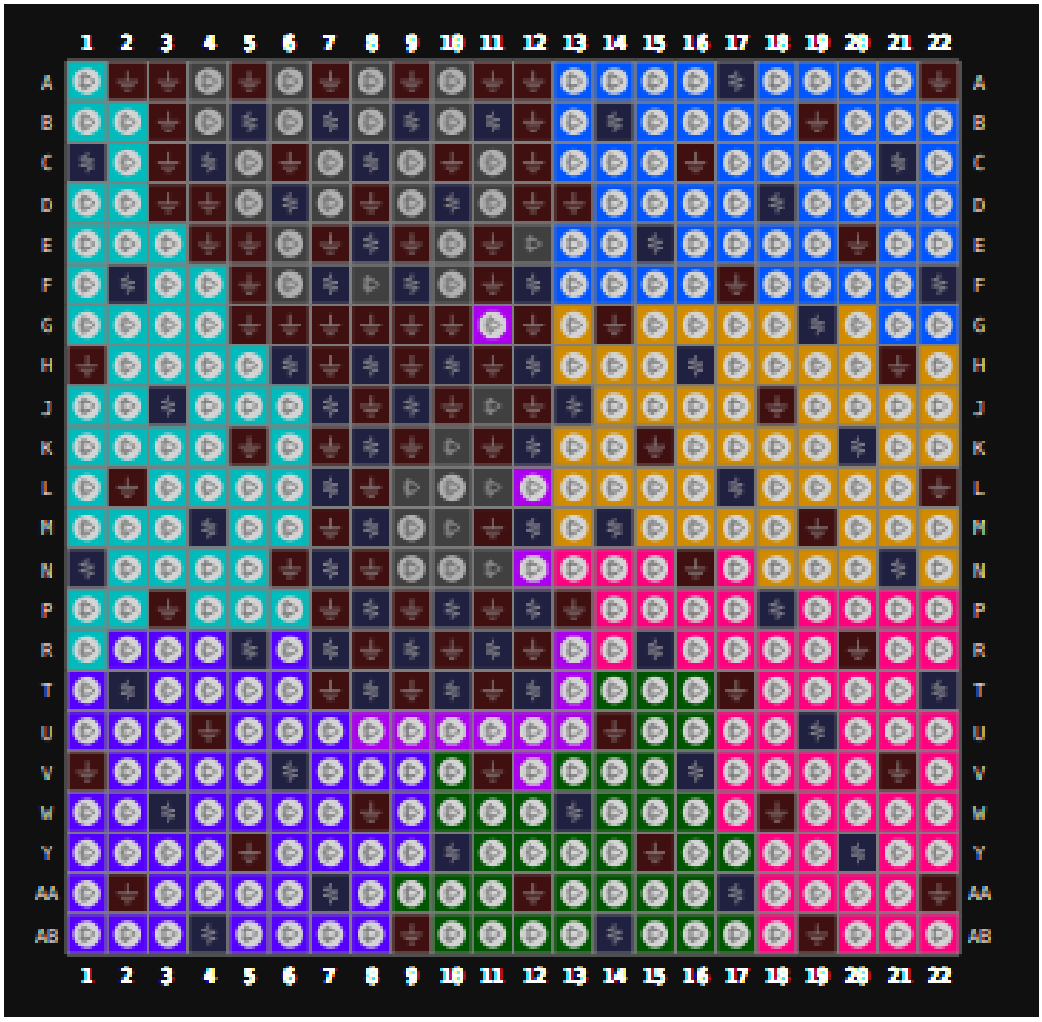


Table 3-2 Other Pins in GW5AST-138 PG484A

VCCIO2	B14,D18,E15,F22,A17,C21
VCCIO3	L17,J13,H16,G19,K20,N21
VCCIO4	U19,Y20,T22,M14,P18,R15
VCCIO5	W13,V16,AA17,AB14,Y10
VCCIO6	AA7,V6,W3,T2,R5,AB4
VCCIO7	C1,J3,N1,M4,H6,F2
VCCIO10	F12,T12
VCCX	P12,M12,R11
VCC	H8,T8,R9,H10,P8,N7,J7,R7,K8,L7,P10,T10,J9,M8
VCCLDO	B7,B9,B5,B11,C4,C8
VDDHAQ1	K12
VDDHAQ0	H12
VDDAQ0_VDDDQ0	F7,D10,D6
VDDTQ0	E8,F9

VSS	K9,D8,A2,A3,A5,A7,A9,A11,A12,A22,AA2,AA12,AA22,AB9,AB19,B3,B12,B19,C3,C6,C10,C12,C16,D3,D4,D12,D13,E4,E5,E7,E9,E11,E20,F5,F11,F17,G5,G6,G7,G8,G9,G10,G12,G14,H1,H7,H9,H11,H21,J8,J10,J12,J18,K5,K7,K11,K15,L2,L8,L22,M7,M11,M19,N6,N8,N16,P3,P7,P9,P11,P13,R8,R10,R12,R20,T7,T9,T11,T17,U4,U14,V1,V11,V21,W8,W18,Y5,Y15

3.1.3 View of PG676A Pins Distribution

Figure 3-3 View of GW5AST-138 PG676A Pins Distribution (Top View)

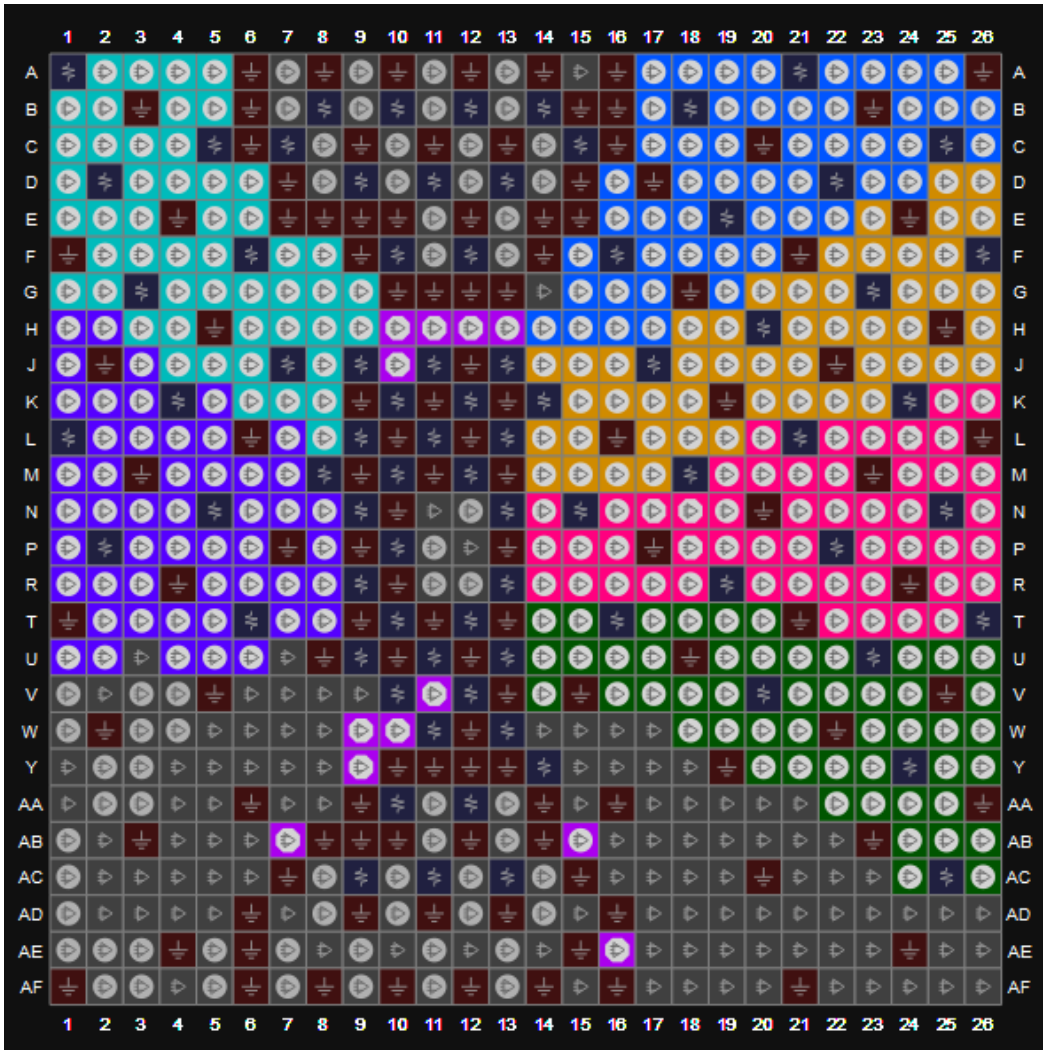


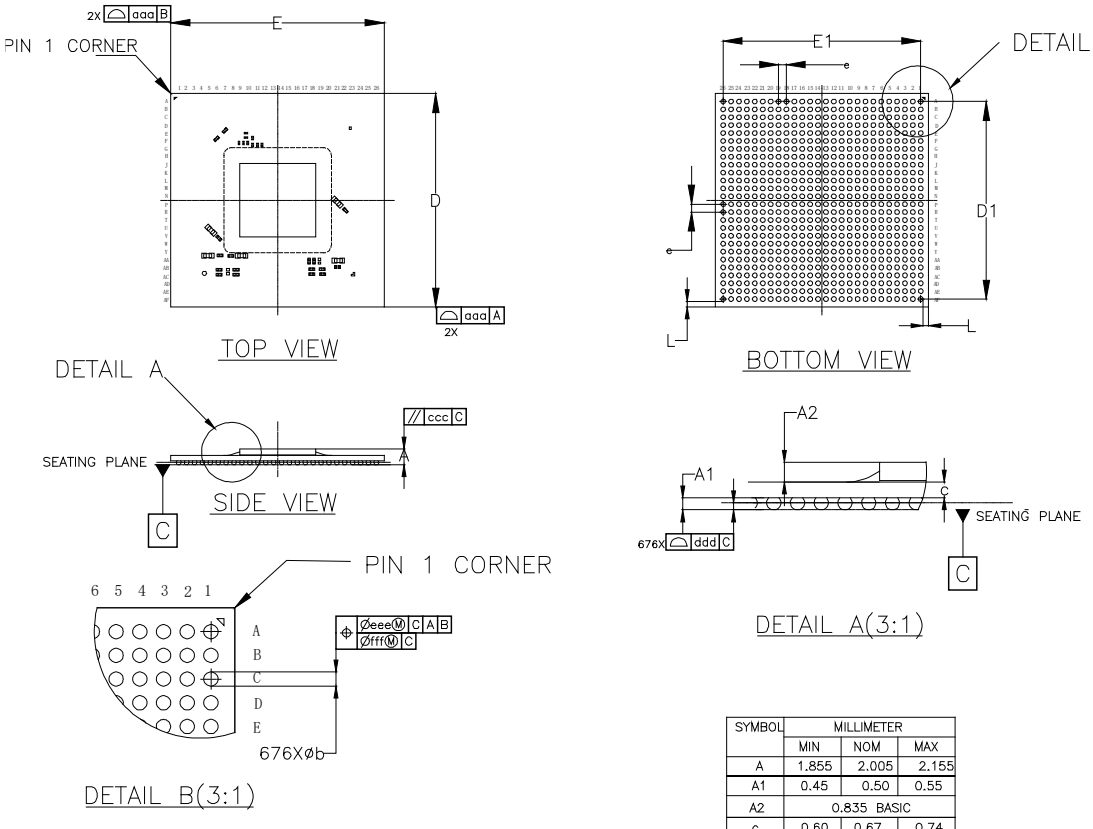
Table 3-3 Other Pins in GW5AST-138 PG676A

VCCIO2	E19,C25,A21,D22,F16,B18
VCCIO3	G23,K14,M18,H20,F26,J17
VCCIO4	L21,P22,N15,K24,N25,R19
VCCIO5	Y24,T16,U23,V20,AC25,T26
VCCIO6	L1,P2,N5,T6,K4,M8
VCCIO7	J7,D2,A1,G3,C5,F6
VCCIO10	Y14,W11
VCCX	N9,L9,J9
VCC	V12,V10,T12,L13,T10,L11,K12,M10,U11,K10,J11,P10,J13
VCCLDO	B12,B10,C7,C15,B14,B8
VDDXM	M12
VDDAM	N13,R13
VDDDM	U13,W13
VDDHAQ0_VDDHAQ1	U9,R9
VDDAQ0	AA12,AC11,AA10
VDDTQ0	AC13,AC9
VDDAQ1	F12,D9,F10
VDDTQ1	D13,D11
VSS	M11,AE15,B15,A10,A12,A14,A16,A26,A6,A8,AA14,AA16,AA26,AA6,AB10,AB12,AB14,AB23,AB3,AA9,AB8,AC15,AC20,AC7,AD11,AD13,AD6,AD9,AD16,AE24,AE4,AE6,AF1,AF10,AF12,AF14,AF16,AF21,AF6,AF8,B16,B23,B3,B6,C11,C13,C16,C20,C6,C9,D15,D17,D7,E10,E12,E14,E24,E4,E7,E8,E9,F1,F14,F21,F9,G10,G11,AB9,G13,Y12,G18,G12,H25,H5,J12,J2,J22,K11,K13,K19,K9,L10,L12,L16,L26,L6,M13,M23,M3,M9,N10,N20,P13,P17,P7,P9,R10,R24,R4,T1,T11,T13,T21,T9,U10,U12,U18,U8,V15,V25,V5,E15,W12,W2,W22,Y11,Y10,Y13,Y19,V13

4 Package Diagram

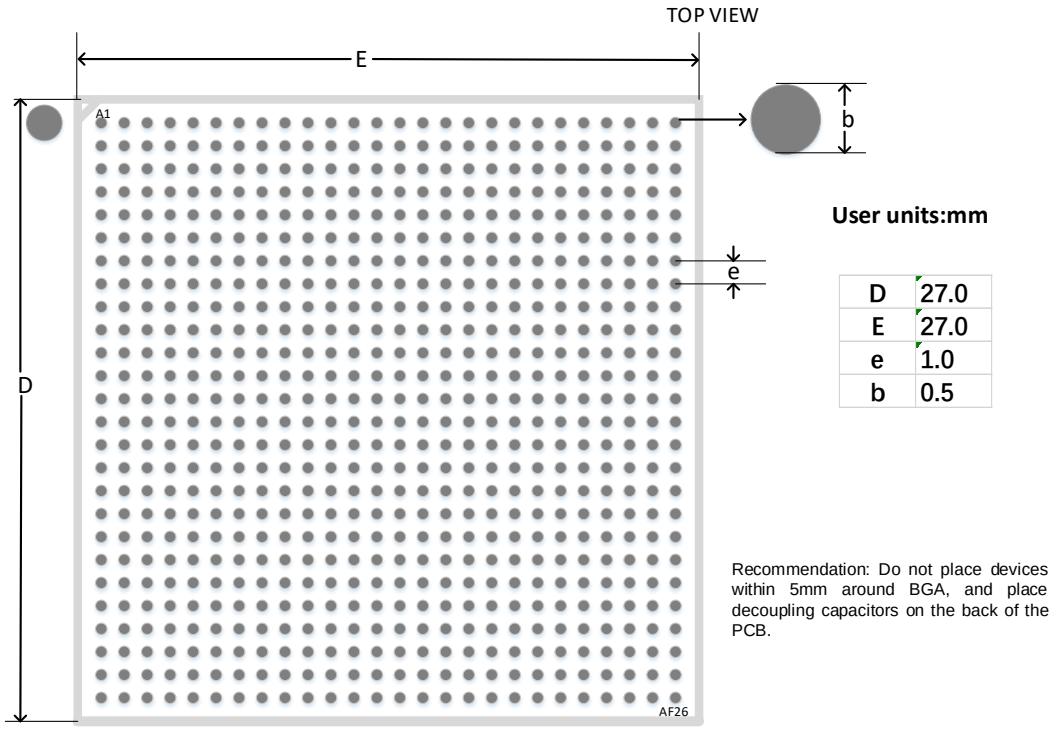
4.1 FPG676A (Flip Chip) Package Outline (27mm x 27mm, GW5AST-138)

Figure 4-1 Package Outline FPG676A (Flip Chip)



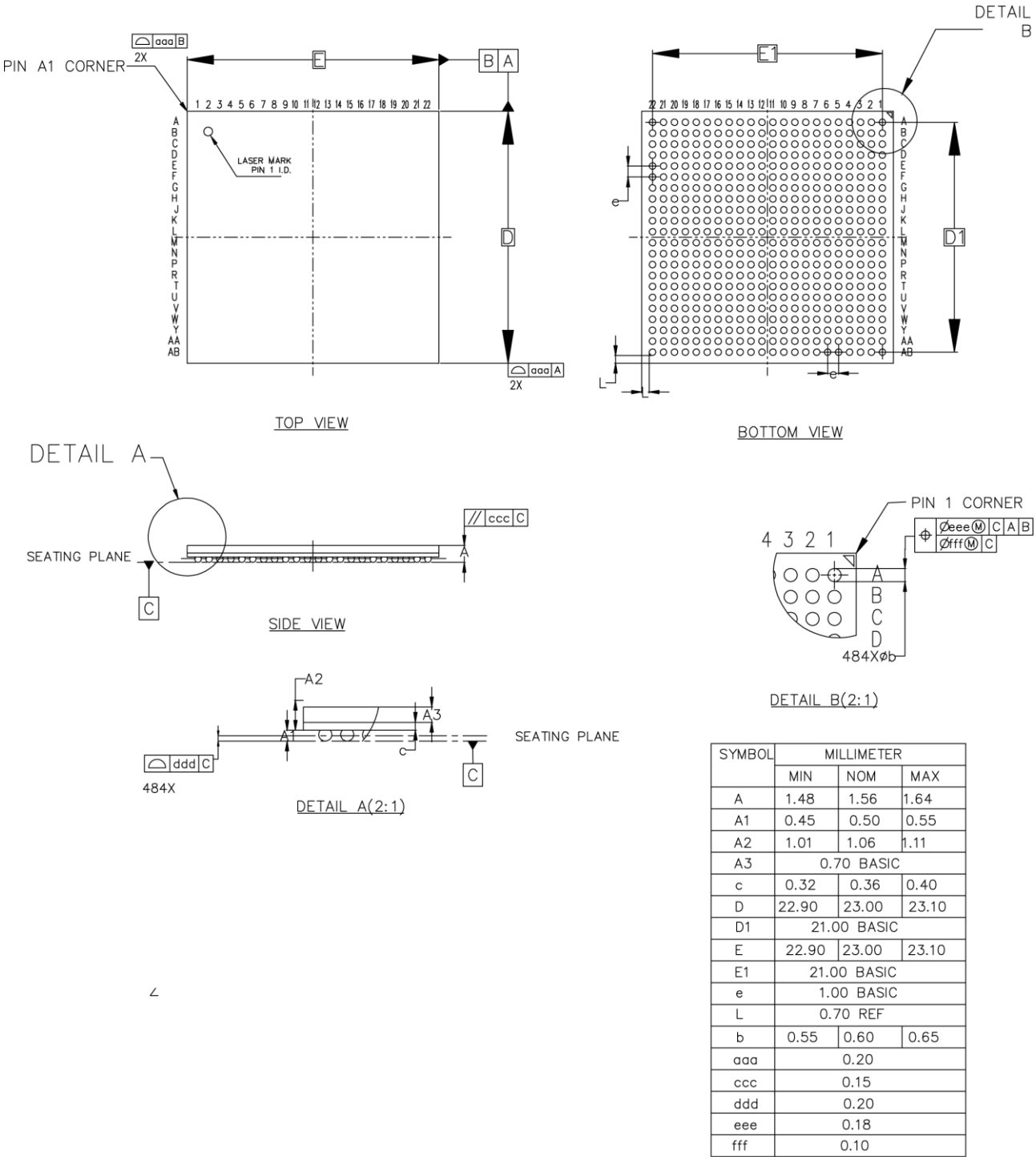
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.855	2.005	2.155
A1	0.45	0.50	0.55
A2	0.835 BASIC		
c	0.60	0.67	0.74
D	26.90	27.00	27.10
D1	25.00 BASIC		
E	26.90	27.00	27.10
E1	25.00 BASIC		
L	0.70 REF		
e	1.00 BASIC		
b	0.55	0.60	0.65
aaa	0.20		
ccc	0.25		
ddd	0.20		
eee	0.25		
fff	0.10		

Figure 4-2 Recommended PCB Layout FPG676A (Flip Chip)



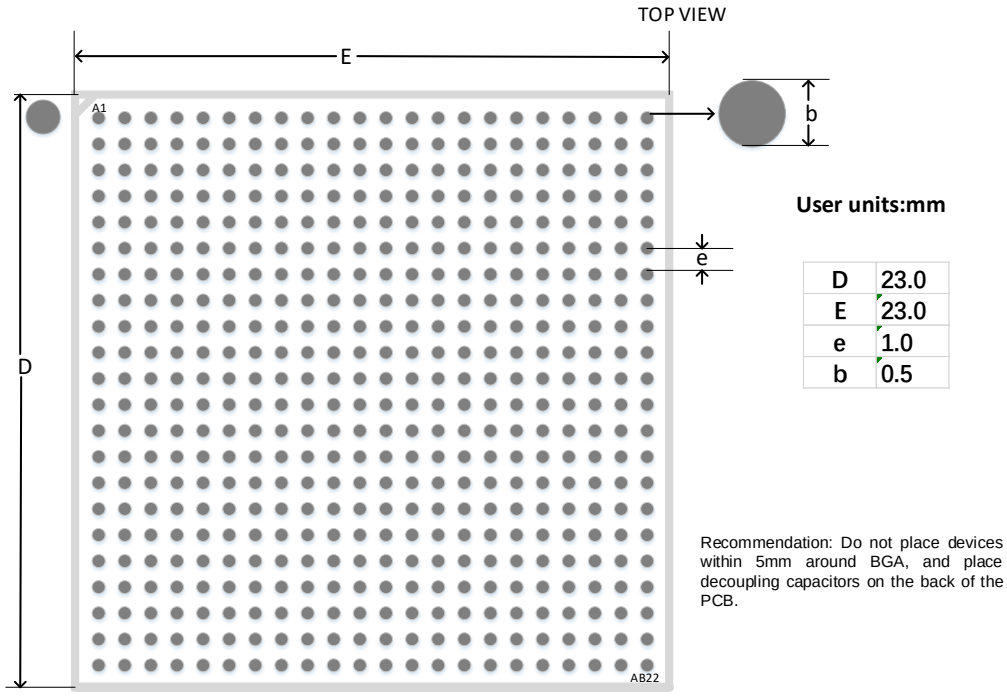
4.2 PG484A Package Outline (23mm x 23mm, GW5AST-138)

Figure 4-3 Package Outline PG484A



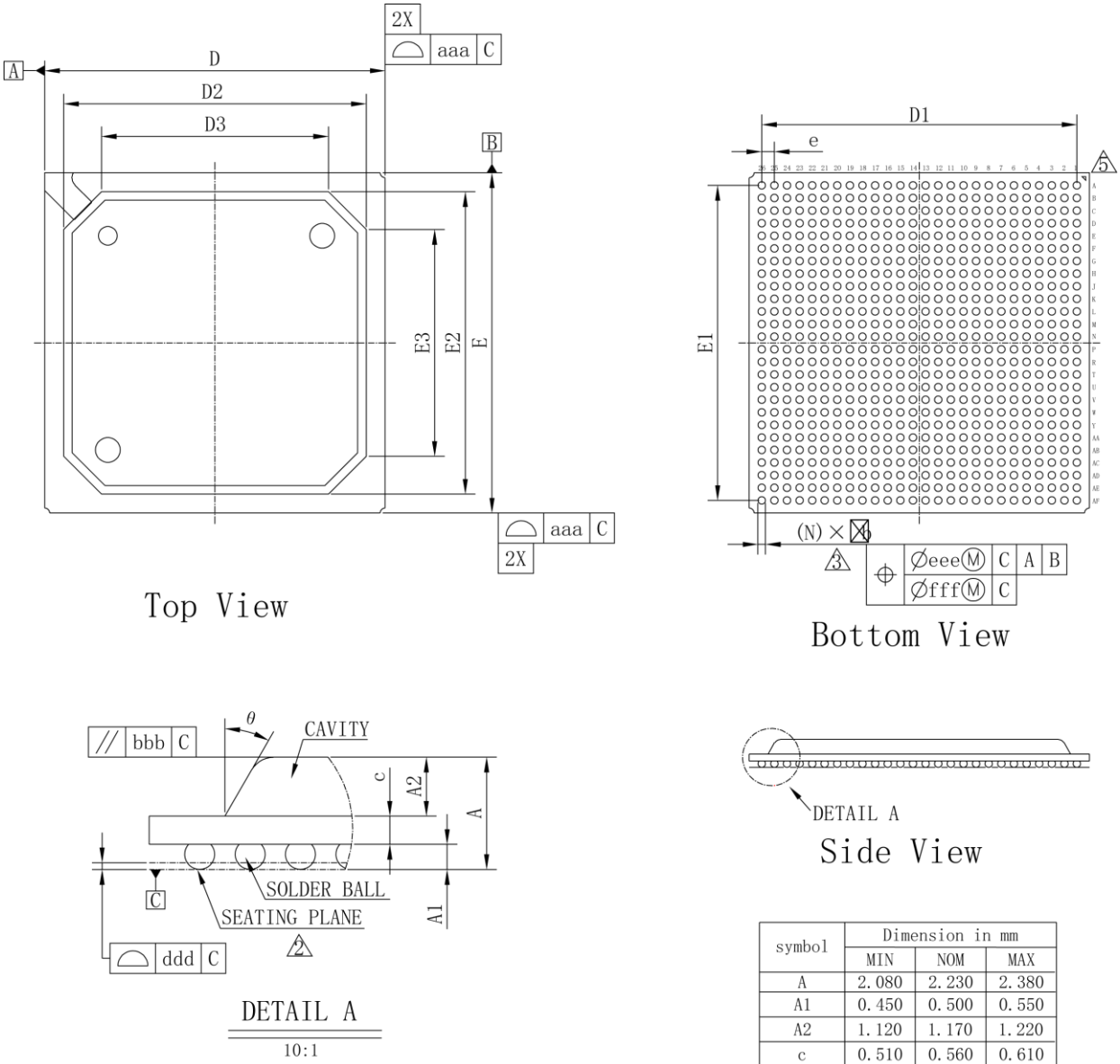
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.48	1.56	1.64
A1	0.45	0.50	0.55
A2	1.01	1.06	1.11
A3	0.70 BASIC		
c	0.32	0.36	0.40
D	22.90	23.00	23.10
D1	21.00 BASIC		
E	22.90	23.00	23.10
E1	21.00 BASIC		
e	1.00 BASIC		
L	0.70 REF		
b	0.55	0.60	0.65
aaa	0.20		
ccc	0.15		
ddd	0.20		
eee	0.18		
fff	0.10		

Figure 4-4 Recommended PCB Layout PG484A



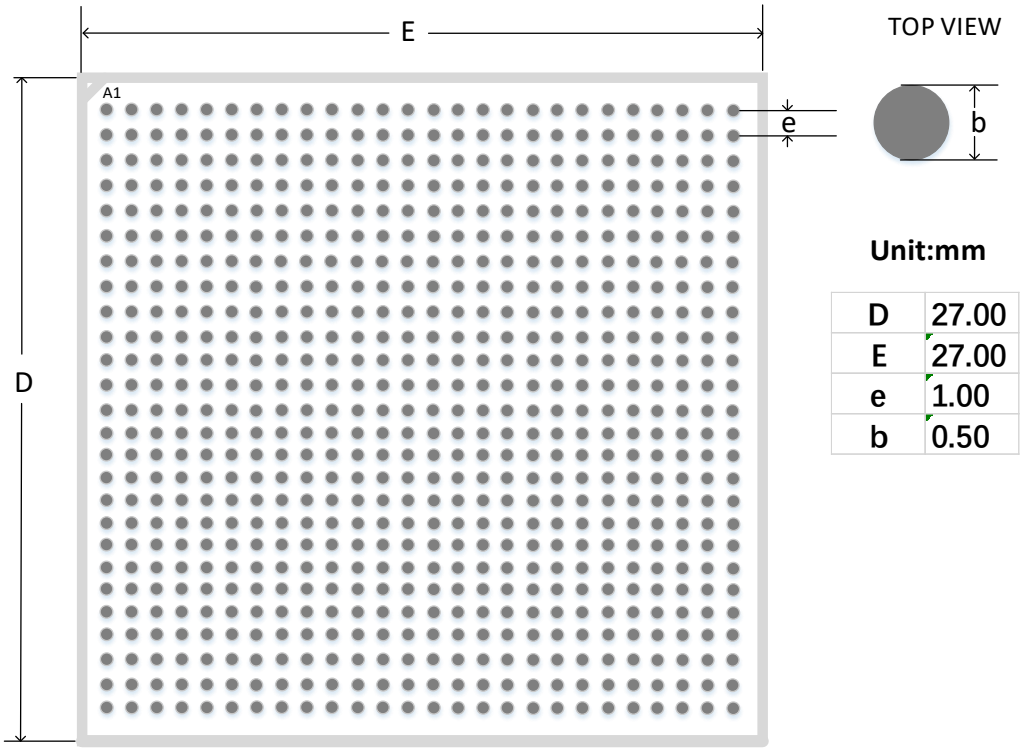
4.3 PG676A Package Outline (27mm x 27mm, GW5AST-138)

Figure 4-5 Package Outline PG676A



symbol	Dimension in mm		
	MIN	NOM	MAX
A	2.080	2.230	2.380
A1	0.450	0.500	0.550
A2	1.120	1.170	1.220
c	0.510	0.560	0.610
D	26.800	27.000	27.200
D1	---	25.000	---
D2	23.800	24.000	24.200
D3	---	18.000	---
E	26.800	27.000	27.200
E1	---	25.000	---
E2	23.800	24.000	24.200
E3	---	18.000	---
e	---	1.000	---
b	0.550	0.600	0.650
aaa	0.200		
bbb	0.200		
ddd	0.250		
eee	0.250		
fff	0.100		
Ball Diam	0.600		
N	676		
MD/ME	26/26		

Figure 4-6 Recommended PCB Layout PG676A

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