GW5AR series of FPGA Products

Package & Pinout User Guide

UG1109-1.0.4E, 03/14/2025

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Revision History

Date	Version	Description
09/12/2023	1.0E	Initial version published.
12/07/2023	1.0.1E	The info. of UG256P package for GW5AR-25 devices updated.
07/05/2024	1.0.2E	The names of voltage pins updated.
01/17/2025	1.0.3E	The “Figure 4-2 Recommended PCB Layout UG256P” in “4.1 UG256P Package Outline (14mm x 14mm)” added.
03/14/2025	1.0.4E	The names of power supply pins updated.

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1 About This Guide

1.1 Purpose

This manual introduces Gowin GW5AR series of FPGA products package and provides pin definitions, a list of pin numbers, pin distribution view, and package diagrams.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- DS1108, GW5AR series of FPGA Products Data Sheet
- UG1110, GW5AR-25 Pinout

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable Input/Output
UG	UBGA Package

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

GOWINSEMI's GW5AR series of FPGA products are the 5 series products of the Arora family, which are system-in-package chips that integrate PSRAM memory chips based on the GW5A. GW5AR series of FPGA products have abundant internal resources, including high-performance DSP resources with a new architecture and support for AI computing, high-speed LVDS interfaces, and abundant BSRAM resources. At the same time, the GW5AR series of FPGA products provide independently-developed DDR3 and a variety of packages. They are suitable for applications such as low power, high performance and compatibility designs.

GOWINSEMI provides a new generation of FPGA hardware development environment that supports FPGA synthesis, placement & routing, bitstream generation and download, etc.

2.1 PB-Free Package

GW5AR series of FPGA products are PB free in line with the EU RoHS environmental directives. The substances used in the GW5AR series of FPGA products are in full compliance with the IPC-1752 standards.

2.2 Package and Max. User I/O Information

Table 2-1 Package, Max. User I/O Information, and LVDS Pairs

Package	Pitch (mm)	Size (mm)	E-pad Size (mm)	GW5AR-25
UG256P	0.8	14x14	-	178 (86)

Note!

For package type abbreviations employed in this manual, see 1.3 Terminology and Abbreviations.

2.3 Power Pins

Table 2-2 GW5AR Power Pins

VCC	VCCIO0	VCCIO1	VCCIO2
VCCIO3	VCCIO4	VCCIO5	VCCIO6
VCCIO7	VCCIO10	VCCX	VCCLDO
VDDAM	VDDDM	VDDXM	VDD12M
VEFUSE	-	-	-

2.4 Pin Quantity

2.4.1 Quantity of GW5AR-25 Pins

Table 2-3 Quantity of GW5AR-25 Pins

Pin Type		GW5AR-25
		UG256P
Single-ended IO/Differential Pair/LVDS [1]	BANK0	30/15/15
	BANK1	0/0/0
	BANK2	28/14/14
	BANK3	14/7/7
	BANK4	21/10/10
	BANK5	25/12/12
	BANK6	28/14/14
	BANK7	28/14/14
	BANK10	4/2/0
	BANK11	0/0/0
Max. User I/O		178
Differential Pair		88
True LVDS Output		86
VCCIO0		2
VCCIO1		3
VCCIO2		3
VCCIO3		2
VCCIO4		2
VCCIO5		3
VCCIO6		3
VCCIO7		4
VCC		8
VDD12M		1
VCCIO10_VCCX_VCCLDO_VDDXM		2
VDDAM_VDDDM		1
VEFUSE		1

Pin Type	GW5AR-25
	UG256P
VSS	33
MODE0	1
MODE1	1
MODE2	0
NC	0

Note!

[1] Single-ended/Differential I/O quantity includes CLK pins and download pins.

2.5 I/O BANK Introduction

GW5AR-25 has eight GPIO Banks. Bank10 is a JTAG Bank with four Ios.

See *DS1108, GW5AR series of FPGA Products Data Sheet > 2.3 Input/Output Blocks* for details.

This manual provides the pin distribution view of GW5AR series of FPGA products. For details, please refer to Chapter 3 View of Pin Distribution. The I/O Banks that form GW5AR series of FPGA products are marked with different colors.

Various symbols and colors are used for the user I/O, power, and ground. The various symbols and colors used for the various pins are defined as follows:

- "  " denotes the I/O in BANK0.
- "  " denotes the I/O in BANK1.
- "  " denotes the I/O in BANK2.
- "  " denotes the I/O in BANK3.
- "  " denotes the I/O in BANK4.
- "  " denotes the I/O in BANK5.
- "  " denotes the I/O in BANK6.
- "  " denotes the I/O in BANK7.
- "  " denotes the I/O in BANK10.
- "  " denotes the I/O in BANK11
- "  " denotes the DIO in MIPI and ADC
- "  " denotes VCC, VCCX, VCCIO, and the filling color does not change.
- "  " denotes VSS, and the filling color does not change.
- "  " denotes NC.

3 View of Pin Distribution

3.1 View of GW5AR-25 Pin Distribution

3.1.1 View of UG256P Pin Distribution

Figure 3-1 View of GW5AR-25 UG256P Pin Distribution (Top View)

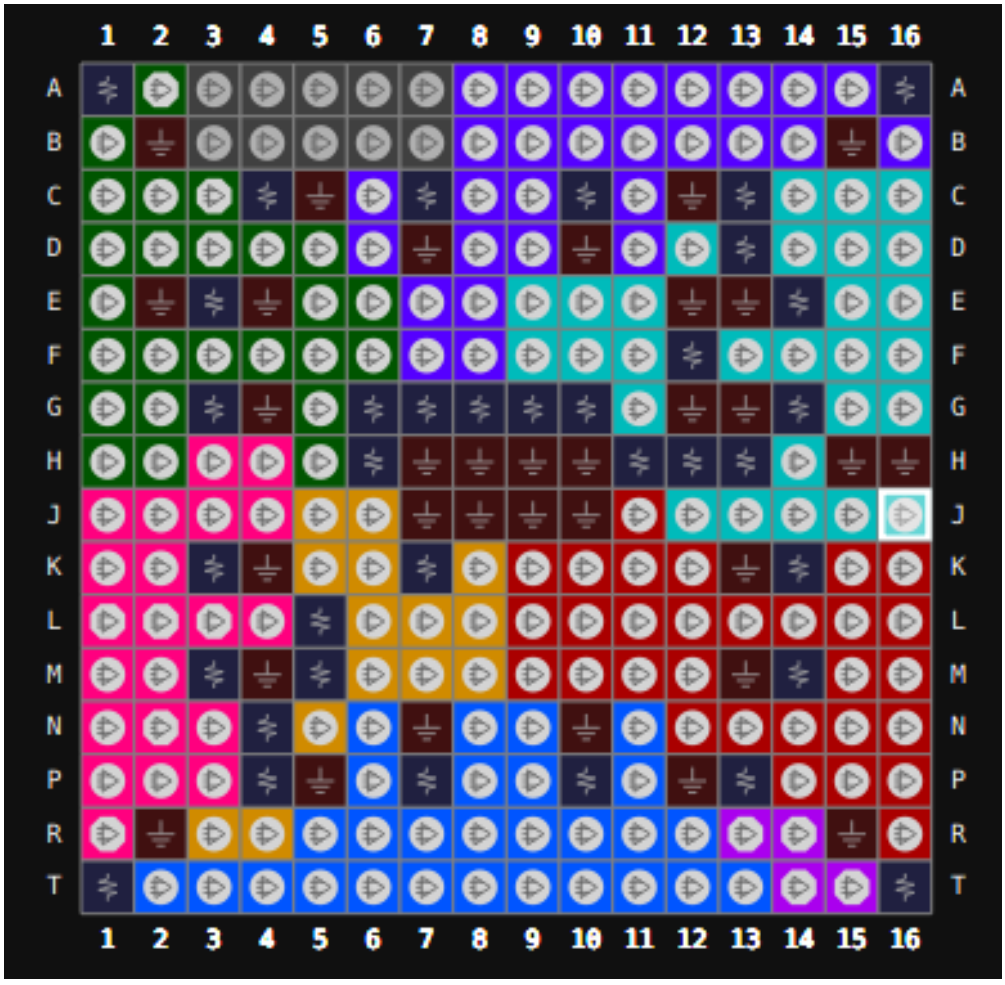


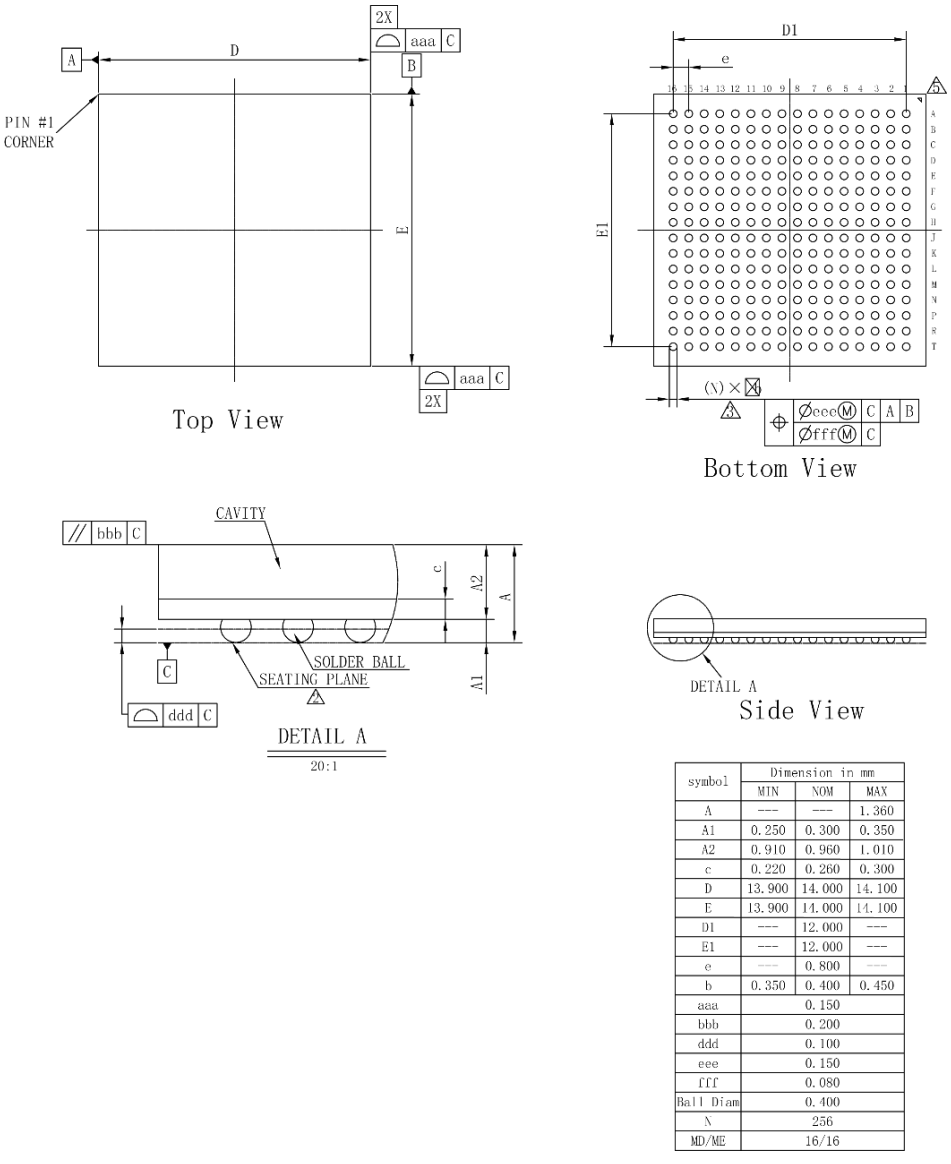
Table 3-1 Other Pins in GW5AR-25 UG256P

VCCIO0	M14,K14
VCCIO1	P10,P13,T16
VCCIO2	T1,P4,P7
VCCIO3	M3,K3
VCCIO4	G3,E3
VCCIO5	A1,C4,C7
VCCIO6	C10,A16,C13
VCCIO7	E14,H13,G14,H12
VEFUSE	M5
VCC	D13,H6,G10,G7,H11,K7,G8,N4
VDD12M	G9
VDDAM_VDDDM	G6
VCCIO10_VCCX_VCCLDO_VDDXM	L5,F12
VSS	B2,B15,C5,C12,D7,D10,E2,E4,E12,E13,G4,G12,G13,H7,H8,H9,H10,H15,H16,J7,J8,J9,J10,K4,K13,M4,M13,N7,N10,P5,P12,R2,R15

4 Package Diagram

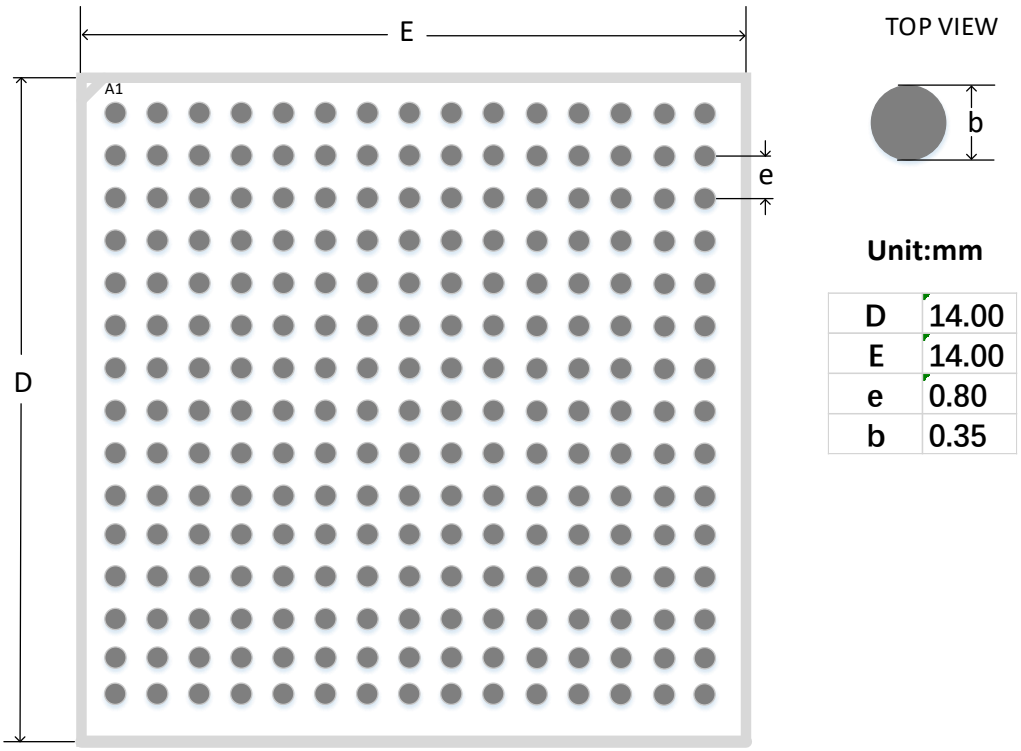
4.1 UG256P Package Outline (14mm x 14mm)

Figure 4-1 Package Outline UG256P



symbol	Dimension in mm		
	MIN	NOM	MAX
A	---	---	1.360
A1	0.250	0.300	0.350
A2	0.910	0.960	1.010
c	0.220	0.260	0.300
D	13.900	14.000	14.100
E	13.900	14.000	14.100
D1	---	12.000	---
E1	---	12.000	---
e	---	0.800	---
b	0.350	0.400	0.450
aaa	0.150		
bbb	0.200		
ddd	0.100		
eee	0.150		
fff	0.080		
Ball Diam	0.400		
N	256		
MD/ME	16/16		

Figure 4-2 Recommended PCB Layout UG256P



D	14.00
E	14.00
e	0.80
b	0.35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