GW5AT series of FPGA Products

Package & Pinout User Guide

UG983-1.2.8E, 08/15/2025

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Revision History

Date	Version	Description
04/20/2023	1.0E	Initial version published.
05/25/2023	1.1E	The info. of PG484 package added.
07/06/2023	1.1.1E	The info. of PG676A package added.
09/08/2023	1.1.2E	The info. of UG324 package added.
11/30/2023	1.1.3E	● The info. of UG324A package added. ● "Table 2-1 Package, Max. User I/O Information, and LVDS Pairs" in "2 Overview" optimized.
02/02/2022	1.1.4E	● The info. of UG484 package for GW5AT-75 devices added. ● The IO info. of all packages updated.
03/29/2024	1.1.5E	The info. of PG484A and UG225 packages for GW5AT-60 devices added.
06/28/2024	1.1.6E	● The names of voltage pins updated. ● The info. of UG324 package for GW5AT-138 devices removed. ● The info. of UG324S package for GW5AT-60 devices added.
07/19/2024	1.1.7E	The ddd value in "Figure 4-18 Recommended PCB Layout PG676A" updated.
08/09/2024	1.1.8E	The information of PG484F package for GW5AT-138 devices added.
09/06/2024	1.1.9E	The information of MG132 package for GW5AT-15 devices added.
10/25/2024	1.2E	● The information of CS130 package for GW5AT-15 devices added. ● The pin quantity of UG324A package in "Table 2-6 Quantity of GW5AT-138 Pins" updated.
12/30/2024	1.2.1E	The information of UG225H and UG324A packages for GW5AT-60 devices added.
03/14/2025	1.2.2E	The names of power supply pins updated.
04/11/2025	1.2.3E	● The "Figure 4-1 Package Outline CS130/CS130F (GW5AT-15)" updated. ● The VSS pins of "Table 3-1 Other Pins in GW5AT-15 MG132" updated.
04/30/2025	1.2.4E	● The information of CS234 and UG324 packages for GW5AT-60 devices added. ● The description of Bank 8 and Bank9 in "2.5 I/O BANK Introduction" added.
05/23/2025	1.2.5E	● "Table 2-4 Quantity of GW5AT-60 Pins" and "Table 3-5 Other Pins in GW5AT-60 PG484A" updated. ● The names of power supply pins of UG225, UG225H, UG324A, UG324S, and CS234 packages for GW5AT-60 devices optimized. ● The names of power supply pins of UG484 package for GW5AT-75 devices optimized.
06/27/2025	1.2.6E	The information of CS130F package for GW5AT-15 devices added.
07/25/2025	1.2.7E	The information of VCCIO1 pin for MG132 package in "3.1 View of GW5AT-15 Pin Distribution".
08/15/2025	1.2.8E	The "A" dimension in the package outlines for PG676A, UG225,

Date	Version	Description
		UG225H, UG324, and UG324S packages updated.

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1 About This Guide

1.1 Purpose

This manual introduces Gowin GW5AT series of FPGA products package and provides pin definitions, lists of pin numbers, pin distribution views, and package diagrams.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- DS981, GW5AT series of FPGA Products Data Sheet
- UG984, GW5AT & GW5AST series of FPGA Products Schematic Manual
- UG982, GW5AT-138 Pinout
- UG1221, GW5AT-75 Pinout
- UG1222, GW5AT-60 Pinout
- UG1224, GW5AT-15 Pinout

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
CS	WLCSP Package
FPG	FCPBGA Package
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable Input/Output
MG	MBGA Package
PG	PBGA Package

Terminology and Abbreviations	Meaning
UG	UBGA Package

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

Gowin GW5AT series of FPGA products are the 5 series of Arora family with abundant internal resources, a new-architecture and high-performance DSP supporting AI operations, high-speed LVDS interfaces, and abundant BSRAM resources. At the same time, GW5AT series integrate self-developed DDR3, 12.5Gbps SerDes supporting multiple protocols, and provide a variety of packages. They are suitable for applications such as low power, high performance and compatibility design.

Gowin provides a new generation of FPGA hardware development environment that supports GW5AT series of products, capable of fulfilling one-stop work such as FPGA synthesis, placement & routing, bitstream generation and download, etc.

2.1 PB-Free Package

GW5AT series of FPGA products are PB free in line with the EU RoHS environmental directives. The substances used in the GW5AT series of FPGA products are in full compliance with the IPC-1752 standards.

2.2 Package and Max. User I/O Information

Table 2-1 Package, Max. User I/O Information, and LVDS Pairs

Package			Pitch (mm)	Size (mm)	E-pad Size (mm)	GW5AT-15	GW5AT-60	GW5AT-75	GW5AT-138
Name	Type	Description							
FPG676A	FCPBGA	Flip Chip	1.0	27x27	-	-	-	-	311(150)
CS130	WLCSP	Wire Bond	0.4	5.3x4.0	-	53(25)	-	-	-
CS130F	WLCSP	Wire Bond	0.4	5.3x4.0	-	53(25)	-	-	-
CS234	WLCSP	Wire Bond	0.4	7.4x5.4	-	-	132(63)	-	-

Package			Pitch (mm)	Size (mm)	E-pad Size (mm)	GW5AT -15	GW5AT-60	GW5AT-75	GW5AT-138
Name	Type	Description							
MG132	MBGA	Wire Bond	0.5	8x8	-	53(25)	-	-	-
PG484	PBGA	Wire Bond	1.0	23x23	-	-	-	-	271(133)
PG484A	PBGA	Wire Bond	1.0	23x23	-	-	297(143)	-	291(143)
PG484F	PBGA	Wire Bond	1.0	23x23	-	-	-	-	276(133)
PG676A	PBGA	Wire Bond	1.0	27x27	-	-	-	-	311(150)
UG225	UBGA	Wire Bond	0.8	13x13	-	-	113(53)	-	-
UG225H	UBGA	Wire Bond	0.8	13x13	-	-	113(53)	-	-
UG324	UBGA	Wire Bond	0.8	15x15	-	-	160(76)	-	-
UG324A	UBGA	Wire Bond	0.8	15x15	-	-	162(76)	-	141(68)
UG324S	UBGA	Wire Bond	0.8	15x15	-	-	198(98)	-	-
UG484	UBGA	Wire Bond	0.8	19x19	-	-	-	311(150)	-

2.3 Power Pins

Table 2-2 GW5AT Power Pins

VDD12M	VDDAM	VDDDM	VDDXM
VDDAQ0	VDDAQ1	VDDHAQ0	VDDHAQ1
VDDTQ0	VDDTQ1	VDDTQ1	VCCIO2
VCCIO3	VCCIO4	VCCIO5	VCCIO6
VCCIO7	VCCIO8	VCCIO9	VCCIO10
VCCIO11	VCCIO12	VCC	VCCX
VREFP	VREFN	VEFUSE	VCCADC
VCCLDO	-	-	-

2.4 Pin Quantity

2.4.1 Quantity of GW5AT-15 Pins

Table 2-3 Quantity of GW5AT-15 Pins

Pin Type		GW5AT-15		
		MG132	CS130	CS130F
Single-ended IO/Differential Pair/LVDS[1]	BANK0	0/0/0	0/0/0	0/0/0
	BANK1	30/14/14	30/14/14	30/14/14
	BANK2	7/3/3	7/3/3	7/3/3
	BANK3	8/4/4	8/4/4	8/4/4
	BANK4	8/4/4	8/4/4	8/4/4
	BANK5	0/0/0	0/0/0	0/0/0
	BANK6	0/0/0	0/0/0	0/0/0
	BANK7	0/0/0	0/0/0	0/0/0
	BANK10	0/0/0	0/0/0	0/0/0

Pin Type		GW5AT-15		
		MG132	CS130	CS130F
	BANK11	0/0/0	0/0/0	0/0/0
Max. User I/O		53	53	53
Differential Pair		25	25	25
True LVDS Output		25	25	25
VCCIO1		2	2	2
VCCIO2		1	1	1
VCCIO3		1	1	1
VCCIO4		1	1	1
VCC		8	4	4
VCCX		3	0	0
VCCLDO		1	0	0
VCCX_VCCLDO_VDDXM		0	3	
VCCX _VDDXM		0	0	3
VDD12M		1	1	
VCCLDO_VDD12M		0	0	1
VEFUSE		1	1	1
VDDAM		2	5	5
VDDXM		1	0	0
VDDAQ0		4	3	3
VDDTQ0		1	2	2
VDDHAQ0		2	2	2
VSS		11	11	11
MODE0		1	1	1
MODE1		1	1	1
MODE2		0	0	0
NC		0	0	0

Note!

[1] Single-ended/Differential I/O quantity includes CLK pins and download pins.

2.4.2 Quantity of GW5AT-60 Pins

Table 2-4 Quantity of GW5AT-60 Pins

Pin Type		GW5AT-60						
		PG484A	CS234	UG324S	UG324A	UG324	UG225H	UG225
Single-ended IO/ Differential Pair/LVDS [1]	BANK0	0/0/0	0/0/0	0/0/0	0/0/0	0/0/0	0/0/0	0/0/0
	BANK1	25/12/12	0/0/0	34/17/17	25/12/12	16/8/8	8/4/4	8/4/4
	BANK2	26/12/12	34/17/17	22/11/11	25/12/12	12/6/6	6/3/3	6/3/3
	BANK3	8/4/4	8/4/4	14/7/7	8/4/4	9/4/4	8/4/4	8/4/4
	BANK4	16/8/8	16/8/8	16/8/8	0/0/0	16/8/8	6/3/3	6/3/3

Pin Type		GW5AT-60						
		PG484A	CS234	UG324S	UG324A	UG324	UG225H	UG225
	BANK5	34/16/16	20/9/9	34/16/16	0/0/0	20/9/9	20/9/9	20/9/9
	BANK6	20/10/10	0/0/0	0/0/0	15/7/7	2/1/1	0/0/0	0/0/0
	BANK7	24/12/12	0/0/0	0/0/0	15/7/7	10/5/5	0/0/0	0/0/0
	BANK8	24/12/12	0/0/0	0/0/0	20/10/10	16/8/8	16/8/8	16/8/8
	BANK9	66/33/33	48/24/24	56/28/28	50/24/24	32/16/16	36/18/18	36/18/18
	BANK10	25/12/12	2/1/1	8/4/4	0/0/0	14/7/7	5/2/2	5/2/2
	BANK11	25/12/12	0/0/0	10/5/5	0/0/0	9/4/4	4/2/2	4/2/2
	BANK12	4/2/0	4/2/0	4/2/0	4/2/0	4/2/0	4/2/0	4/2/0
Max. User I/O		297	132	198	162	160	113	113
Differential Pair		145	65	98	78	78	55	55
True LVDS Output		143	63	96	76	76	53	53
VCCIO1		3	0	3	3	2	0	0
VCCIO2		3	2	3	4	2	0	0
VCCIO2		0	0	2	0	0	0	0
VCCIO3		0	2	0	1	2	0	0
VCCIO4		3	2	2	0	2	0	0
VCCIO5		3	2	2	0	2	2	2
VCCIO6		2	0	0	2	0	0	0
VCCIO7		2	0	0	2	0	0	0
VCCIO8		2	0	0	3	2	2	2
VCCIO9		6	3	6	6	4	2	2
VCCIO10		3	1	2	0	4	0	0
VCCIO11		3	0	2	0	4	0	0
VCCIO12		0	1	0	1	1	0	0
VCCIO1_2		0	0	0	0	0	1	1
VCCIO10_11		0	0	0	0	0	2	2
VCCIO3_4_12		0	0	0	0	0	2	2
VCCIO3_12		2	0	0	0	0	0	0
VCCIO6_7		0	0	0	0	2	0	0
VCCIO12_VCCX_VDDHAQ0		0	0	11	0	0	0	0
VCC		14	0	11	18	9	7	7
VCCX		4	4	0	4	9	0	0
VCC_VDDDM		0	8	0	0	0	0	0
VDD12M		6	1	4	5	1	1	1
VDDAM		0	4	0	0	0	0	0
VDDAM_VDDDM		0	0	0	0	9	3	3

Pin Type	GW5AT-60						
	PG484A	CS234	UG324S	UG324A	UG324	UG225H	UG225
VDDXM	0	4	0	0	0	0	0
VCCX_VDDXM	0	0	0	0	0	6	6
VDDAQ0	3	6	0	2	6	3	3
VDDHAQ0	1	0	0	1	0	2	2
VDDTQ0	2	2	0	2	5	3	3
VCCADC	0	0	0	0	0	1	1
VCCADC_VDDHAQ0	0	2	0	0	4	0	0
VEFUSE	0	1	1	0	1	1	1
VEFUSE_VCCADC	1	0	0	1	0	0	0
VREFN	1	0	0	1	0	0	0
VREFP	1	0	0	1	0	0	0
VSS	88	17	45	76	48	35	35
MODE0	1	1	1	1	1	1	1
MODE1	1	1	1	1	1	1	1
MODE2	1	0	0	1	0	0	0
NC	9	0	7	4	0	0	0

Note!

[1] Single-ended/Differential I/O quantity includes CLK pins and download pins.

2.4.3 Quantity of GW5AT-75 Pins

Table 2-5 Quantity of GW5AT-75 Pins

Pin Type		GW5AT-75
		UBGA484
Single-ended IO/Differential Pair/LVDS[1]	BANK0	0/0/0
	BANK1	0/0/0
	BANK2	50/19/19
	BANK3	50/19/19
	BANK4	50/0/0
	BANK5	50/20/20
	BANK6	50/19/19
	BANK7	50/18/18
	BANK10	11/0/0
Max. User I/O[2]		311
Differential Pair		150
True LVDS Output		150
VCCIO2		3
VCCIO3		4
VCCIO4		4

Pin Type	GW5AT-75
	UBGA484
VCCIO5	5
VCCIO6	3
VCCIO7	3
VCCIO10	2
VCCX_VDDXM	2
VCC	12
VCCLDO	3
VDDAM_VDDDM	2
VDDAQ0	2
VDDHAQ0_VDDHAQ1	2
VDDTQ0	3
VDDAQ1	2
VDDTQ1	3
VSS	52
MODE0	1
MODE1	1
MODE2	1
NC	1

Note!

- [1] Single-ended/Differential I/O quantity includes CLK pins and download pins.
- [2] RECONFIG_N pin cannot be multiplexed as I/O.

2.4.4 Quantity of GW5AT-138 Pins

Table 2-6 Quantity of GW5AT-138 Pins

Pin Type		GW5AT-138					
		FPG676A (Flip Chip)	PG484A	PG484	PG484F	PG676A	UG324A
Single-ended IO/Differential pair/LVDS [1]	BANK0	0/0/0	0/0/0	0/0/0	0/0/0	0/0/0	0/0/0
	BANK1	0/0/0	0/0/0	0/0/0	0/0/0	0/0/0	0/0/0
	BANK2	50/24/24	50/24/24	50/24/24	50/24/24	50/24/24	25/12/12
	BANK3	50/24/24	50/24/24	50/24/24	50/24/24	50/24/24	25/12/12
	BANK4	50/24/24	50/24/24	50/24/24	50/24/24	50/24/24	50/24/24
	BANK5	50/24/24	35/17/17	35/17/17	35/17/17	50/24/24	13/6/6
	BANK6	50/24/24	50/24/24	50/24/24	50/24/24	50/24/24	13/6/6
	BANK7	50/24/24	50/24/24	30/14/14	30/14/14	50/24/24	4/2/2
	BANK10	12/6/6	12/6/6	12/6/6	12/6/6	12/6/6	12/6/6
Max. User I/O [2]		311	296	276	276	311	141
Differential Pair		150	143	133	133	150	68

Pin Type	GW5AT-138					
	FPG676A (Flip Chip)	PG484A	PG484	PG484F	PG676A	UG324A
True LVDS Output	150	143	133	133	150	68
VCCIO0	0	0	0	0	0	0
VCCIO1	0	0	0	0	0	0
VCCIO2	6	6	6	6	6	4
VCCIO3	6	6	6	6	6	3
VCCIO4	6	6	6	6	6	7
VCCIO5	6	5	5	5	6	0
VCCIO6	6	6	6	6	6	0
VCCIO7	6	6	6	6	6	0
VCCIO5_6_7	0	0	0	0	0	6
VCCIO10	2	2	2	2	2	2
VCCX	3	3	3	3	3	3
VCC	13	14	14	14	13	18
VCCLDO	6	6	6	6	6	1
VDDHAQ1	1	1	0	0	0	0
VDDHAQ0	1	1	2	2	0	1
VDDHAQ0_VDDHAQ1	0	0	0	0	2	0
VDDAQ1_VDDDQ1	3	0	0	0	0	0
VDDAQ0_VDDDQ0	3	0	0	0	0	0
VDDAQ0	0	3	3	3	3	2
VDDAQ1	0	0	0	0	3	0
VDDTQ1	2	0	0	0	2	0
VDDTQ0	2	2	2	2	2	2
VDDAM	0	0	0	0	2	0
VDDDM	0	0	0	0	2	0
VDDXM	1	0	1	1	1	1
VDDAM_VDDDM	4	0	2	2	0	3
VSS	120	88	88	88	120	76
MODE0	1	1	1	1	1	1
MODE1	1	1	1	1	1	1
MODE2	1	1	1	1	1	1
NC	102	8	5	5	103	9

Note!

- [1] Single-ended/Differential I/O quantity includes CLK pins and download pins.
- [2] RECONFIG_N pin cannot be multiplexed as I/O.

2.5 I/O BANK Introduction

GW5AT-15 has four GPIO Banks.

GW5AT-60 has eleven GPIO Banks. Bank12 is a JTAG Bank with four IOs.

GW5AT-75 has six GPIO Banks (Bank2~7), two SerDes Banks and a Bank for configuration (Bank 10).

GW5AT-138 has six GPIO Banks (Bank2~7), two SerDes Banks and a Bank for configuration (Bank 10). Bank 10 can also be used as an I/O Bank.

See *DS981, GW5AT series of FPGA Products Data Sheet > 2.3 Input/Output Blocks* for details.

This manual provides the pin distribution view of GW5AT series of FPGA products. For details, please refer to Chapter 3 View of Pin Distribution. The I/O Banks that form GW5AT series of FPGA products are marked with different colors.

Various symbols and colors are used for the user I/O, power, and ground. The various symbols and colors used for the various pins are defined as follows:

- "  " denotes the I/O in BANK1
- "  " denotes the I/O in BANK2.
- "  " denotes the I/O in BANK3.
- "  " denotes the I/O in BANK4.
- "  " denotes the I/O in BANK5.
- "  " denotes the I/O in BANK6.
- "  " denotes the I/O in BANK7.
- "  " denotes the I/O in BANK8.
- "  " denotes the I/O in BANK9.
- "  " denotes the I/O in BANK10.
- "  " denotes the DIO in SerDes Bank Q0, SerDes Bank Q1, MIPI, and ADC.
- "  " denotes VCC, VCCX, and VCCIO.
- "  " denotes VSS.
- "  " denotes NC.

3 View of Pin Distribution

3.1 View of GW5AT-15 Pin Distribution

3.1.1 View of MG132 Pin Distribution

Figure 3-1 View of GW5AT-15 MG132 Pin Distribution (Top View)

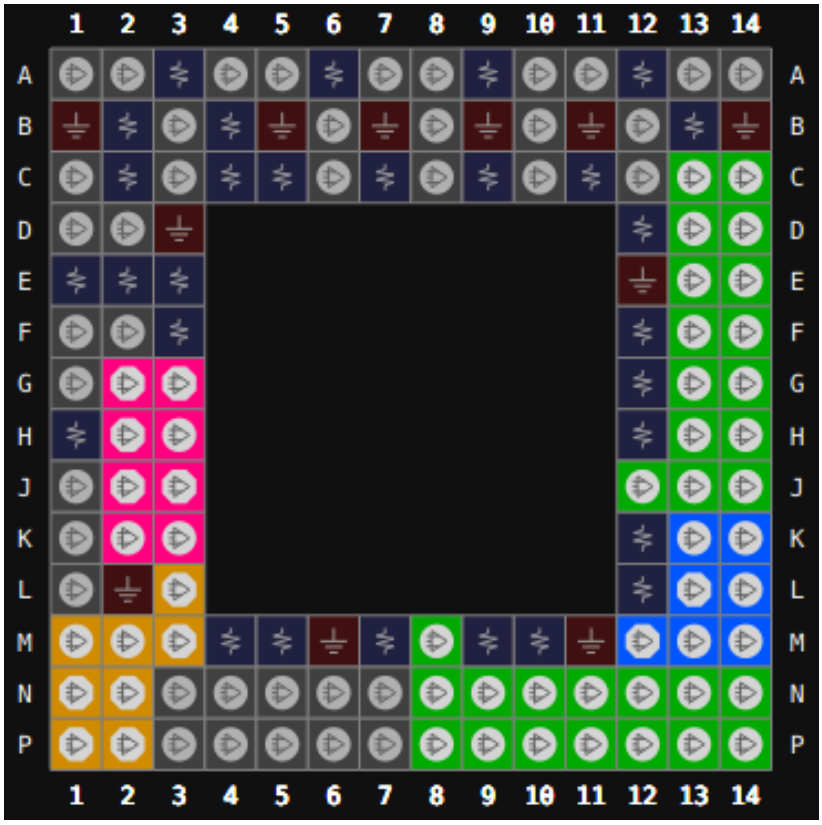


Table 3-1 Other Pins in GW5AT-15 MG132

VCC	E3,H1,B13,M10,B2,C5,C9,G12
VCCIO1	D12,M9
VCCIO2	M9
VCCIO3	M4
VCCIO4	F3
VCCX	H12,E1,C4
VCCLDO	F12
VDD12M	M7
VEFUSE	L12
VDDAM	M5, E2
VDDXM	C2
VDDHAQ0	C7,C11
VDDTQ0	B4
VDDAQ0	A6,A3,A12,A9
VSS	B1,B5,B7,B9,B11,B14,D3,E12,L2,M6,M11

3.1.2 View of CS130 Pin Distribution

Figure 3-2 View of GW5AT-15 CS130 Pin Distribution (Top View)

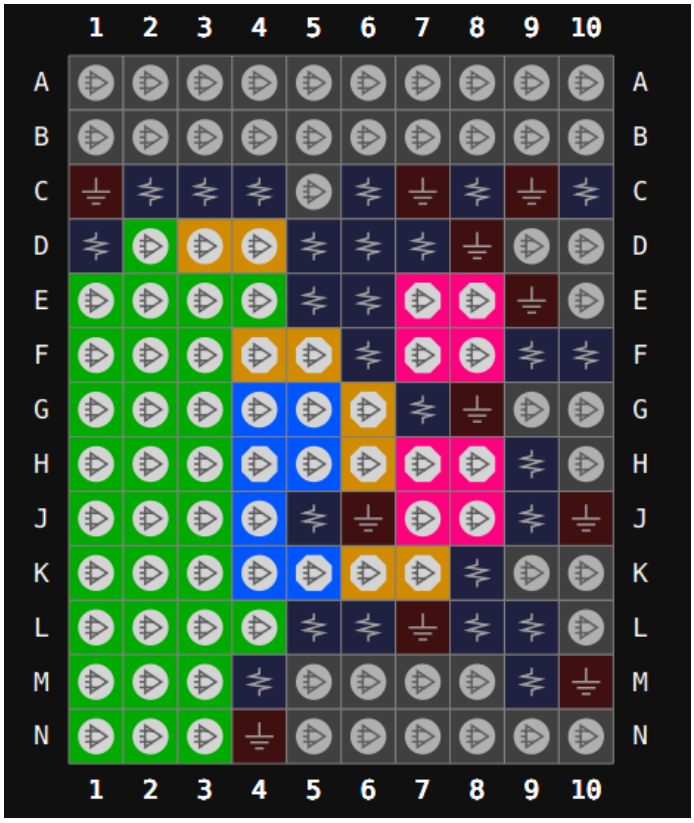


Table 3-2 Other Pins in GW5AT-15 CS130

VCC	F6,E5,E6,D5
VCCIO1	D1,C3

VCCIO2	M4
VCCIO3	J5
VCCIO4	G7
VCCX_VCCLDO_VDDXM	F9,L8,J9
VDD12M	K8
VEFUSE	L5
VDDAM	L6,L9,F10,M9,H9
VDDHAQ0	D6,D7
VDDTQ0	C8,C4
VDDAQ0	C2,C6,C10
VSS	J10,M10,E9,D8,G8,L7,J6,N4,C9,C7,C1

3.1.3 View of CS130F Pin Distribution

Figure 3-3 View of GW5AT-15 CS130F Pin Distribution (Top View)

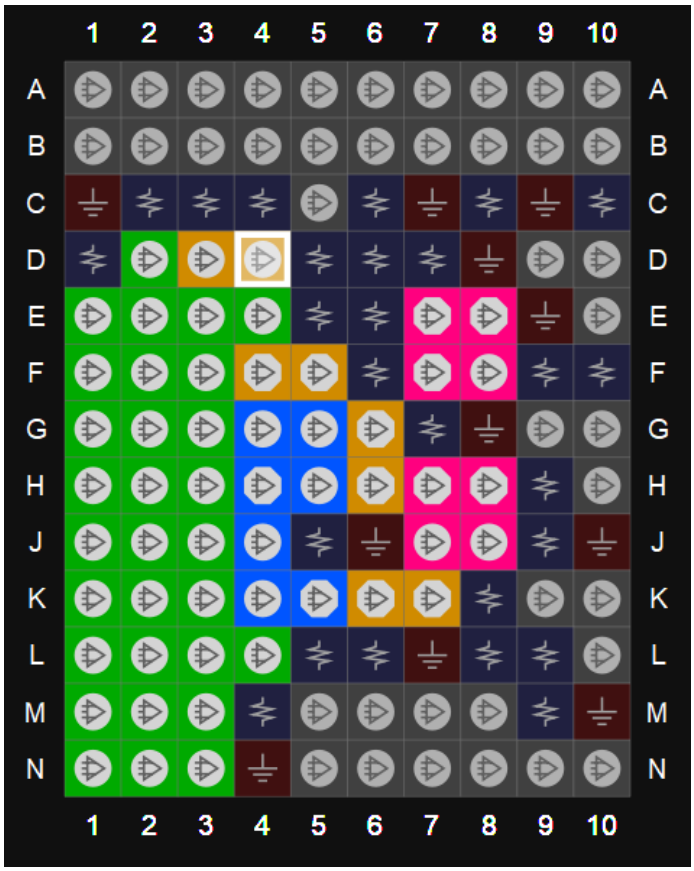


Table 3-3 Other Pins in GW5AT-15 CS130F

VCC	F6,E5,E6,D5
VCCIO1	D1,C3
VCCIO2	M4
VCCIO3	J5
VCCIO4	G7
VCCX _VDDXM	F9,L8,J9

VCCLDO_VDD12M	K8
VEFUSE	L5
VDDAM	L6,L9,F10,M9,H9
VDDHAQ0	D6,D7
VDDTQ0	C8,C4
VDDAQ0	C2,C6,C10
VSS	J10,M10,E9,D8,G8,L7,J6,N4,C9,C7,C1

3.2 View of GW5AT-60 Pin Distribution

3.2.1 View of CS234 Pin Distribution

Figure 3-4 View of GW5AT-15 CS234 Pin Distribution (Top View)

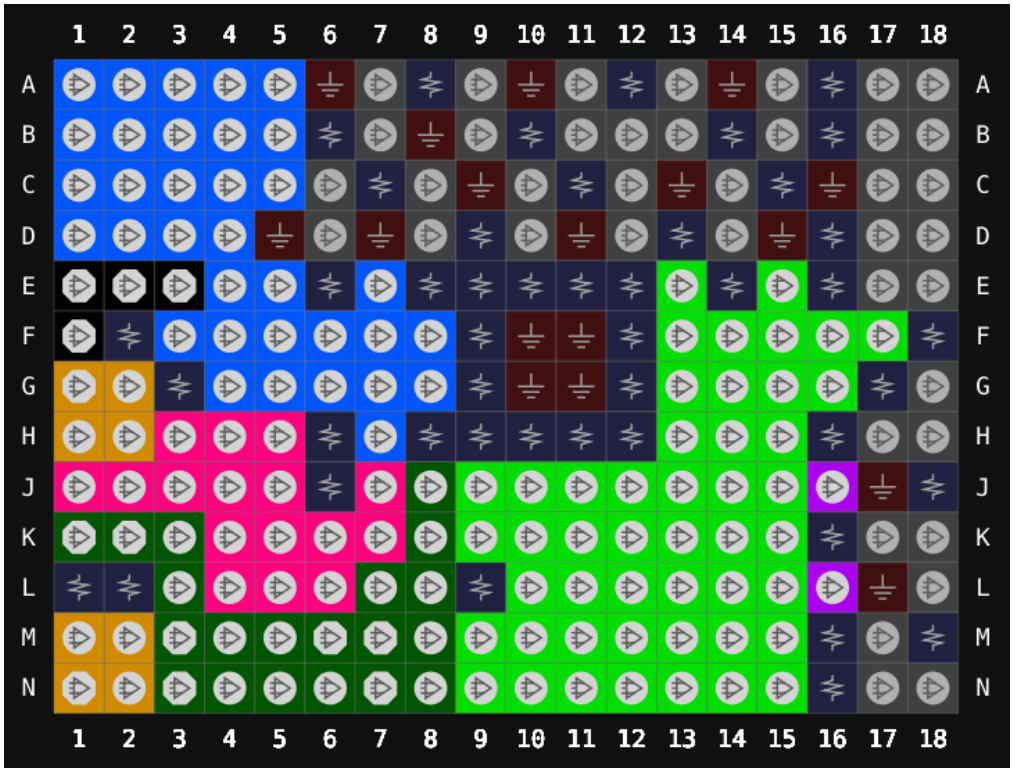


Table 3-4 Other Pins in GW5AT-15 CS234

VCCIO2	E6,E8
VCCIO3	L2,G3
VCCIO4	H6,J6
VCCIO5	H8,L9
VCCIO9	E14,H16,M16
VCCIO10	K16
VCCIO12	F2
VCCX	H12,E9,E12,H9
VEFUSE	L1
VCCADC_VDDHAQ0	A8,A12

VCC_VDDDM	H11,G9,F9,G12,E11,H10,E10,F12
VDDAM	E16,F18,M18,D16
VDDXM	B16,J18,A16,G17
VDD12M	N16
VDDAQ0	C11,C15,B6,D9,C7,D13
VDDTQ0	B14,B10
VSS	A6,A10,A14,B8,C9,C13,C16,D5,D7,D11,D15,F10, F11,G10,G11,J17,L17

3.2.2 View of PG484A Pin Distribution

Figure 3-5 View of GW5AT-60 PG484A Pin Distribution (Top View)

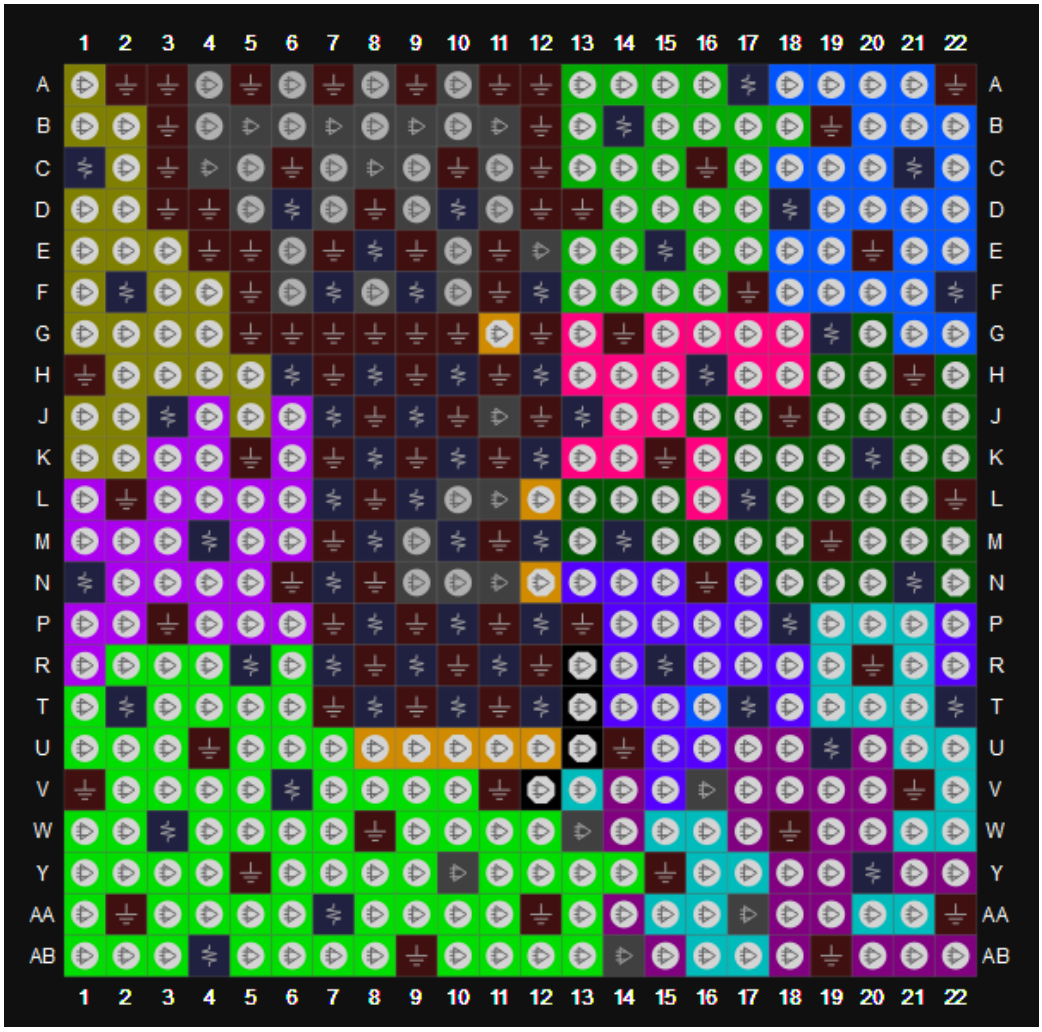


Table 3-5 Other Pins in GW5AT-60 PG484A

VCCIO1	B14,A17,C21
VCCIO2	D18,E15,F22
VCCIO4	H16,J13,G19
VCCIO5	L17,N21,K20
VCCIO6	M14,P18

VCCIO7	T22,R15
VCCIO8	Y20,U19
VCCIO9	V6,AB4,T2,AA7,W3,R5
VCCIO10	C1,H6,F2
VCCIO11	M4,J3,N1
VCCIO3_12	F12,T12
VCC	J9,P10,P8,N7,H10,M8,R9,T8,R7,T10,K8,H8,J7,L7
VCCX	P12,R11,H12,M12
VEFUSE_VCCADC	K10
VREFN	L9
VREFP	M10
VDD12M	B5,B7,B9,B11,C4,C8
VDDAQ0	F9,E8,F7
VDDHAQ0	K12
VDDTQ0	D10,D6
VSS	D8,A2,A3,A5,A7,A9,A11,A12,A22,AA2,AA12,AA22,AB9,AB19,B3,B12,B19,C3,C6,C10,C12,C16,D3,D4,D12,D13,E4,E5,E7,E9,E11,E20,F5,F11,F17,G5,G6,G7,G8,G9,G10,G12,G14,H1,H7,H9,H11,H21,J8,J10,J12,J18,K5,K7,K11,K15,L2,L8,L22,M7,M11,M19,N6,N8,N16,P3,P7,P9,P11,P13,R8,R10,R12,R20,T7,T9,T11,U4,U14,V1,V11,V21,W8,W18,Y5,Y15,K9,T17

3.2.3 View of UG225 Pin Distribution

Figure 3-6 View of GW5AT-60 UG225 Pin Distribution (Top View)

Table 3-6 Other Pins in GW5AT-60 UG225

VCCIO5	M14,J12
VCCIO8	P12,P8
VCCIO9	M7,P4
VCCIO1_2	B12
VCCIO10_11	M2,L4
VCCIO3_4_12	D14,H14
VCC	F9,H9,G8,J8,H7,K7,J10
VCCADC	E12
VEFUSE	L11
VDDAM_VDDDM	D2,H2,G4
VCCX_VDDXM	M12,J6,B1,F7,K9,G10
VDD12M	G6
VDDAQ0	D5,D11,B8
VDDHAQ0	D7,D9
VDDTQ0	A10,A6,B4
VSS	A1,A15,B10,B6,C13,C3,E11,F14,F2,F6,G7,G9,H8,J7,J9,K14,K2,K6,N13,N3,P10,P6,R1,R15,A2,B2,A4,D3,E4,A8,C9,C11,A12,C7,C5

3.2.4 View of UG225H Pin Distribution

Figure 3-7 View of GW5AT-60 UG225H Pin Distribution (Top View)

Table 3-7 Other Pins in GW5AT-60 UG225H

VCCIO5	M14,J12
VCCIO8	P12,P8
VCCIO9	M7,P4
VCCIO1_2	B12
VCCIO10_11	M2,L4
VCCIO3_4_12	D14,H14
VCC	F9,H9,G8,J8,H7,K7,J10
VCCADC	E12
VEFUSE	L11
VDDAM_VDDDM	D2,H2,G4
VCCX_VDDXM	M12,J6,B1,F7,K9,G10
VDD12M	G6
VDDAQ0	D5,D11,B8
VDDHAQ0	D7,D9
VDDTQ0	A10,A6,B4
VSS	A1,A15,B10,B6,C13,C3,E11,F14,F2,F6,G7,G9,H8,J7,J9,K14,K2,K6,N13,N3,P10,P6,R1,R15,A2,B2,A4,D3,E4,A8,C9,C11,A12,C7,C5

3.2.5 View of UG324 Pin Distribution

Figure 3-8 View of GW5AT-60 UG324 Pin Distribution (Top View)

Table 3-8 Other Pins in GW5AT-60 UG324

VCCIO1	E11,B12
VCCIO2	B15,G15
VCCIO3	H16,J17
VCCIO4	J18,J14
VCCIO5	R17,M15
VCCIO6_7	U14,R12
VCCIO8	P9,U9
VCCIO9	R6,N7,U4,P5
VCCIO10	M4,R2,J3,J2
VCCIO11	J5,H6,G4,E2
VCCIO12	E17
VCC	M12,H11,K9,J8,L8,J10,K11,H9,L10
VCCADC_VDDHAQ0	B8,B10,A6,B5
VCCX	J12,E14,P10,B17,P14,E9,G10,B1,M9
VEFUSE	L11
VDD12M	V4
VDDAQ0	C5,B4,A3,D3,D7,C7
VDDTQ0	B11,A12,D13,E10,D9
VDDAM_VDDDM	L2,F3,G7,P3,N1,U2,C2,M7,H3
VDDXM	E5,K7
VSS	A1,A18,C16,E15,G12,G17,G2,G5,H10,H8,J11,J15,J4,J9,K10,K8,L9,M17,M2,M6,N13,R1,R14,R18,R4,R9,T16,U12,U6,V1,V18,B13,K1,K3,N3,T3,E4,D12,B7,C3,D10,D5,B3,C8,C12,D6,C10,A9

3.2.6 View of UG324A Pin Distribution

Figure 3-9 View of GW5AT-60 UG324A Pin Distribution (Top View)

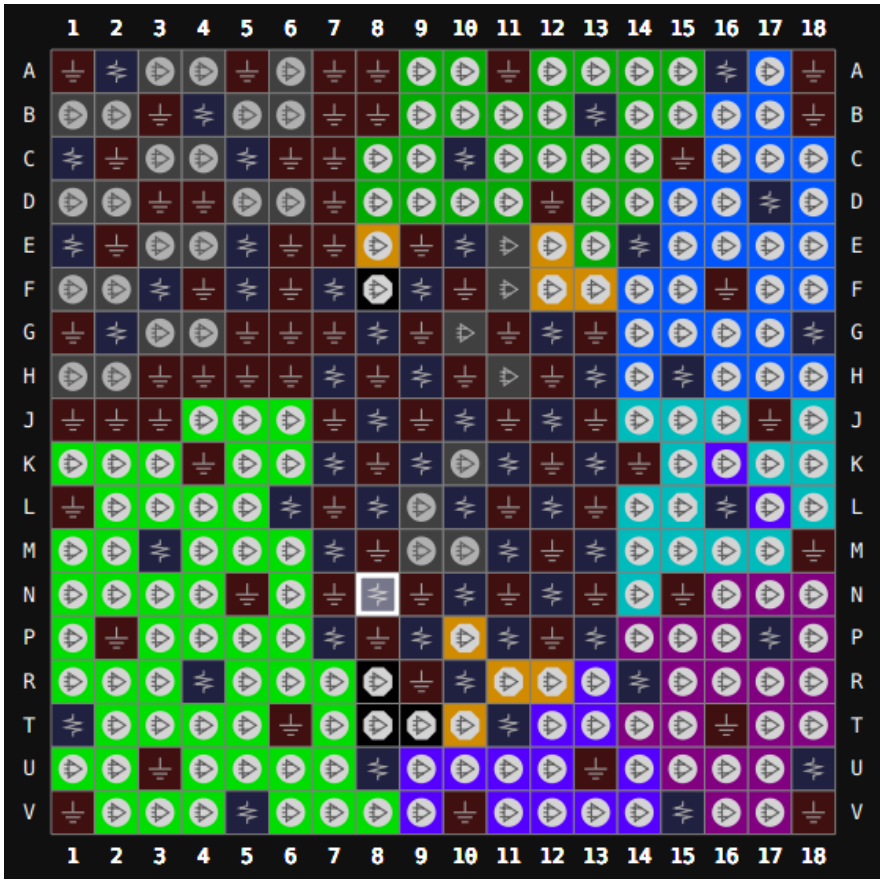


Table 3-9 Other Pins in GW5AT-60 UG324A

VCCIO1	C10,A16,B13
VCCIO2	G18,H15,D17,E14
VCCIO3	E10
VCCIO6	U8,T11
VCCIO7	P17,L16
VCCIO8	R14,V15,U18
VCCIO9	V5,M3,P7,T1,R4,L6
VCCIO2	R10
VCCX	K13,H13,P13,M13
VCC	K7,F9,M7,J12,N10,M11,N8,K11,N12,H7,P11,L12, J8,P9,G8,L8,F7,H9
VEFUSE_VCCADC	J10
VDD12M	G2,E1,A2,C1,F3
VDDAQ0	F5,E5
VDDTQ0	B4,C5
VDDHAQ0	G12
VREFN	K9
VREFP	L10

VSS	A1,A11,A18,A5,A7,A8,B18,B3,B7,B8,C15,C2,C6,C7,D12,D3,D4,D7,E2,E6,E7,E9,F10,F16,F4,F6,G1,G11,G13,G5,G6,G7,G9,H10,H12,H3,H4,H5,H6,H8,J1,J11,J13,J17,J2,J3,J7,J9,K12,K14,K4,K8,L1,L11,L13,L7,M12,M18,M8,N11,N13,N15,N5,N7,N9,P12,P2,P8,R9,T16,T6,U13,U3,V1,V10,V18

3.2.7 View of UG324S Pin Distribution

Figure 3-10 View of GW5AT-60 UG324S Pin Distribution (Top View)

Table 3-10 Other Pins in GW5AT-60 UG324S

VCCIO1	E17,G15,J14
VCCIO2	J17,M15,R17
VCCIO3	R12,U14
VCCIO4	P9,U9
VCCIO5	R6,U4
VCCIO9	R2,G4,E2,M4,J2,J5
VCCIO10	F8,C3
VCCIO11	B15,G12
VCCIO12_VCCX_VDDHAQ0	P10,M9,D14,B1,P14,G10,J12,D4,K7,B17,P5
VEFUSE	R4
VDD12M	H9,J10,K9,J8,M12,G7,K11,L8,M7,L10,H11
VDDAQ0	E11,B7,B11,D10

VSS	A1,A11,A18,A7,A9,B13,B5,B9,C10,C12,C14,C16,C4,C6,D8,E13,E15,F11,F9,G17,G2,G5,H10,H8,J11,J15,J4,J9,K10,K8,L11,L9,M17,M2,M6,N13,R1,R14,R18,R9,T16,U12,U6,V1,V18

3.3 View of GW5AT-75 Pin Distribution

3.3.1 View of UG484 Pin Distribution

Figure 3-11 View of GW5AT-75 UG484 Pin Distribution (Top View)

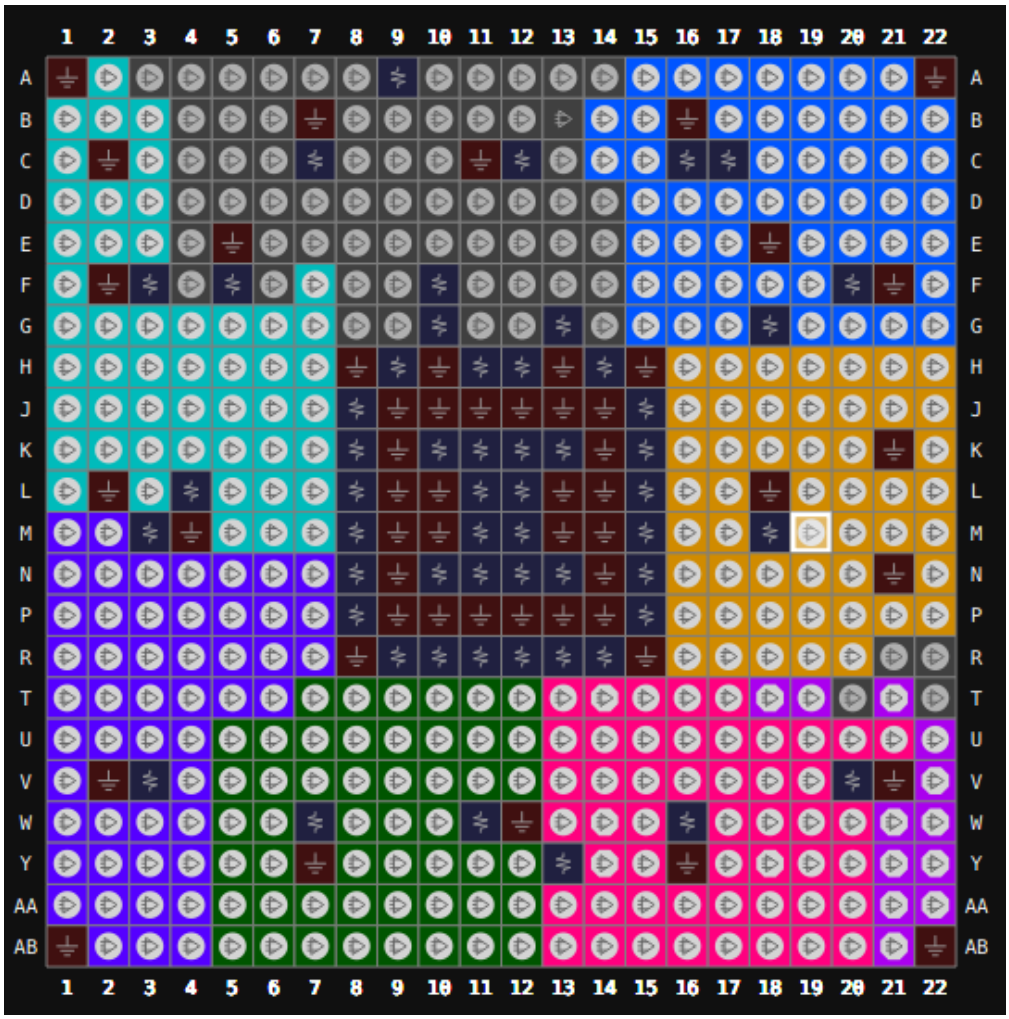


Table 3-11 Other Pins in GW5AT-75 UG484

VCCIO2	G18,F20,L15
VCCIO3	P15,N15,M15,M18
VCCIO4	R13,R12,R14,Y13
VCCIO5	R11,R9,R10,W11,W7
VCCIO6	P8,N8,V3
VCCIO7	L8,M3,M8
VCCIO10	V20,W16
VCCX_VDDXM	L4,F3
VCCLDO	K8,J8,F5

VCC	L11,M12,N12,M11,K10,K12,N11,N10,K13,N13,L12,K11
VDDTQ1	C12,H14,H12
VDDAQ1	C16,G13
VDDTQ0	F10,C17,H11
VDDHAQ0_VDDHAQ1	K15,J15
VDDAQ0	C7,G10
VDDAM_VDDDM	H9,A9
VSS	A22,AB22,F21,K21,N21,V21,E18,L18,B16,Y16,H15,R15,J14,K14,L14,M14,N14,P14,H13,J13,L13,M13,P13,J12,P12,W12,C11,J11,P11,H10,J10,L10,M10,P10,J9,K9,L9,M9,N9,P9,H8,R8,B7,Y7,E5,M4,C2,F2,L2,V2,A1,AB1

3.4 View of GW5AT-138 Pin Distribution

3.4.1 View of FPG676A (Flip Clip) Pin Distribution

Figure 3-12 View of GW5AT-138 FPG676A (Flip Chip) Pin Distribution (Top View)

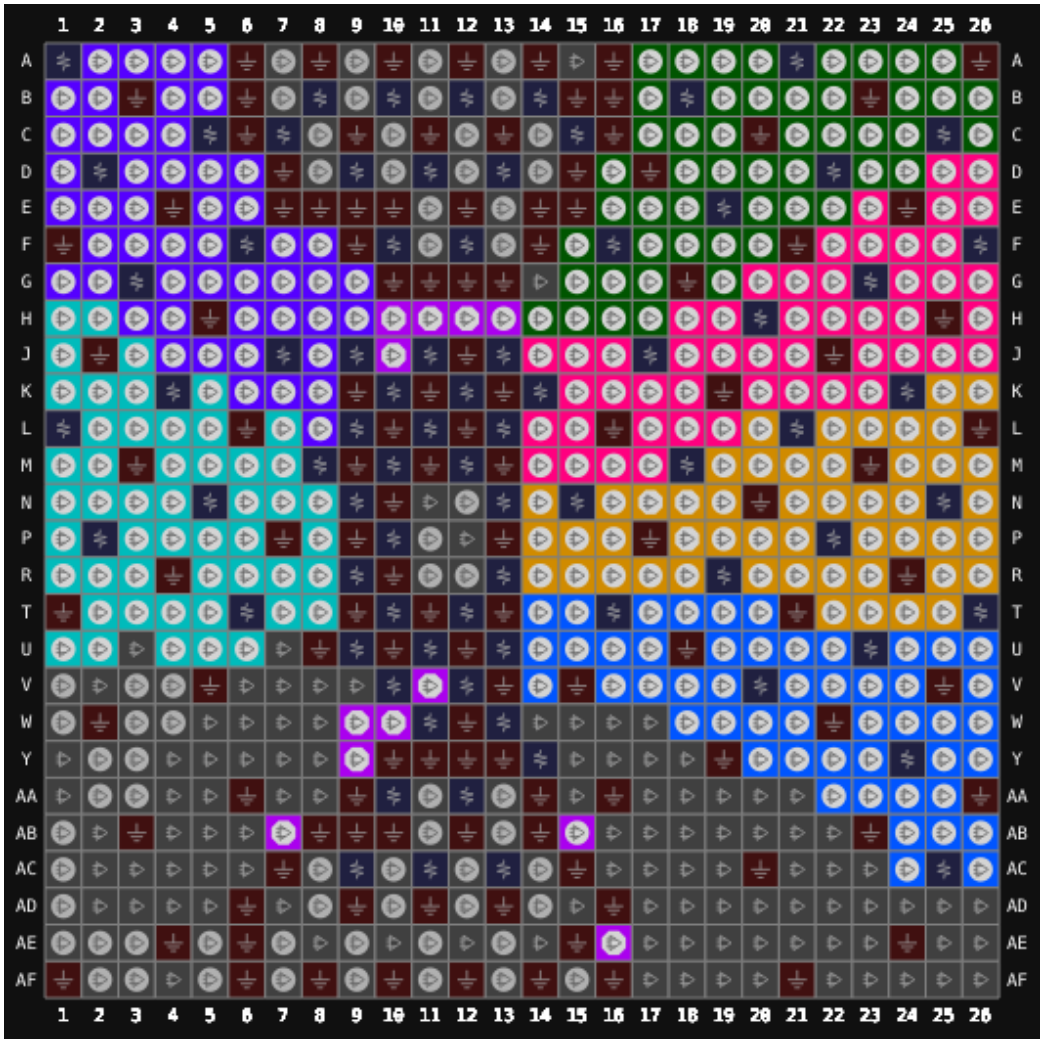


Table 3-12 Other Pins in GW5AT-138 FPG676A (Flip Chip)

VCCIO2	V20,U23,T26,Y24,AC25,T16
VCCIO3	R19,K24,N25,N15,P22,L21
VCCIO4	F26,M18,J17,H20,G23,K14
VCCIO5	C25,D22,F16,A21,B18,E19
VCCIO6	J7,D2,F6,C5,A1,G3
VCCIO7	M8,K4,P2,T6,L1,N5
VCCIO10	W11,Y14
VCCX	N9,L9,J9
VCC	L11,V10,P10,L13,K12,V12,K10,T12,M10,T10,J11,J13,U11
VCCLDO	C15,B8,B14,C7,B12,B10
VDDHAQ1	R9
VDDHAQ0	U9
VDDAQ1_VDDDQ1	AC9,AC13,AC11
VDDAQ0_VDDDQ0	D11,D9,D13
VDDTQ1	AA12,AA10
VDDTQ0	F10,F12
VDDXM	M12
VDDAM_VDDDM	N13,R13,U13,W13
VSS	M11,AE15,B15,A10,A12,A14,A16,A26,A6,A8,AA14,AA16,AA26,AA6,AB10,AB12,AB14,AB23,AB3,AA9,AB8,AC15,AC20,AC7,AD11,AD13,AD6,AD9,AD16,AE24,AE4,AE6,AF1,AF10,AF12,AF14,AF16,AF21,AF6,AF8,B16,B23,B3,B6,C11,C13,C16,C20,C6,C9,D15,D17,D7,E10,E12,E14,E24,E4,E7,E8,E9,F1,F14,F21,F9,G10,G11,AB9,G13,Y12,G18,G12,H25,H5,J12,J2,J22,K11,K13,K19,K9,L10,L12,L16,L26,L6,M13,M23,M3,M9,N10,N20,P13,P17,P7,P9,R10,R24,R4,T1,T11,T13,T21,T9,U10,U12,U18,U8,V15,V25,V5,E15,W12,W2,W22,Y11,Y10,Y13,Y19,V13

3.4.2 View of PG484 Pin Distribution

Figure 3-13 View of GW5AT-138 PG484 Pin Distribution (Top View)

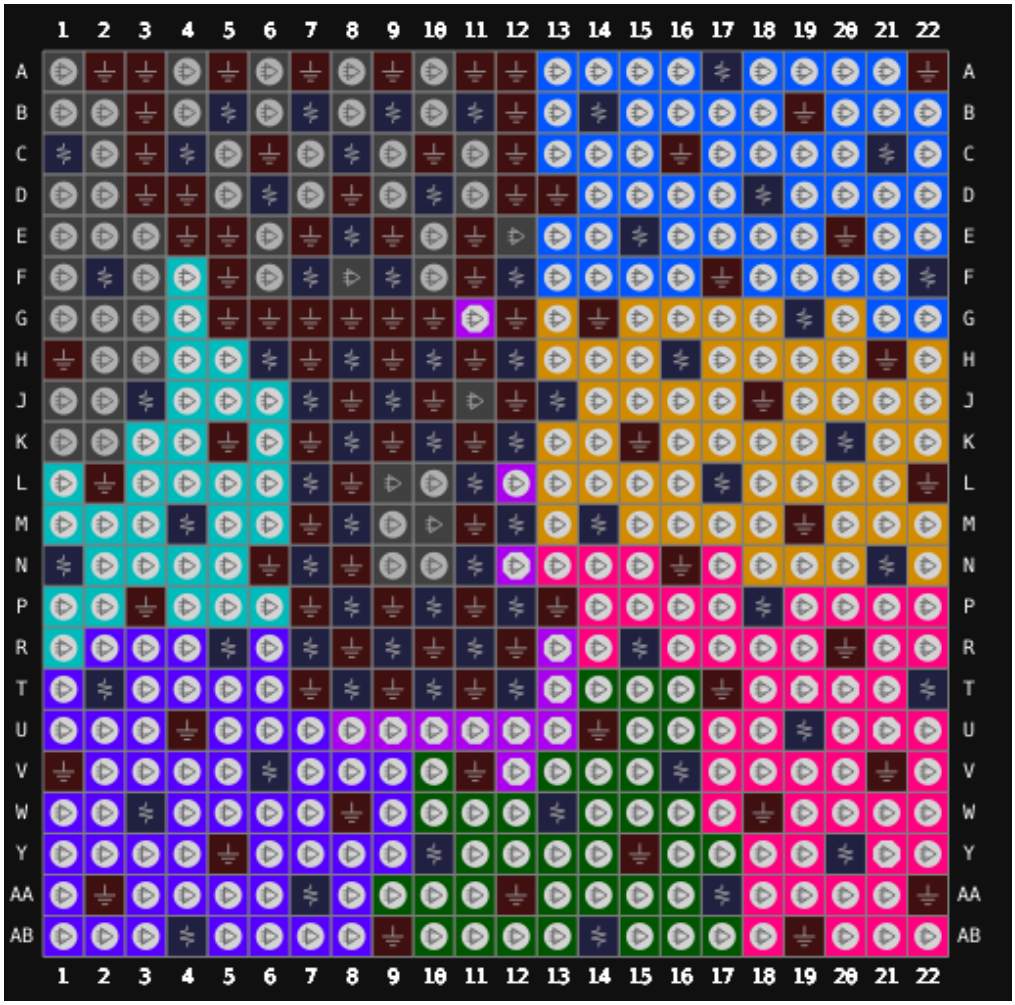


Table 3-13 Other Pins in GW5AT-138 PG484

VCCIO2	B14,D18,E15,F22,A17,C21
VCCIO3	L17,J13,H16,G19,K20,N21
VCCIO4	U19,Y20,T22,M14,P18,R15
VCCIO5	W13,V16,AA17,AB14,Y10
VCCIO6	AA7,V6,W3,T2,R5,AB4
VCCIO7	C1,J3,N1,M4,H6,F2
VCCIO10	F12,T12
VCCX	P12,M12,R11
VCC	H8,T8,R9,H10,P8,N7,J7,R7,K8,L7,P10,T10,J9,M8
VCCLDO	B7,B9,B5,B11,C4,C8
VDDXM	K10
VDDAM_VDDDM	L11,N11
VDDHAQ0	H12, K12
VDDAQ0_VDDDQ0	F7,D10,D6
VDDTQ0	E8,F9

VSS	K9,D8,A2,A3,A5,A7,A9,A11,A12,A22,AA2,AA12,AA22,AB9,AB19,B3,B12,B19,C3,C6,C10,C12,C16,D3,D4,D12,D13,E4,E5,E7,E9,E11,E20,F5,F11,F17,G5,G6,G7,G8,G9,G10,G12,G14,H1,H7,H9,H11,H21,J8,J10,J12,J18,K5,K7,K11,K15,L2,L8,L22,M7,M11,M19,N6,N8,N16,P3,P7,P9,P11,P13,R8,R10,R12,R20,T7,T9,T11,T17,U4,U14,V1,V11,V21,W8,W18,Y5,Y15

3.4.3 View of PG484A Pin Distribution

Figure 3-14 View of GW5AT-138 PG484A Pin Distribution (Top View)

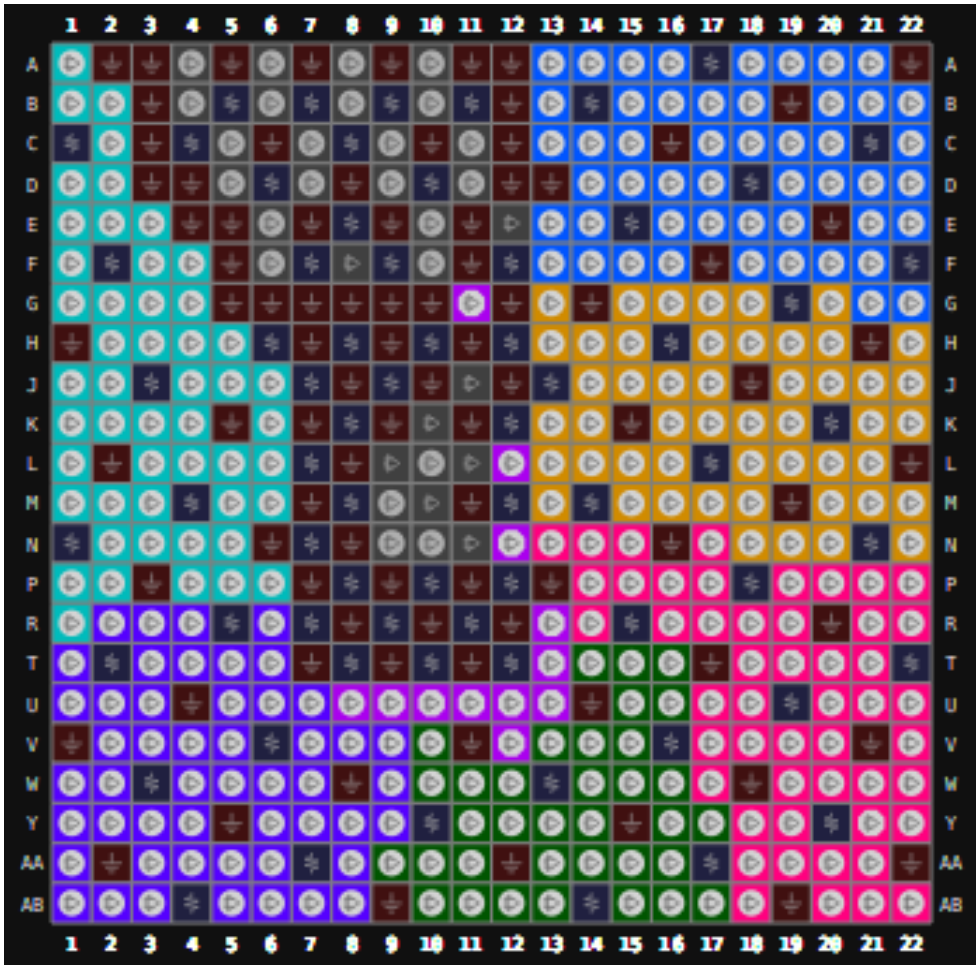


Table 3-14 Other Pins in GW5AT-138 PG484A

VCCIO2	B14,D18,E15,F22,A17,C21
VCCIO3	L17,J13,H16,G19,K20,N21
VCCIO4	U19,Y20,T22,M14,P18,R15
VCCIO5	W13,V16,AA17,AB14,Y10
VCCIO6	AA7,V6,W3,T2,R5,AB4
VCCIO7	C1,J3,N1,M4,H6,F2
VCCIO10	F12,T12
VCCX	P12,M12,R11
VCC	H8,T8,R9,H10,P8,N7,J7,R7,K8,L7,P10,T10,J9,M8
VCCLDO	B7,B9,B5,B11,C4,C8

VDDHAQ1	K12
VDDHAQ0	H12
VDDAQ0_VDDDQ0	F7,D10,D6
VDDTQ0	E8,F9
VSS	K9,D8,A2,A3,A5,A7,A9,A11,A12,A22,AA2,AA12,AA22,AB9,AB19,B3,B12,B19,C3,C6,C10,C12,C16,D3,D4,D12,D13,E4,E5,E7,E9,E11,E20,F5,F11,F17,G5,G6,G7,G8,G9,G10,G12,G14,H1,H7,H9,H11,H21,J8,J10,J12,J18,K5,K7,K11,K15,L2,L8,L22,M7,M11,M19,N6,N8,N16,P3,P7,P9,P11,P13,R8,R10,R12,R20,T7,T9,T11,T17,U4,U14,V1,V11,V21,W8,W18,Y5,Y15

3.4.4 View of PG484F Pin Distribution

Figure 3-15 View of GW5AT-138 PG484F Pin Distribution (Top View)

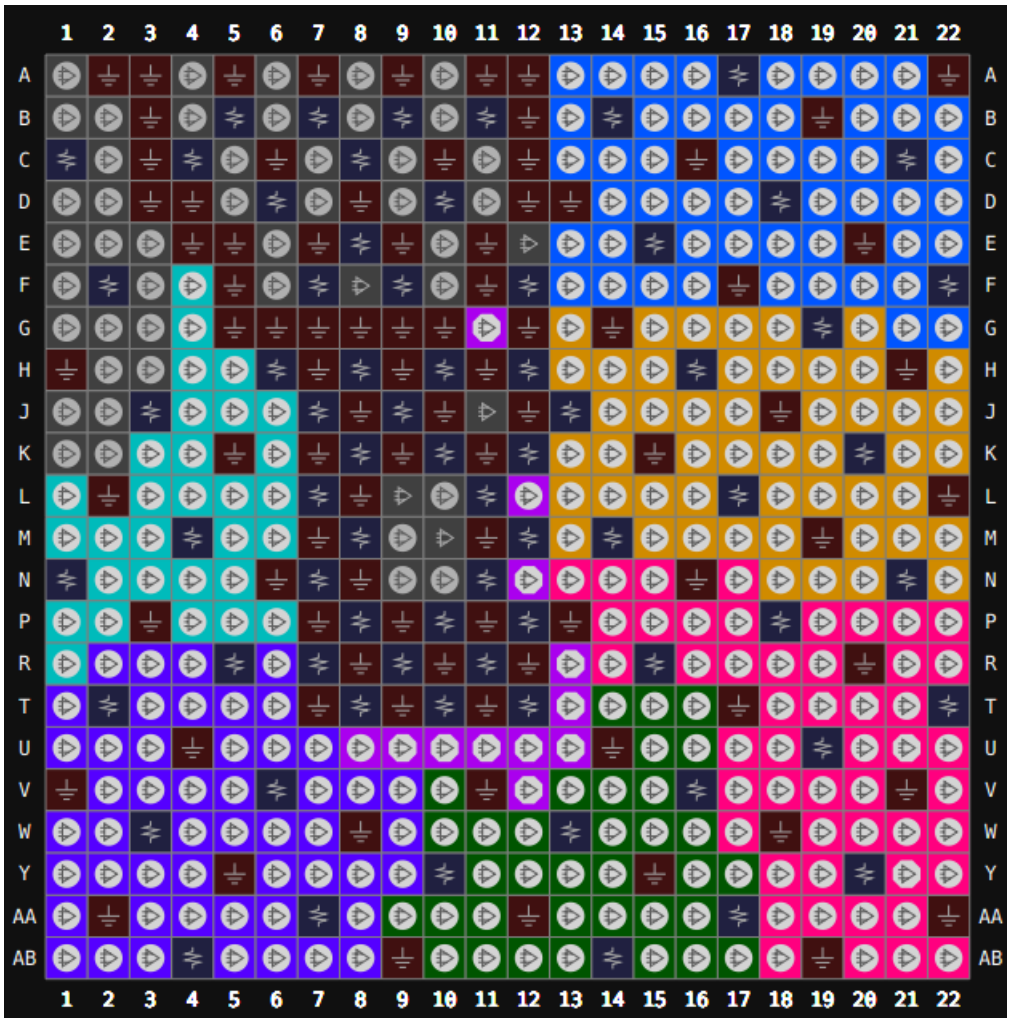


Table 3-15 Other Pins in GW5AT-138 PG484F

VCCIO2	C21,B14,A17,F22,E15,D18
VCCIO3	K20,H16,J13,G19,N21,L17
VCCIO4	Y20,R15,M14,T22,U19,P18
VCCIO5	Y10,W13,AA17,V16,AB14
VCCIO6	R5,V6,T2,W3,AA7,AB4

VCCIO7	M4,H6,C1,F2,N1,J3
VCCIO10	F12,T12
VCCX	M12,P12,R11
VCC	L11,K8,P8,H8,N11,M8,P10,T8,J9,R7,R9,N7,H10,T10
VCCLDO	C8,B7,B9,B11,C4,B5
VDDXM	K10
VDDAM_VDDDM	J7,L7
VDDHAQ0	K12,H12
VDDAQ0	D10,D6,F7
VDDTQ0	E8,F9
VSS	K9,D8,A2,A3,A5,A7,A9,A11,A12,A22,AA2,AA12,AA22,AB9,AB19,B3,B12,B19,C3,C6,C10,C12,C16,D3,D4,D12,D13,E4,E5,E7,E9,E11,E20,F5,F11,F17,G5,G6,G7,G8,G9,G10,G12,G14,H1,H7,H9,H11,H21,J8,J10,J12,J18,K5,K7,K11,K15,L2,L8,L22,M7,M11,M19,N6,N8,N16,P3,P7,P9,P11,P13,R8,R10,R12,R20,T7,T9,T11,T17,U4,U14,V1,V11,V21,W8,W18,Y5,Y15

3.4.5 View of PG676A Pin Distribution

Figure 3-16 View of GW5AT-138 PG676A Pin Distribution (Top View)

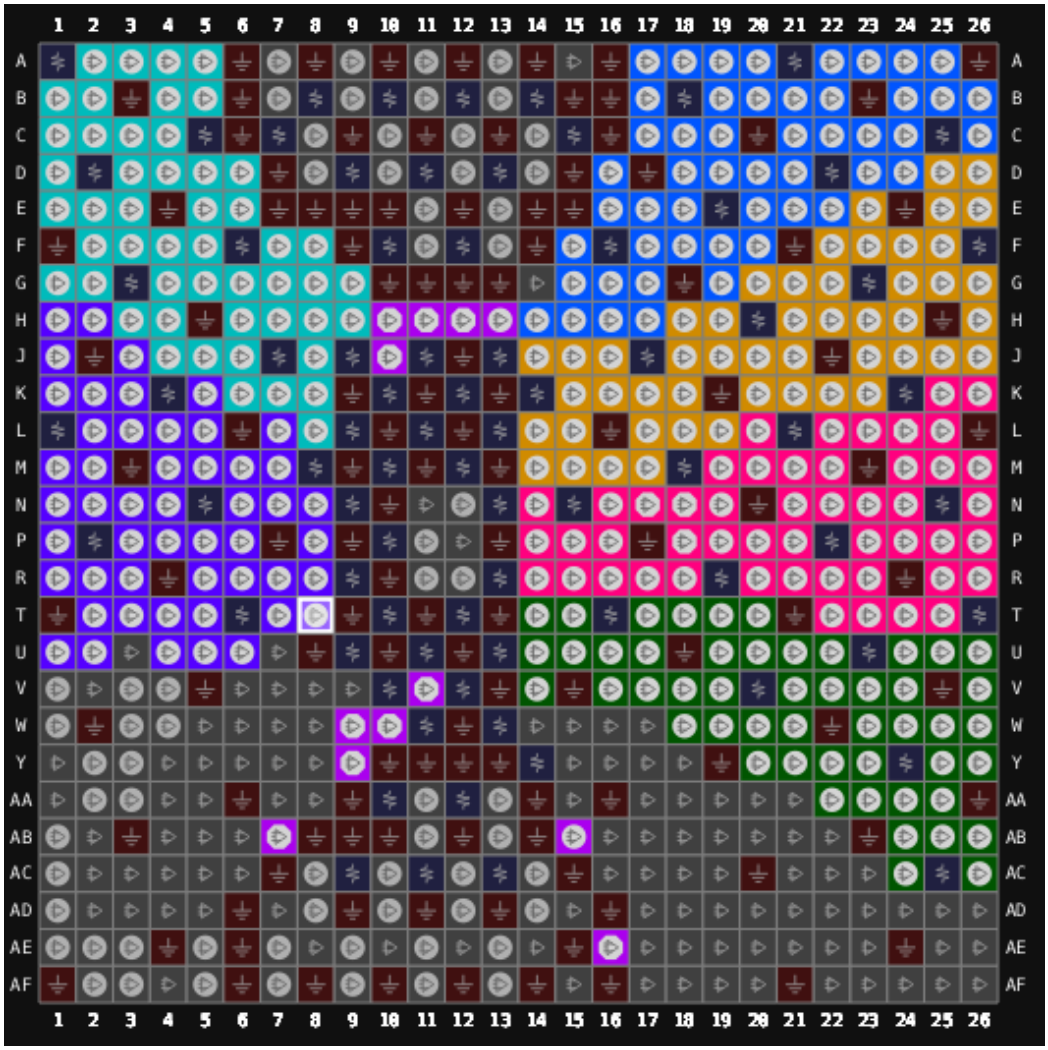


Table 3-16 Other Pins in GW5AT-138 PG676A

VCCIO2	E19,C25,A21,D22,F16,B18
VCCIO3	G23,K14,M18,H20,F26,J17
VCCIO4	L21,P22,N15,K24,N25,R19
VCCIO5	Y24,T16,U23,V20,AC25,T26
VCCIO6	L1,P2,N5,T6,K4,M8
VCCIO7	J7,D2,A1,G3,C5,F6
VCCIO10	Y14,W11
VCCX	N9,L9,J9
VCC	V12,V10,T12,L13,T10,L11,K12,M10,U11,K10,J11,P10,J13
VCCLDO	B12,B10,C7,C15,B14,B8
VDDXM	M12
VDDAM	N13,R13
VDDDM	U13,W13
VDDHAQ0_VDDHAQ1	U9,R9
VDDAQ0	AA12,AC11,AA10
VDDTQ0	AC13,AC9
VDDAQ1	F12,D9,F10
VDDTQ1	D13,D11
VSS	M11,AE15,B15,A10,A12,A14,A16,A26,A6,A8,AA14,AA16,AA26,AA6,AB10,AB12,AB14,AB23,AB3,AA9,AB8,AC15,AC20,AC7,AD11,AD13,AD6,AD9,AD16,AE24,AE4,AE6,AF1,AF10,AF12,AF14,AF16,AF21,AF6,AF8,B16,B23,B3,B6,C11,C13,C16,C20,C6,C9,D15,D17,D7,E10,E12,E14,E24,E4,E7,E8,E9,F1,F14,F21,F9,G10,G11,AB9,G13,Y12,G18,G12,H25,H5,J12,J2,J22,K11,K13,K19,K9,L10,L12,L16,L26,L6,M13,M23,M3,M9,N10,N20,P13,P17,P7,P9,R10,R24,R4,T1,T11,T13,T21,T9,U10,U12,U18,U8,V15,V25,V5,E15,W12,W2,W22,Y11,Y10,Y13,Y19,V13

3.4.6 View of UG324A Pin Distribution

Figure 3-17 View of GW5AT-138 UG324A Pin Distribution (Top View)

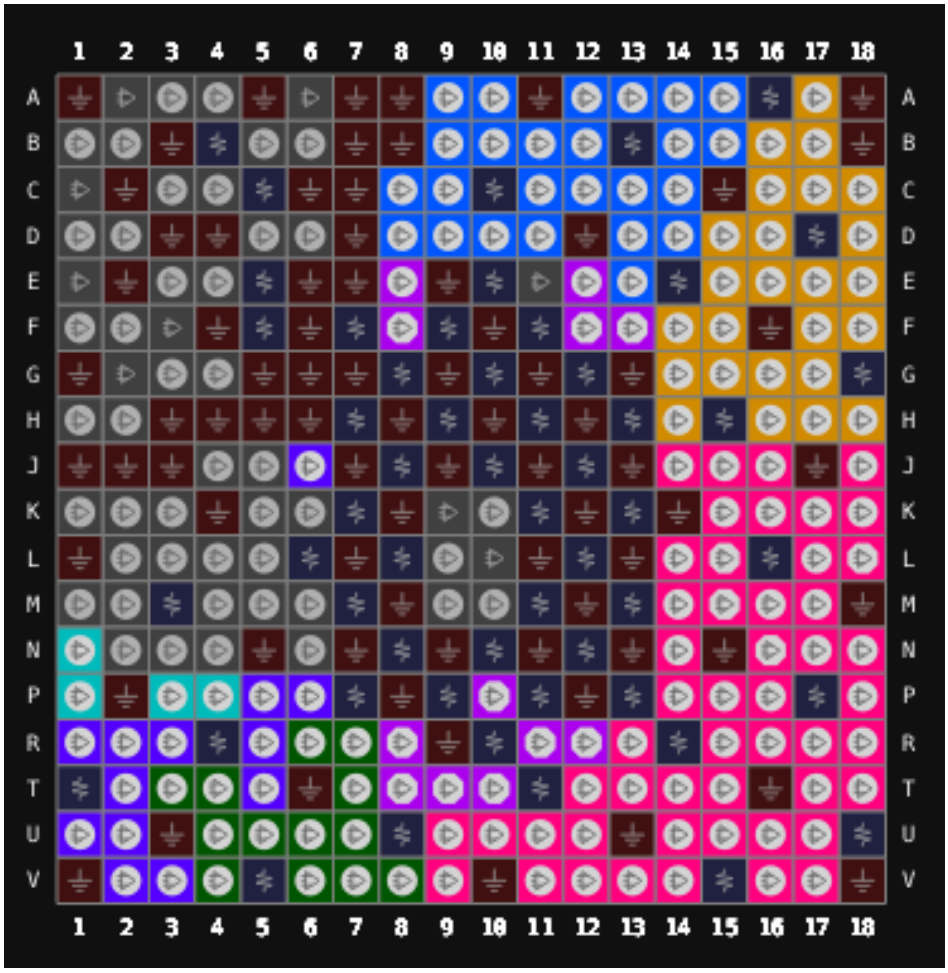


Table 3-17 Other Pins in GW5AT-138 UG324A

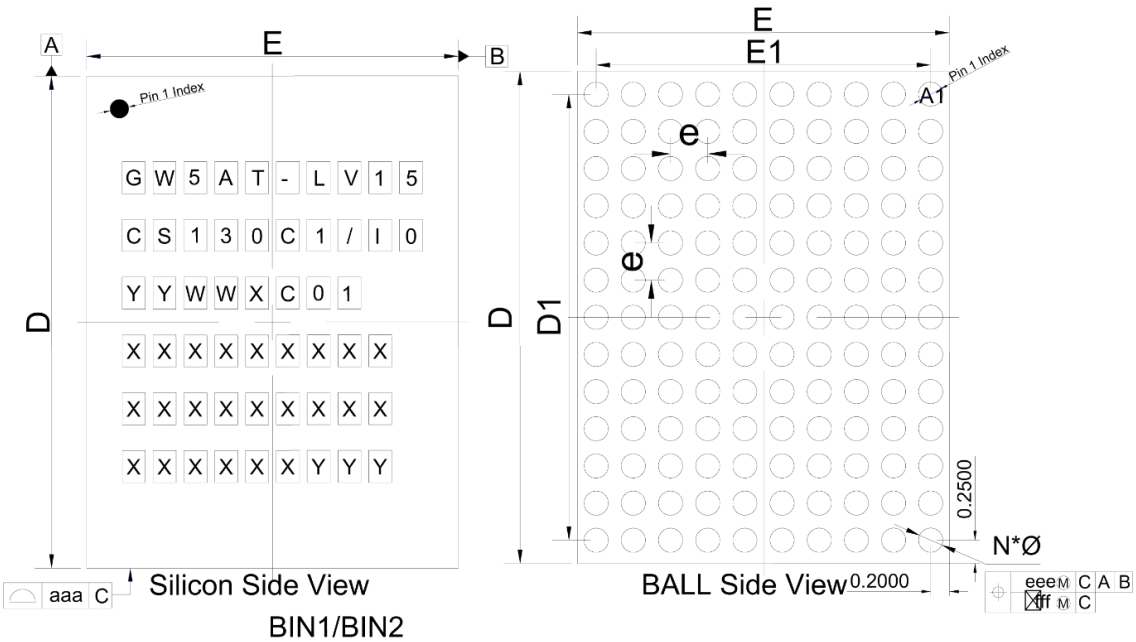
VCCIO2	A16,C10,D17,B13
VCCIO3	H15,G18,E14
VCCIO4	T11,P17,V15,R14,L16,U8,U18
VCCIO5	T1,V5
VCCIO6	P7,R4
VCCIO7	L6,M3
VCCIO10	E10,R10
VCCX	K13,M13,P13
VCC	P9,K7,L12,N8,N10,F9,G8,H7,P11,F7,L8,K11,M7,J8, H9,M11,J12,N12
VCCLDO	H13
VDDXM	J10
VDDAM_VDDDM	F11,H11,G10
VDDHAQ0	G12
VDDAQ0	E5,F5
VDDTQ0	B4,C5

VSS	A1,A5,A7,A8,A11,A18,B3,B7,B8,B18,C2,C6,C7,C15, D3,D4,D7,D12,E2,E6,E7,E9,F4,F6,F10,F16,G1,G5,G 6,G7,G9,G11,G13,H3,H4,H5,H6,H8,H10,H12,J1,J2,J 3,J7,J11,J13,J17,K4,K8,K12,K14,L1,L7,L11,L13,M8, M12,M18,N5,N7,N9,N11,N13,N15,P2,P8,P12,R9,T6, T16,U3,U13,V1,V10,V18,J9

4 Package Diagram

4.1 CS130/CS130F Package Outline (4.0mm x 5.3mm, GW5AT-15)

Figure 4-1 Package Outline CS130/CS130F (GW5AT-15)



ITEM	SYMBOL	COMMON DIMENSIONS
TOTAL THICKNESS	A	605±56um
SOLDER BALL HEIGHT	A1	206±20um
PI+RDL+UBM THICKNESS	A2	44±11um
EMC+BackSide Coating THICKNESS	A3	355±25um
PACKAGE SIZE	E*D	4000*5300±50um
BALL DIAMETER BEFORE REFLOW	Øb	250±20um
BALL DIAMETER AFTER REFLOW	Ø	260±20um
UBM PAD OPENING		210um
BALL PITCH	e	400um
BALL COUNT	N	130ea
EDGE BALL CENTER TO CENTER	E1	3600um
	D1	4800um
PACKAGE EDGE TOLERANCE	aaa	0.10
EMC FLATNESS	bbb	0.10
COPLANARITY	ddd	0.08
BALL OFFSET (PACKAGE)	eee	0.15
BALL OFFSET (BALL)	fff	0.05
SOLDER BALL MATERIAL		SAC305 ,96.5%Sn,3%Ag,0.5%Cu

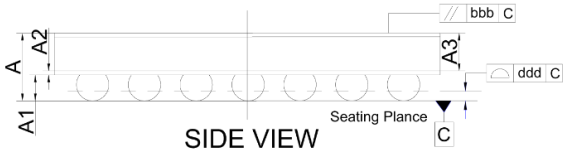
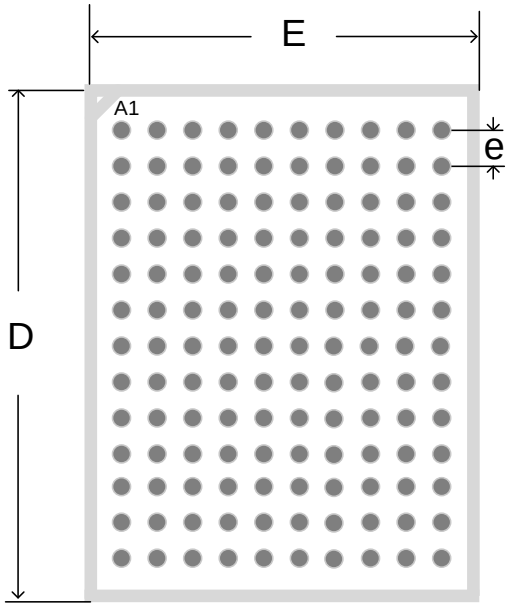
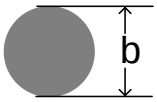


Figure 4-2 Recommended PCB Layout CS130/CS130F (GW5AT-15)



TOP VIEW

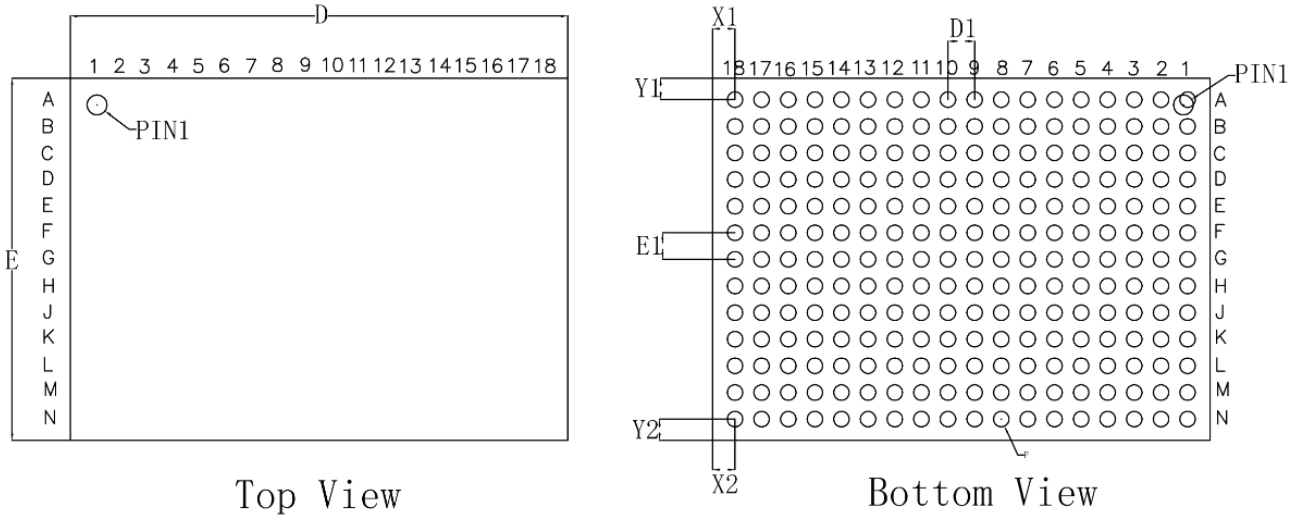


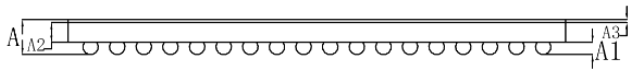
Unit:mm

D	5.30
E	4.00
e	0.40
b	0.20

4.2 CS234 Package Outline (7.4mm x 5.4mm, GW5AT-60)

Figure 4-3 Package Outline CS234 (GW5AT-60)





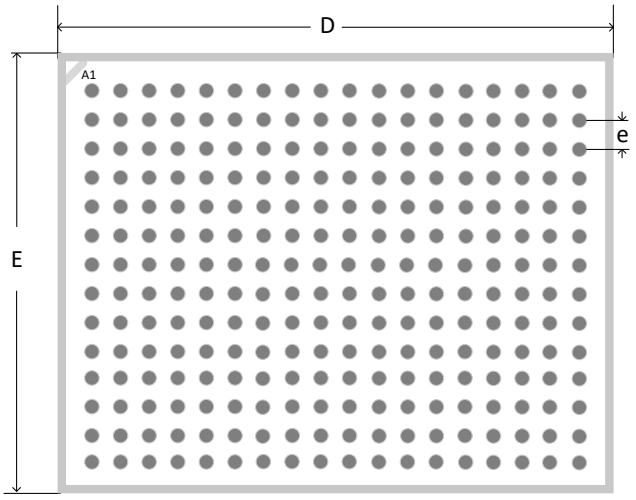
Side View

Notch

Unit: mm

		NO.	Mean	Tolerance
Top Thickness		A	0.525	±0.0375
Ball Height		A1	0.185	±0.020
Wafer Thickness		A2	0.300	±0.0125
Backside Coating Thickness		A3	0.040	±0.005
PKG DIE Size	X	D	7.474	±0.025
	Y	E	5.444	±0.025
Ball Size After reflow		F	0.234	±0.020
Ball Pitch		D1	0.400	NA
		E1	0.400	NA
Ball center to die edge		X1	0.337	NA
		Y1	0.322	NA
		X2	0.337	NA
		Y2	0.322	NA

Figure 4-4 Recommended PCB Layout CS234 (GW5AT-60)

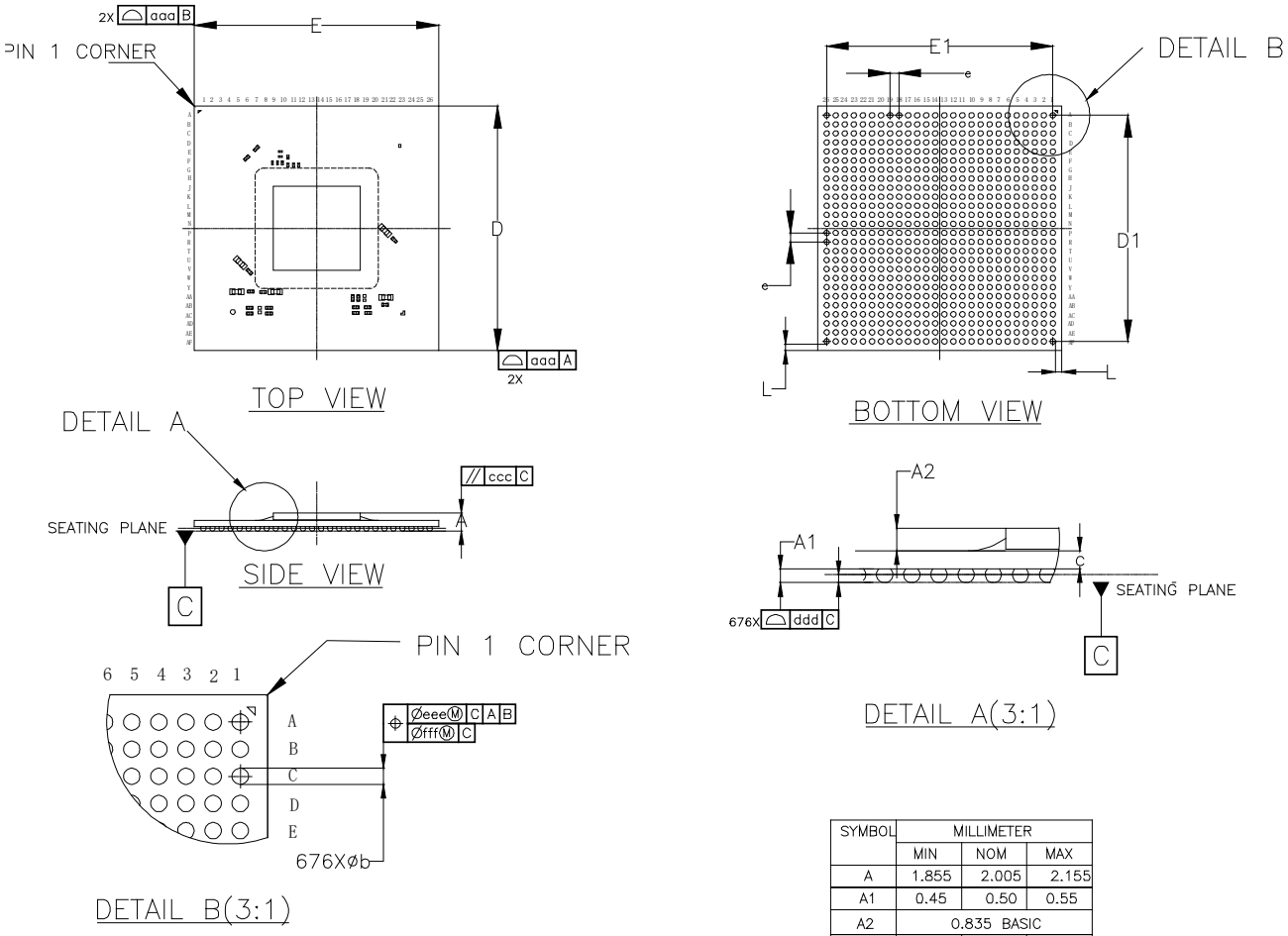


Unit:mm

D	7.474
E	5.444
e	0.40
b	0.20

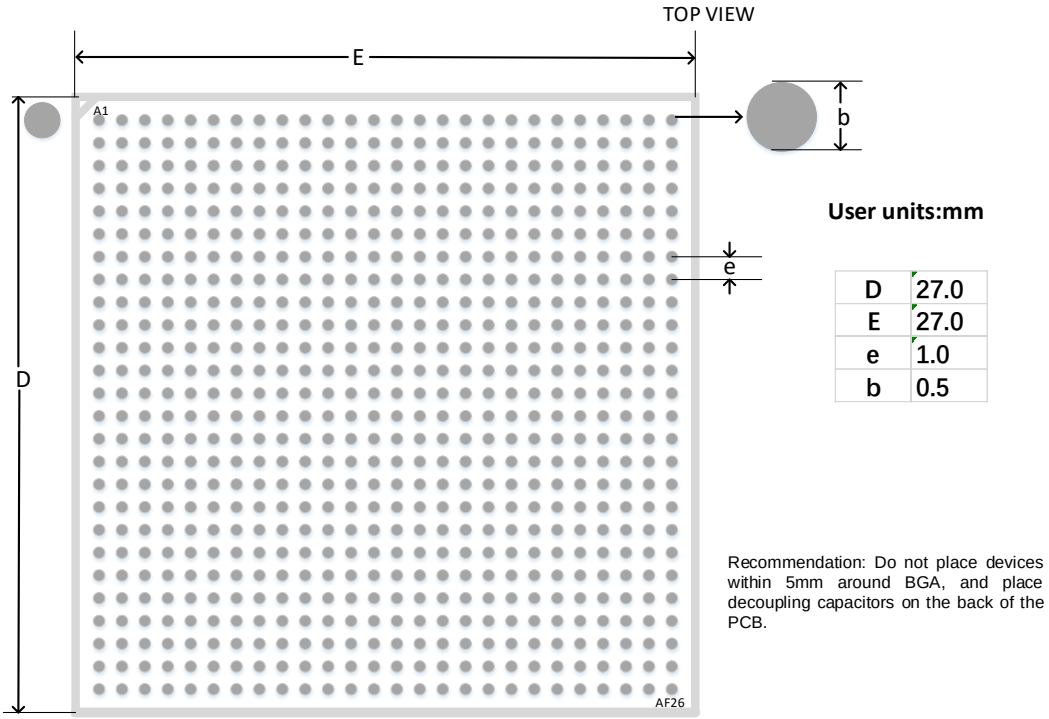
4.3 FPG676A (Flip Chip) Package Outline (27mm x 27mm, GW5AT-138)

Figure 4-5 Package Outline FPG676A (Flip Chip, GW5AT-138)



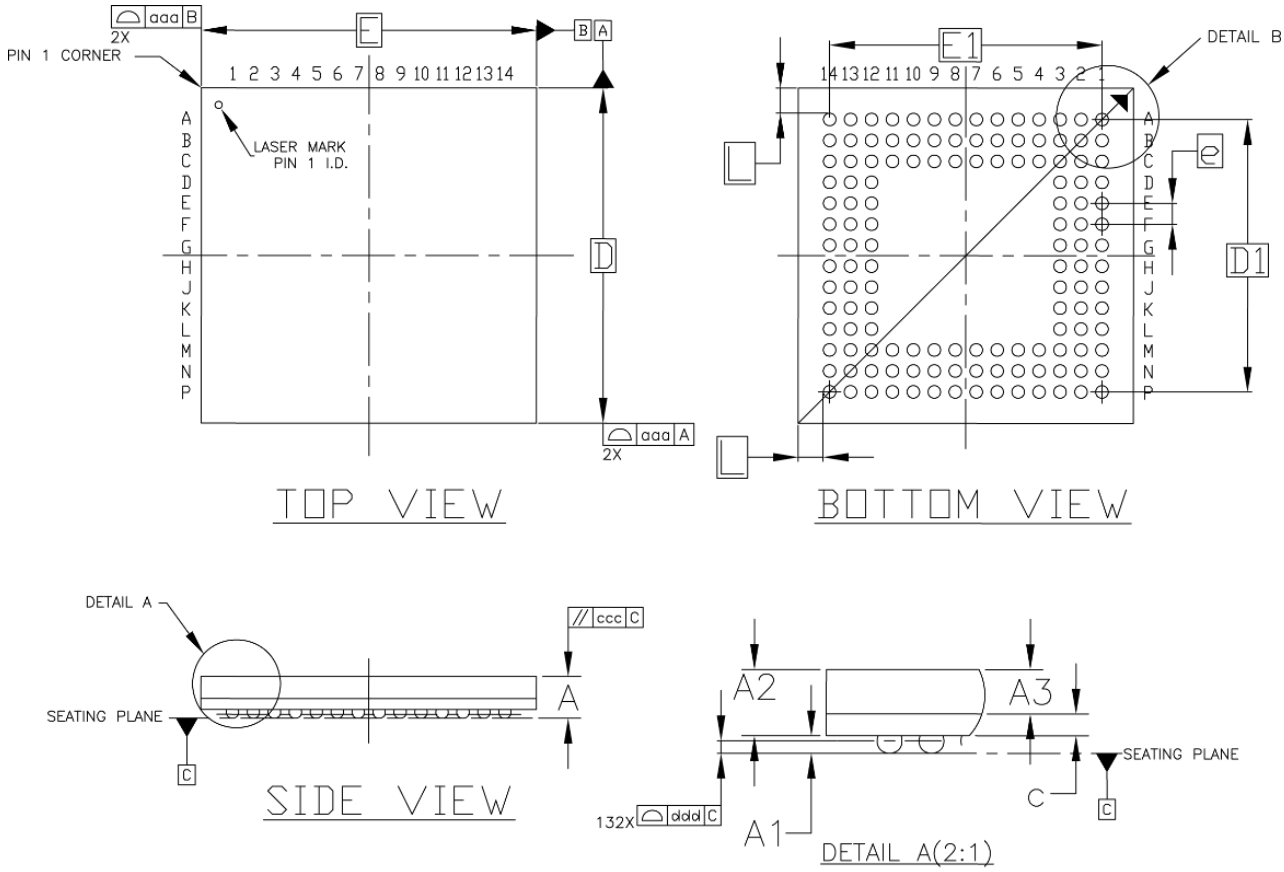
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.855	2.005	2.155
A1	0.45	0.50	0.55
A2	0.835 BASIC		
c	0.60	0.67	0.74
D	26.90	27.00	27.10
D1	25.00 BASIC		
E	26.90	27.00	27.10
E1	25.00 BASIC		
L	0.70 REF		
e	1.00 BASIC		
b	0.55	0.60	0.65
aaa	0.20		
ccc	0.25		
ddd	0.20		
eee	0.25		
fff	0.10		

Figure 4-6 Recommended PCB Layout FPG676A (Flip Chip, GW5AT-138)



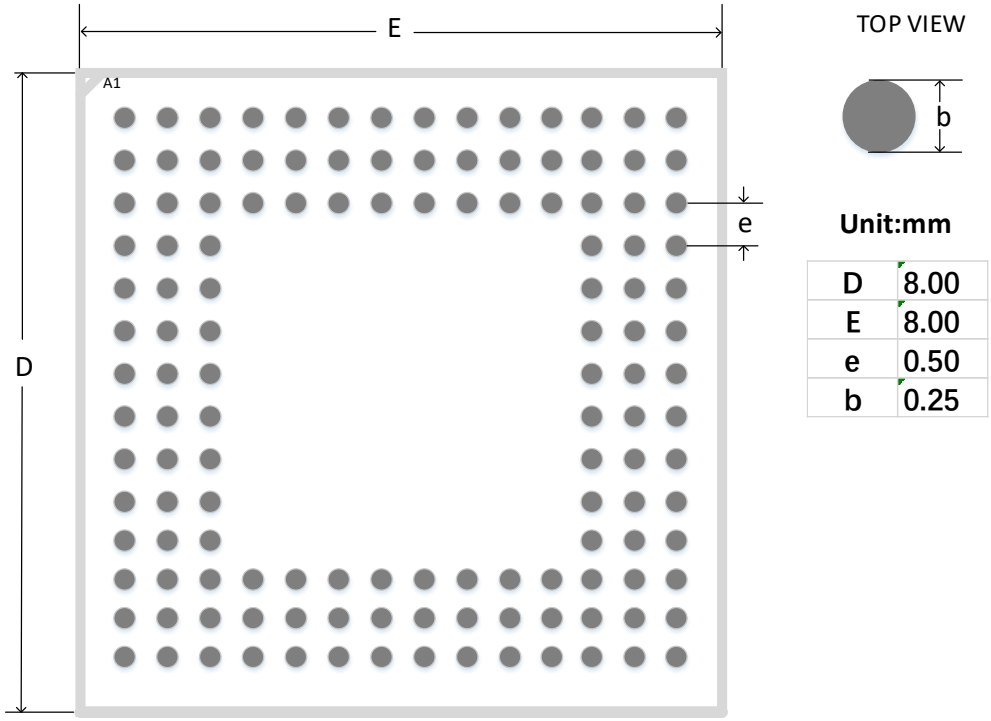
4.4 MG132 Package Outline (8mm x 8mm, GW5AT-15)

Figure 4-7 Package Outline MG132 (GW5AT-15)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.19	1.27	1.35
A1	0.16	0.21	0.26
A2	1.01	1.06	1.11
A3	BASIC		
c	0.32	0.36	0.40
D	7.90	8.00	8.10
D1	6.50 BASIC		
E	7.90	8.00	8.10
E1	6.50 BASIC		
e	0.50 BASIC		
b	0.25	0.30	0.35
L	0.60 REF		
aaa	0.15		
ccc	0.08		
ddd	0.08		
eee	0.15		
fff	0.05		

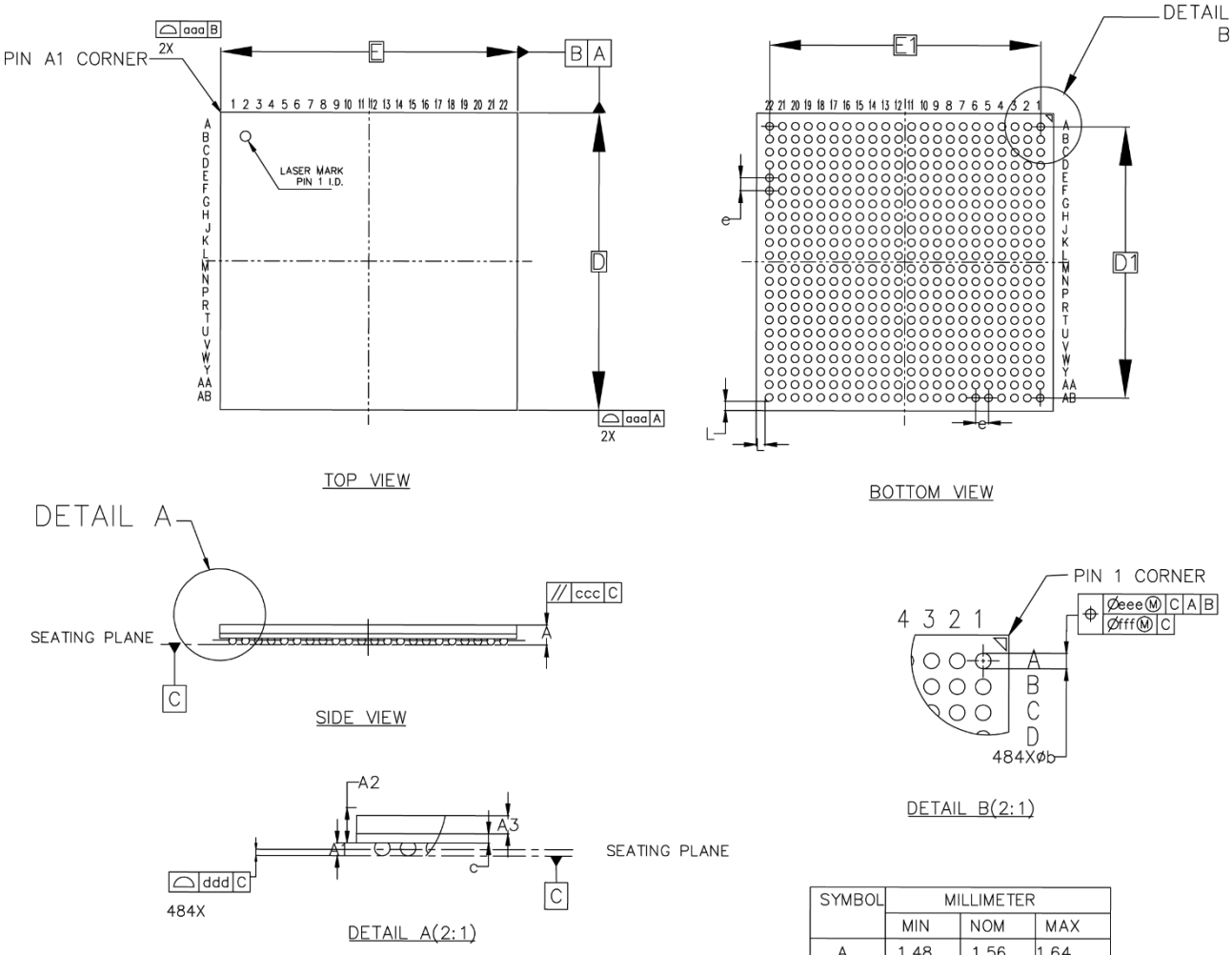
Figure 4-8 Recommended PCB Layout MG132 (GW5AT-15)



D	8.00
E	8.00
e	0.50
b	0.25

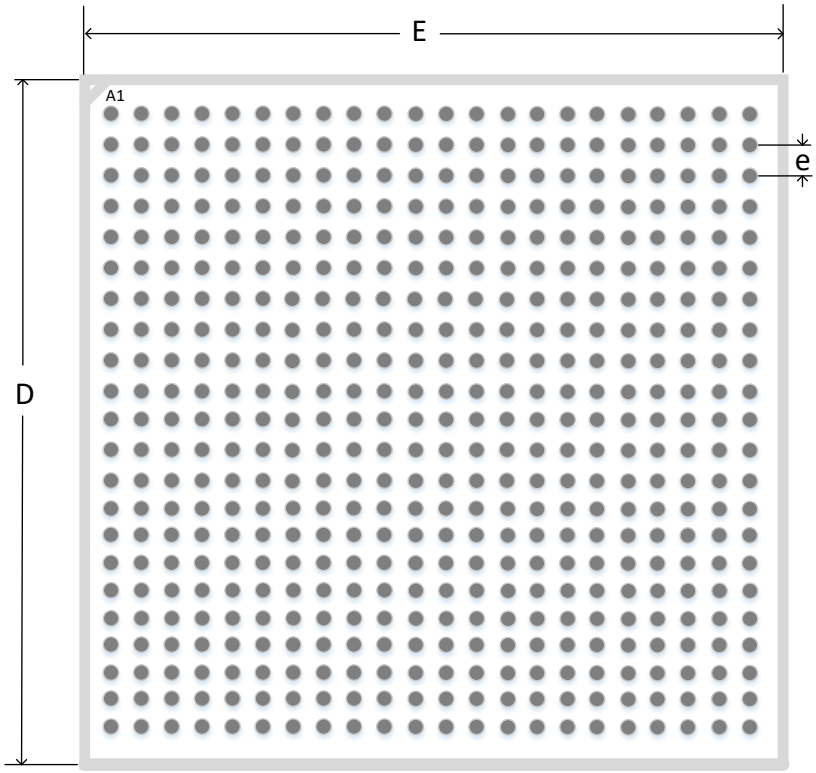
4.5 PG484 Package Outline (23mm x 23mm, GW5AT-138)

Figure 4-9 Package Outline PG484 (GW5AT-138)



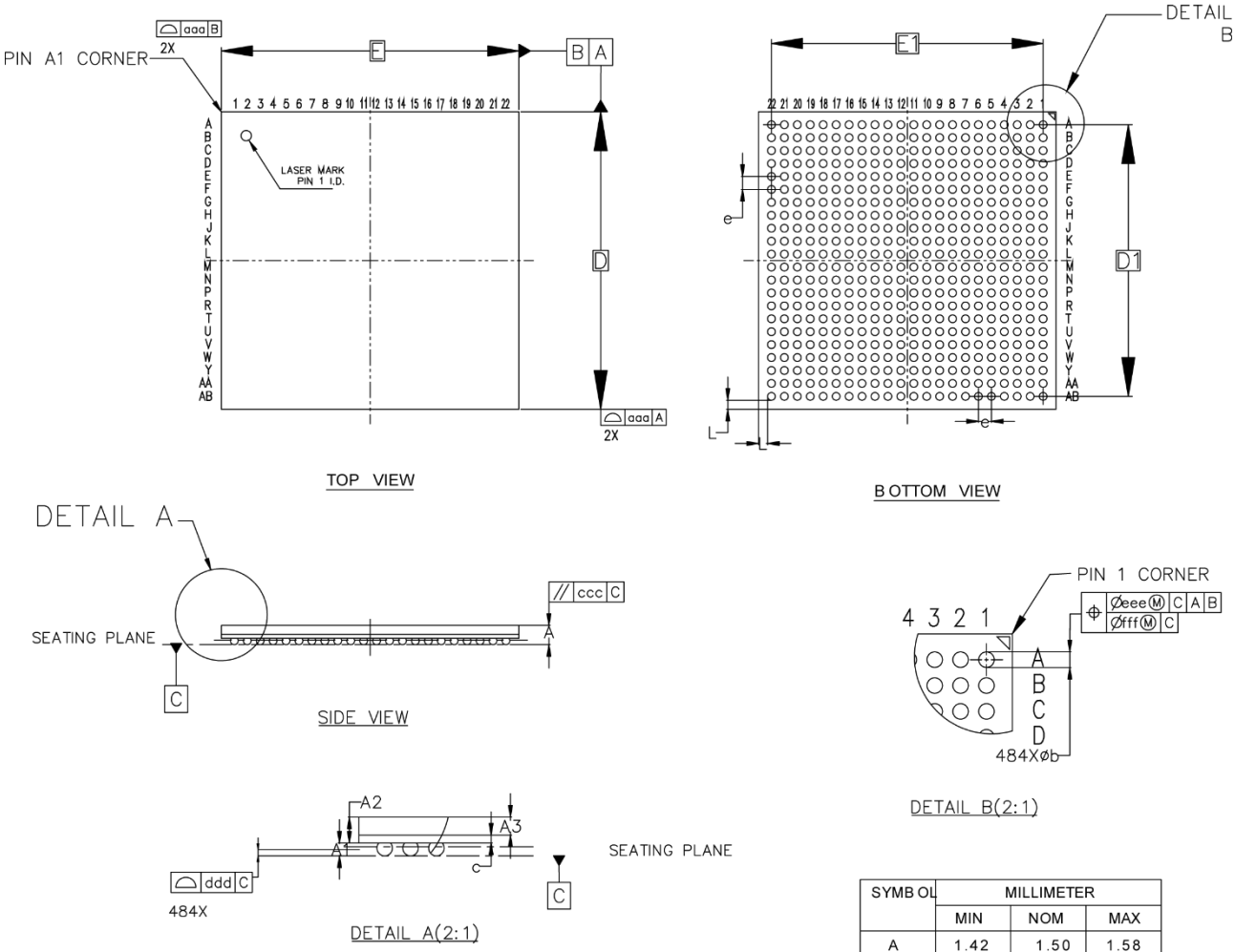
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.48	1.56	1.64
A1	0.45	0.50	0.55
A2	1.01	1.06	1.11
A3	0.70 BASIC		
c	0.32	0.36	0.40
D	22.90	23.00	23.10
D1	21.00 BASIC		
E	22.90	23.00	23.10
E1	21.00 BASIC		
e	1.00 BASIC		
L	0.70 REF		
b	0.55	0.60	0.65
aaa	0.20		
ccc	0.15		
ddd	0.20		
eee	0.18		
fff	0.10		

Figure 4-10 Recommended PCB Layout PG484 (GW5AT-138)



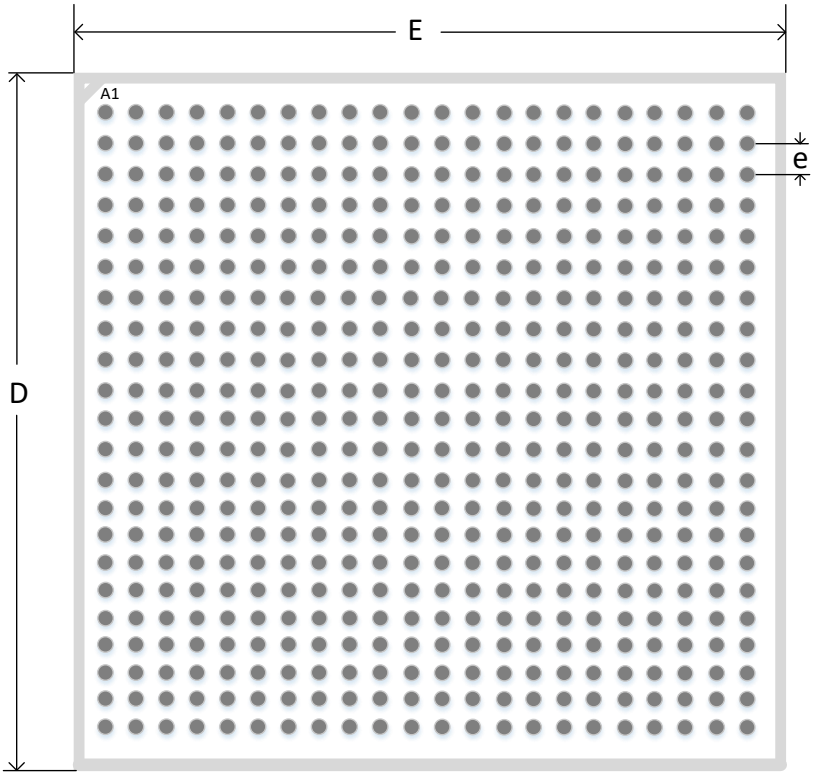
4.6 PG484A Package Outline (23mm x 23mm, GW5AT-60)

Figure 4-11 Package Outline PG484A (GW5AT-60)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.42	1.50	1.58
A1	0.45	0.50	0.55
A2	0.94	1.00	1.05
A3	0.70 BASIC		
c	0.26	0.30	0.34
D	22.90	23.00	23.10
D1	21.00 BASIC		
E	22.90	23.00	23.10
E1	21.00 BASIC		
e	1.00 BASIC		
L	0.70 REF		
b	0.55	0.60	0.65
aaa	0.20		
ccc	0.15		
ddd	0.20		
eee	0.18		
fff	0.10		

Figure 4-12 Recommended PCB Layout PG484A (GW5AT-60)

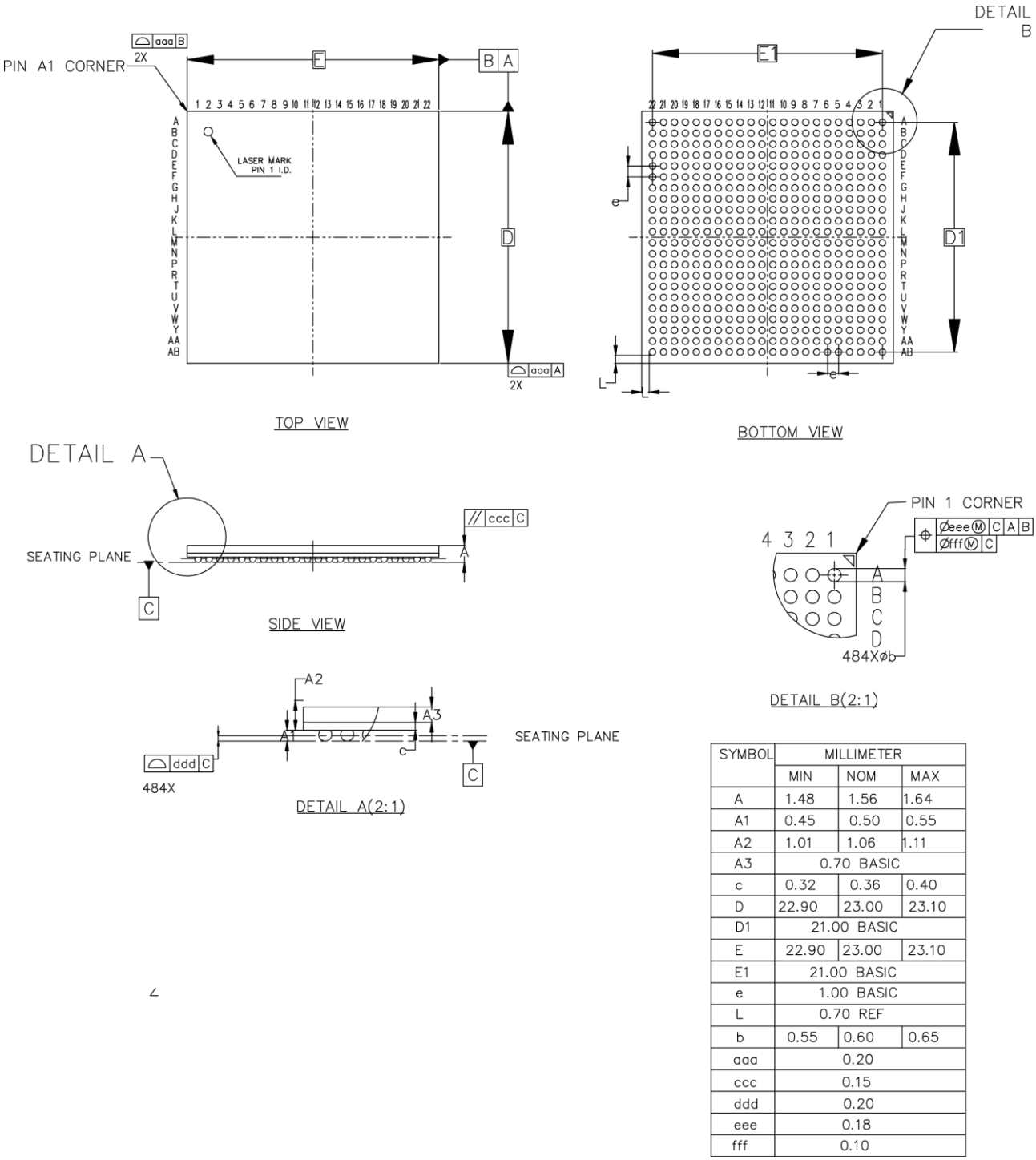


Unit:mm

D	23.00
E	23.00
e	1.00
b	0.50

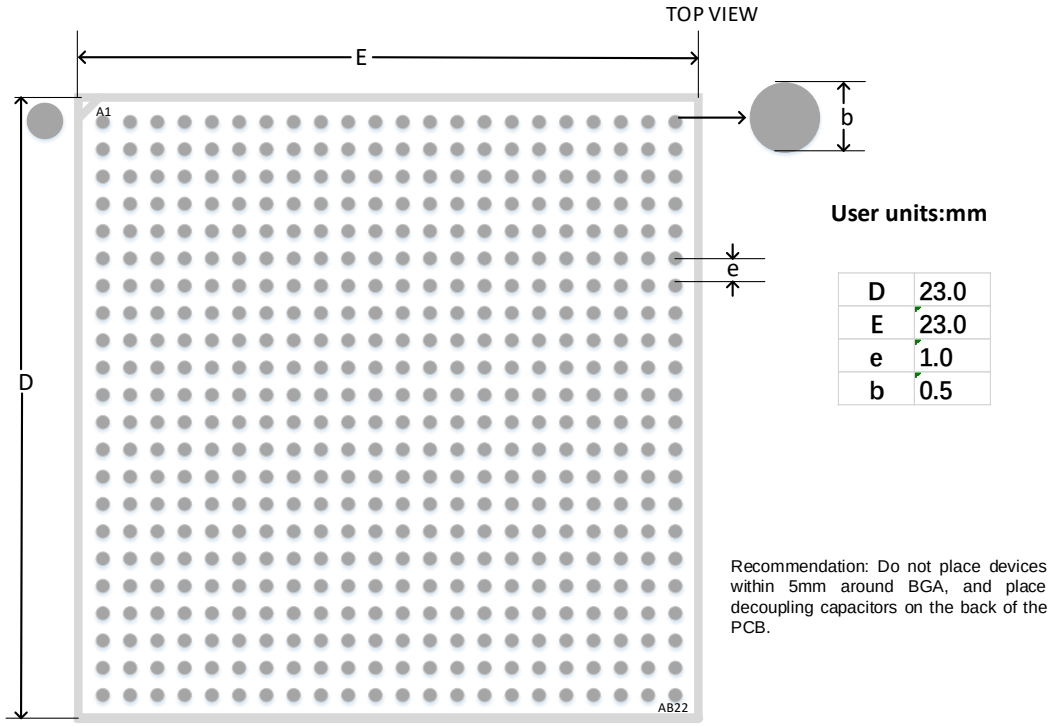
4.7 PG484A Package Outline (23mm x 23mm, GW5AT-138)

Figure 4-13 Package Outline PG484A (GW5AT-138)



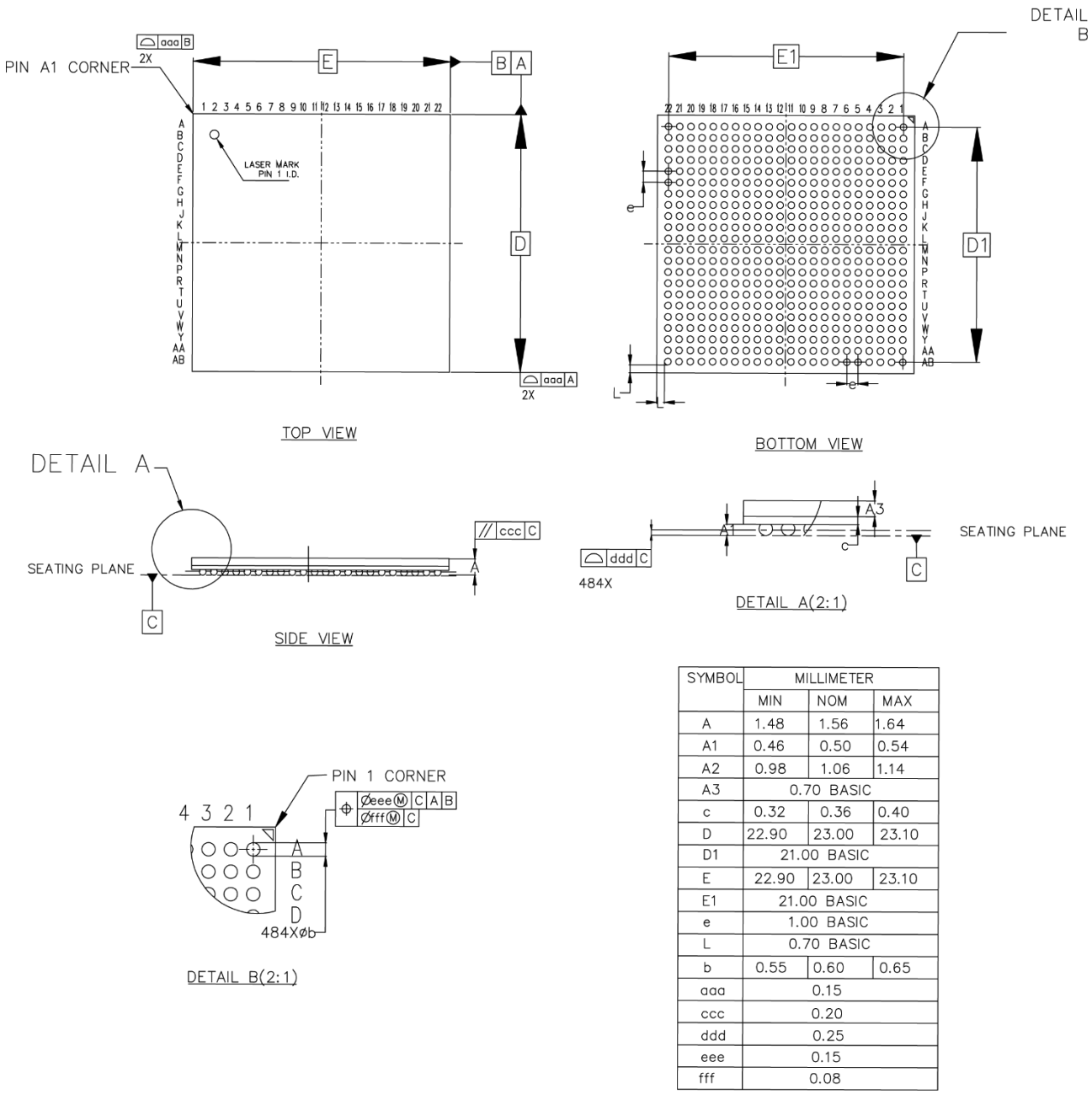
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.48	1.56	1.64
A1	0.45	0.50	0.55
A2	1.01	1.06	1.11
A3	0.70 BASIC		
c	0.32	0.36	0.40
D	22.90	23.00	23.10
D1	21.00 BASIC		
E	22.90	23.00	23.10
E1	21.00 BASIC		
e	1.00 BASIC		
L	0.70 REF		
b	0.55	0.60	0.65
aaa	0.20		
ccc	0.15		
ddd	0.20		
eee	0.18		
fff	0.10		

Figure 4-14 Recommended PCB Layout PG484A (GW5AT-138)



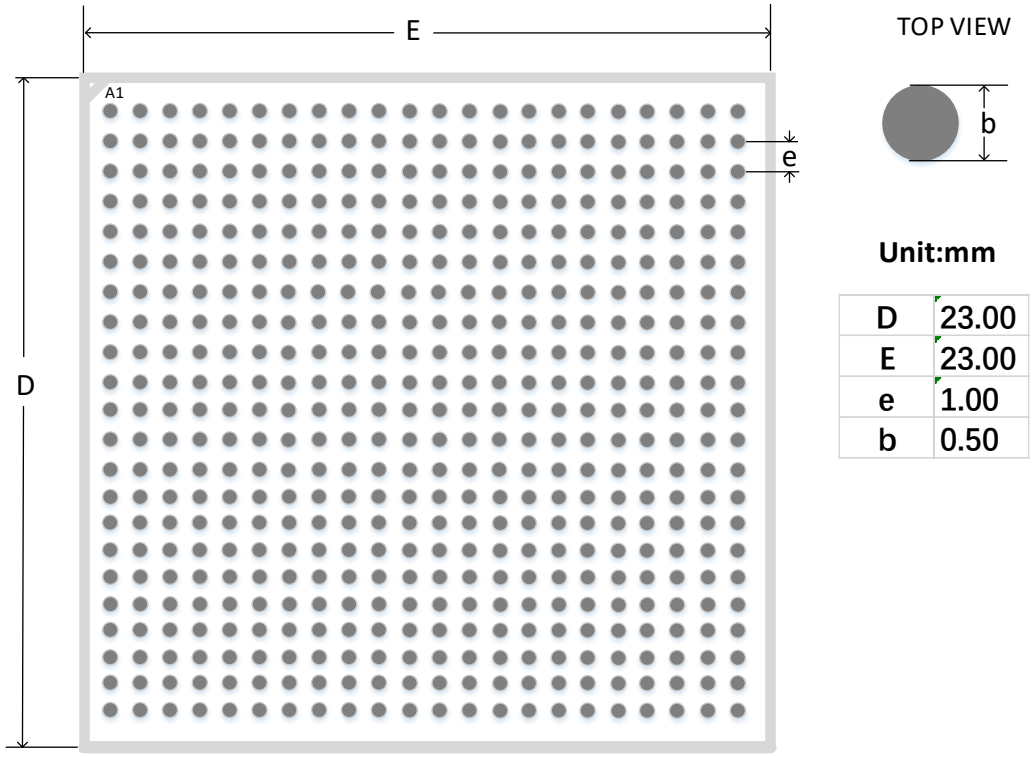
4.8 PG484F Package Outline (23mm x 23mm, GW5AT-138)

Figure 4-15 Package Outline PG484F (GW5AT-138)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.48	1.56	1.64
A1	0.46	0.50	0.54
A2	0.98	1.06	1.14
A3	0.70 BASIC		
c	0.32	0.36	0.40
D	22.90	23.00	23.10
D1	21.00 BASIC		
E	22.90	23.00	23.10
E1	21.00 BASIC		
e	1.00 BASIC		
L	0.70 BASIC		
b	0.55	0.60	0.65
aaa	0.15		
ccc	0.20		
ddd	0.25		
eee	0.15		
fff	0.08		

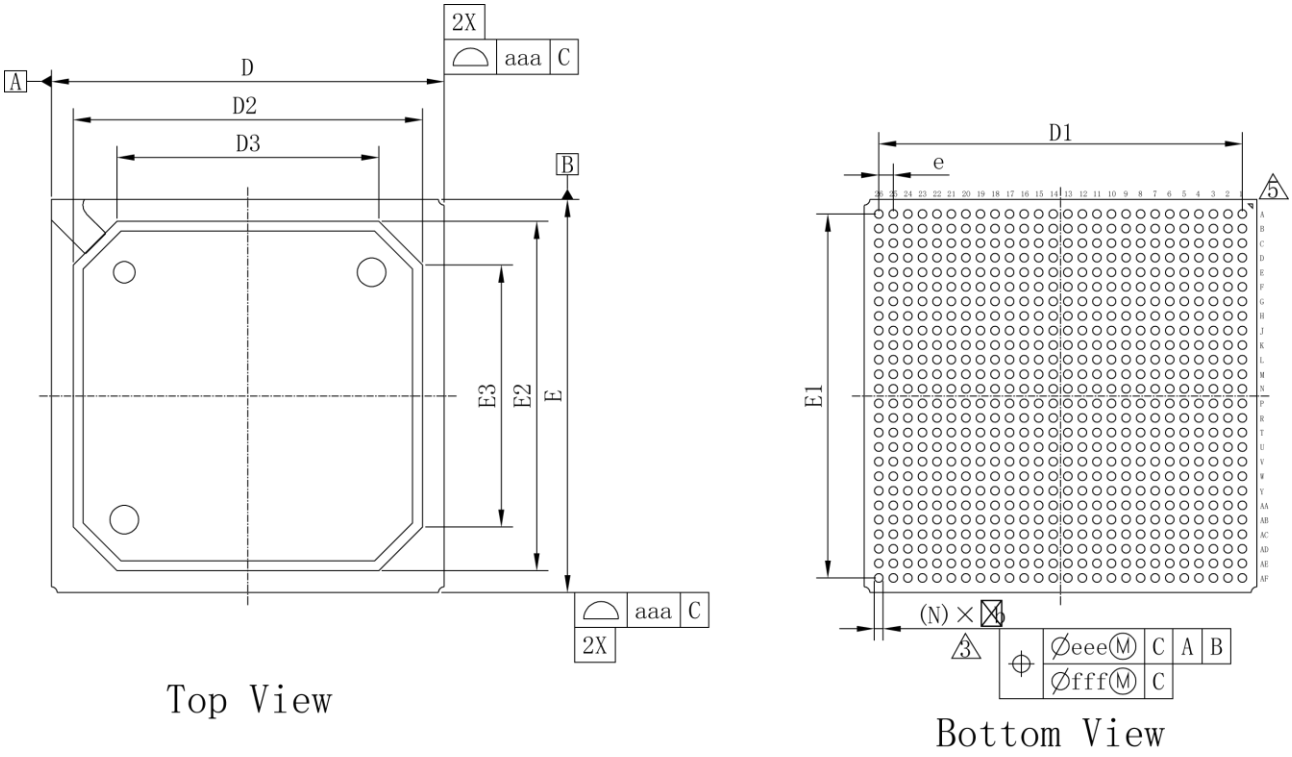
Figure 4-16 Recommended PCB Layout PG484F (GW5AT-138)



D	23.00
E	23.00
e	1.00
b	0.50

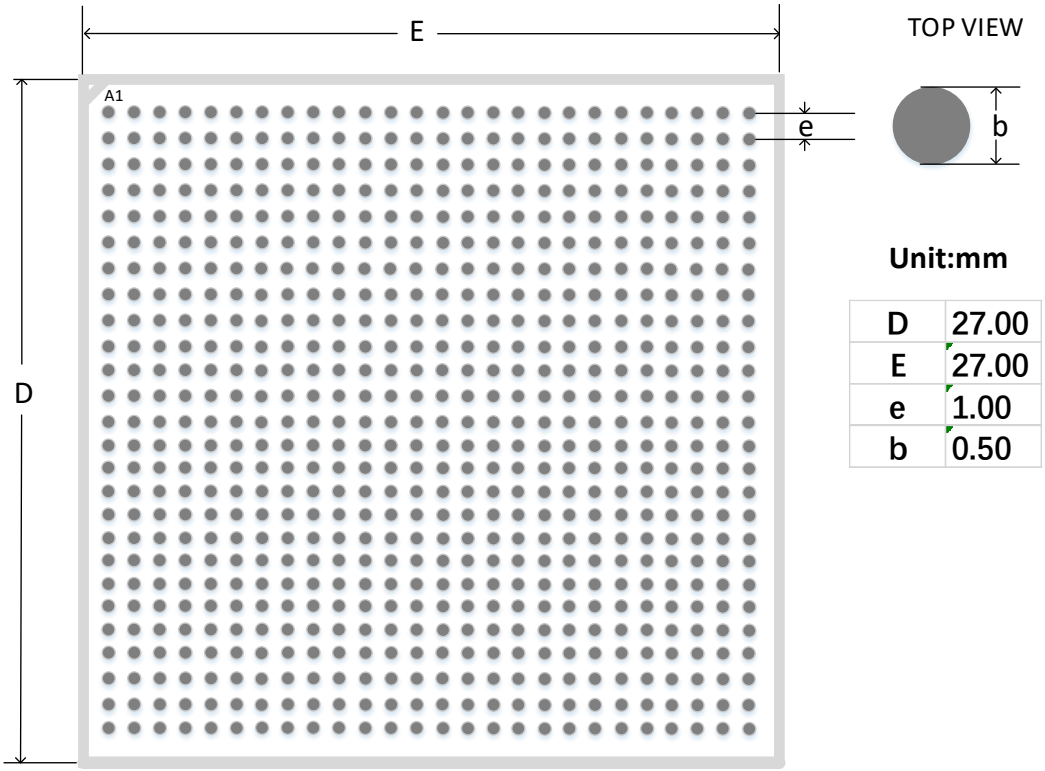
4.9 PG676A Package Outline (27mm x 27mm, GW5AT-138)

Figure 4-17 Package Outline PG676A (GW5AT-138)



symbol	Dimension in mm		
	MIN	NOM	MAX
A	2.080	2.230	2.380
A1	0.450	0.500	0.550
A2	1.120	1.170	1.220
c	0.510	0.560	0.610
D	26.800	27.000	27.200
D1	---	25.000	---
D2	23.800	24.000	24.200
D3	---	18.000	---
E	26.800	27.000	27.200
E1	---	25.000	---
E2	23.800	24.000	24.200
E3	---	18.000	---
e	---	1.000	---
b	0.550	0.600	0.650
aaa	0.200		
bbb	0.200		
ddd	0.250		
eee	0.250		
fff	0.100		
Ball Diam	0.600		
N	676		
MD/ME	26/26		

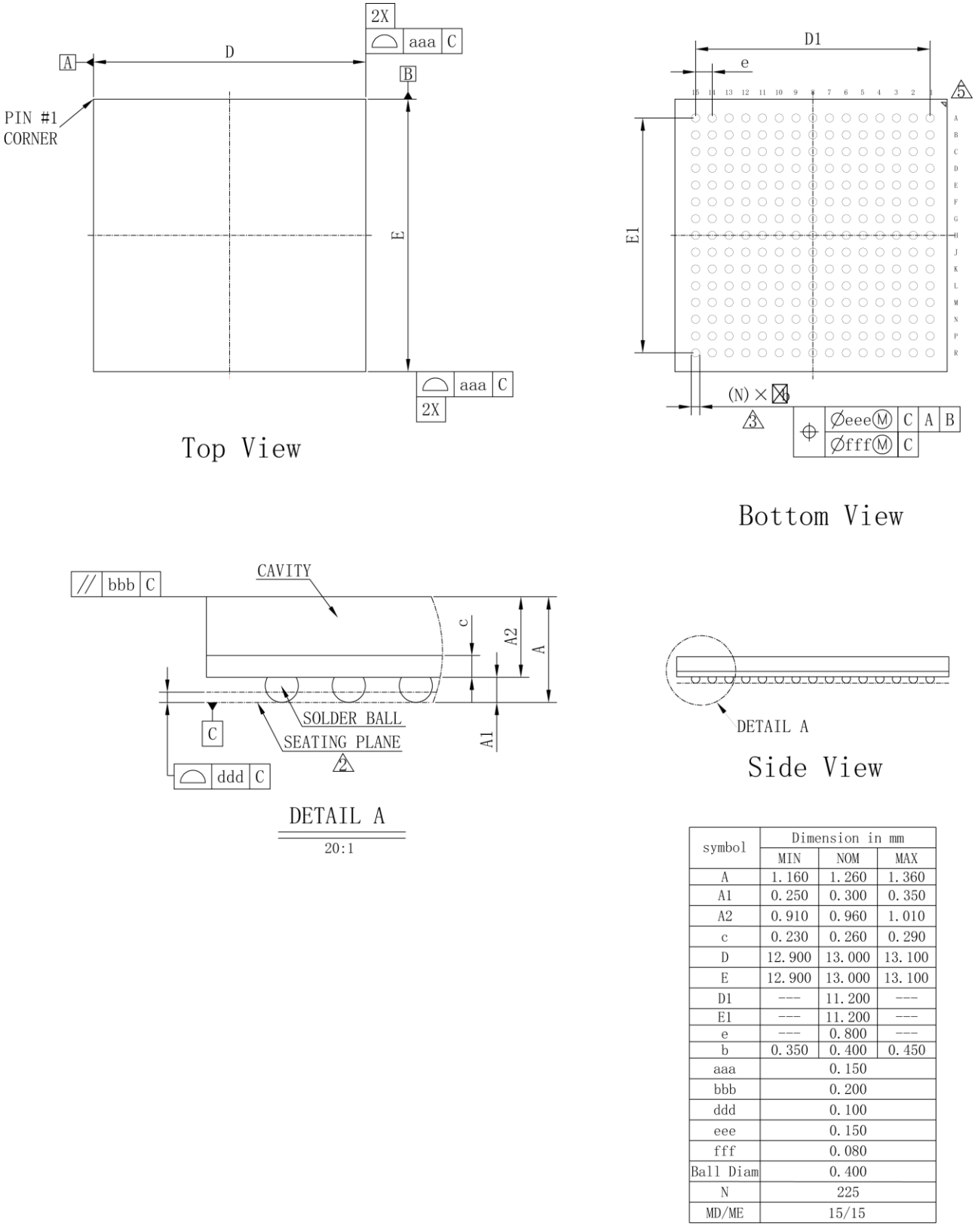
Figure 4-18 Recommended PCB Layout PG676A (GW5AT-138)



D	27.00
E	27.00
e	1.00
b	0.50

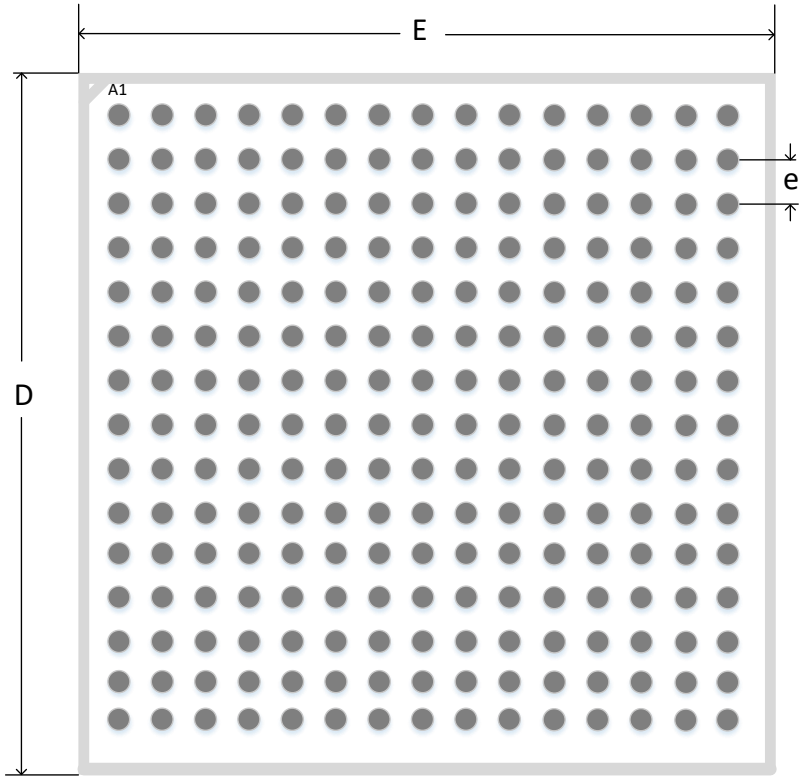
4.10 UG225 Package Outline (13mm x 13mm, GW5AT-60)

Figure 4-19 Package Outline UG225 (GW5AT-60)



symbol	Dimension in mm		
	MIN	NOM	MAX
A	1.160	1.260	1.360
A1	0.250	0.300	0.350
A2	0.910	0.960	1.010
c	0.230	0.260	0.290
D	12.900	13.000	13.100
E	12.900	13.000	13.100
D1	---	11.200	---
E1	---	11.200	---
e	---	0.800	---
b	0.350	0.400	0.450
aaa	0.150		
bbb	0.200		
ddd	0.100		
eee	0.150		
fff	0.080		
Ball Diam	0.400		
N	225		
MD/ME	15/15		

Figure 4-20 Recommended PCB Layout UG225 (GW5AT-60)

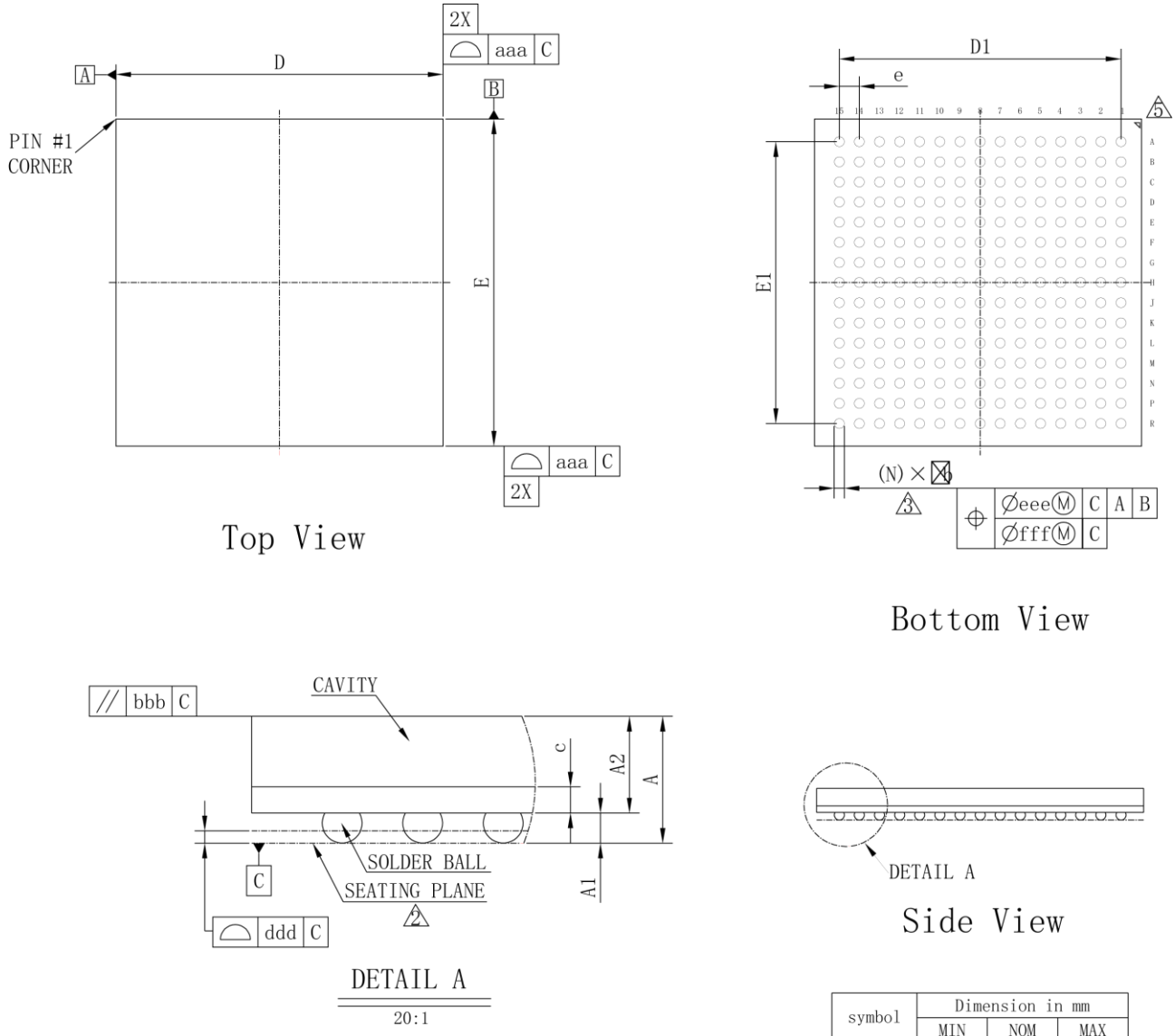


Unit:mm

D	13.00
E	13.00
e	0.80
b	0.35

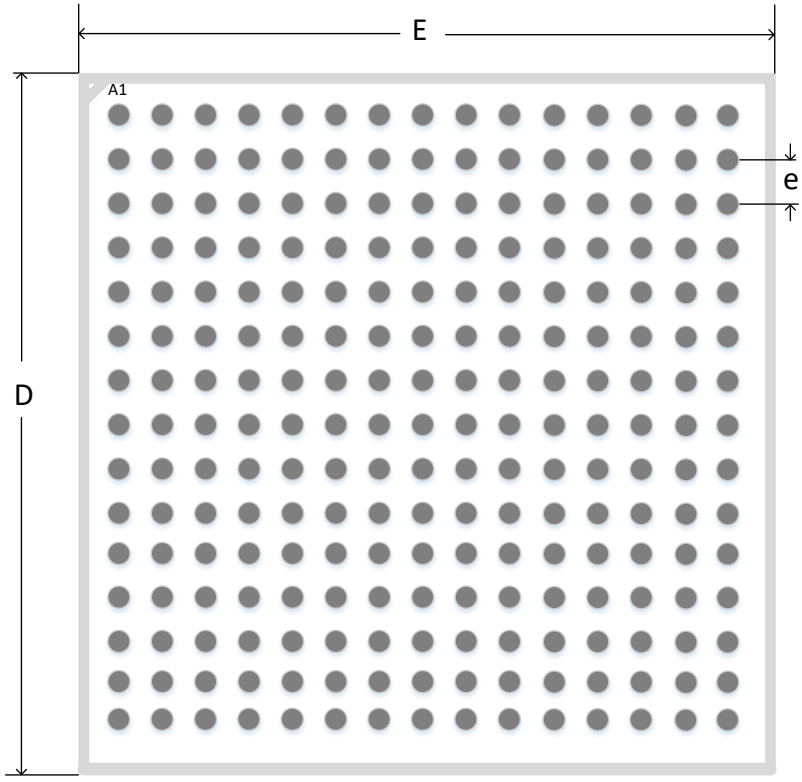
4.11 UG225H Package Outline (13mm x 13mm, GW5AT-60)

Figure 4-21 Package Outline UG225H (GW5AT-60)



symbol	Dimension in mm		
	MIN	NOM	MAX
A	1.160	1.260	1.360
A1	0.250	0.300	0.350
A2	0.910	0.960	1.010
c	0.230	0.260	0.290
D	12.900	13.000	13.100
E	12.900	13.000	13.100
D1	---	11.200	---
E1	---	11.200	---
e	---	0.800	---
b	0.350	0.400	0.450
aaa	0.150		
bbb	0.200		
ddd	0.100		
eee	0.150		
fff	0.080		
Ball Diam	0.400		
N	225		
MD/ME	15/15		

Figure 4-22 Recommended PCB Layout UG225H (GW5AT-60)

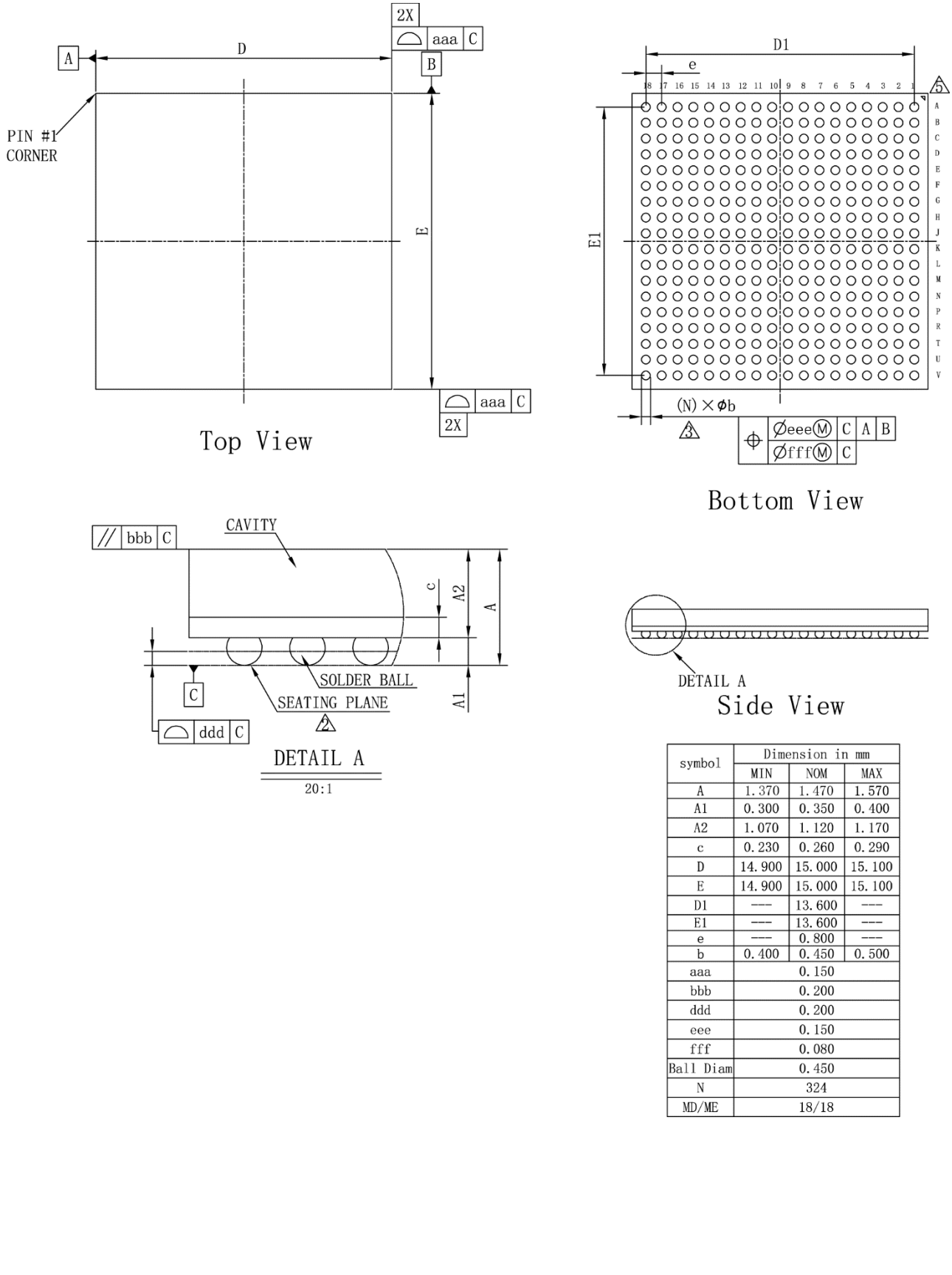


Unit:mm

D	13.00
E	13.00
e	0.80
b	0.35

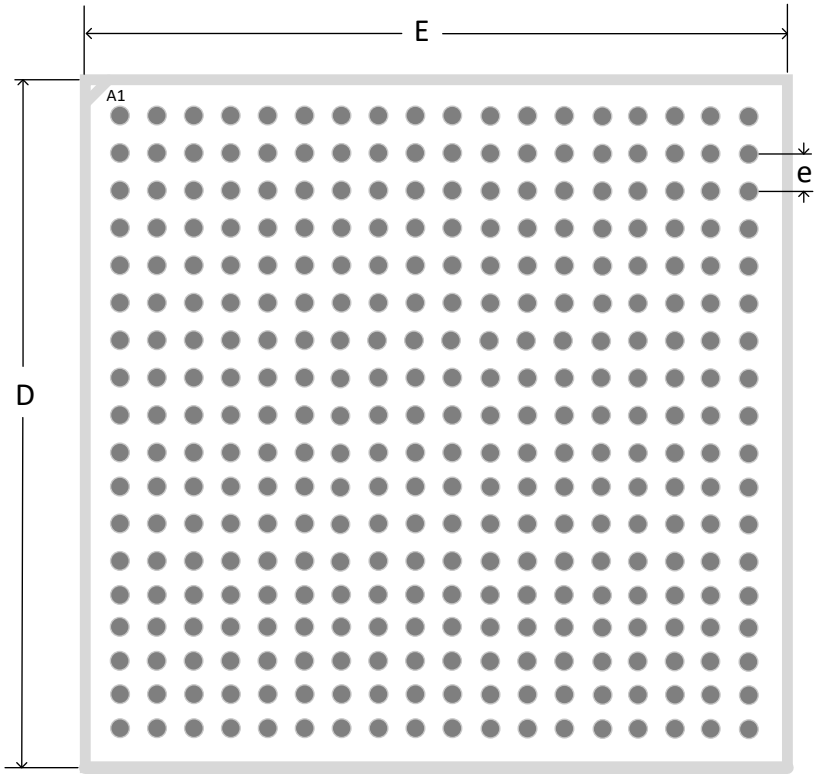
4.12 UG324 Package Outline (15mm x 15mm, GW5AT-60)

Figure 4-23 Package Outline UG324 (GW5AT-60)



symbol	Dimension in mm		
	MIN	NOM	MAX
A	1.370	1.470	1.570
A1	0.300	0.350	0.400
A2	1.070	1.120	1.170
c	0.230	0.260	0.290
D	14.900	15.000	15.100
E	14.900	15.000	15.100
D1	---	13.600	---
E1	---	13.600	---
e	---	0.800	---
b	0.400	0.450	0.500
aaa	0.150		
bbb	0.200		
ddd	0.200		
eee	0.150		
fff	0.080		
Ball Diam	0.450		
N	324		
MD/ME	18/18		

Figure 4-24 Recommended PCB Layout UG324 (GW5AT-60)

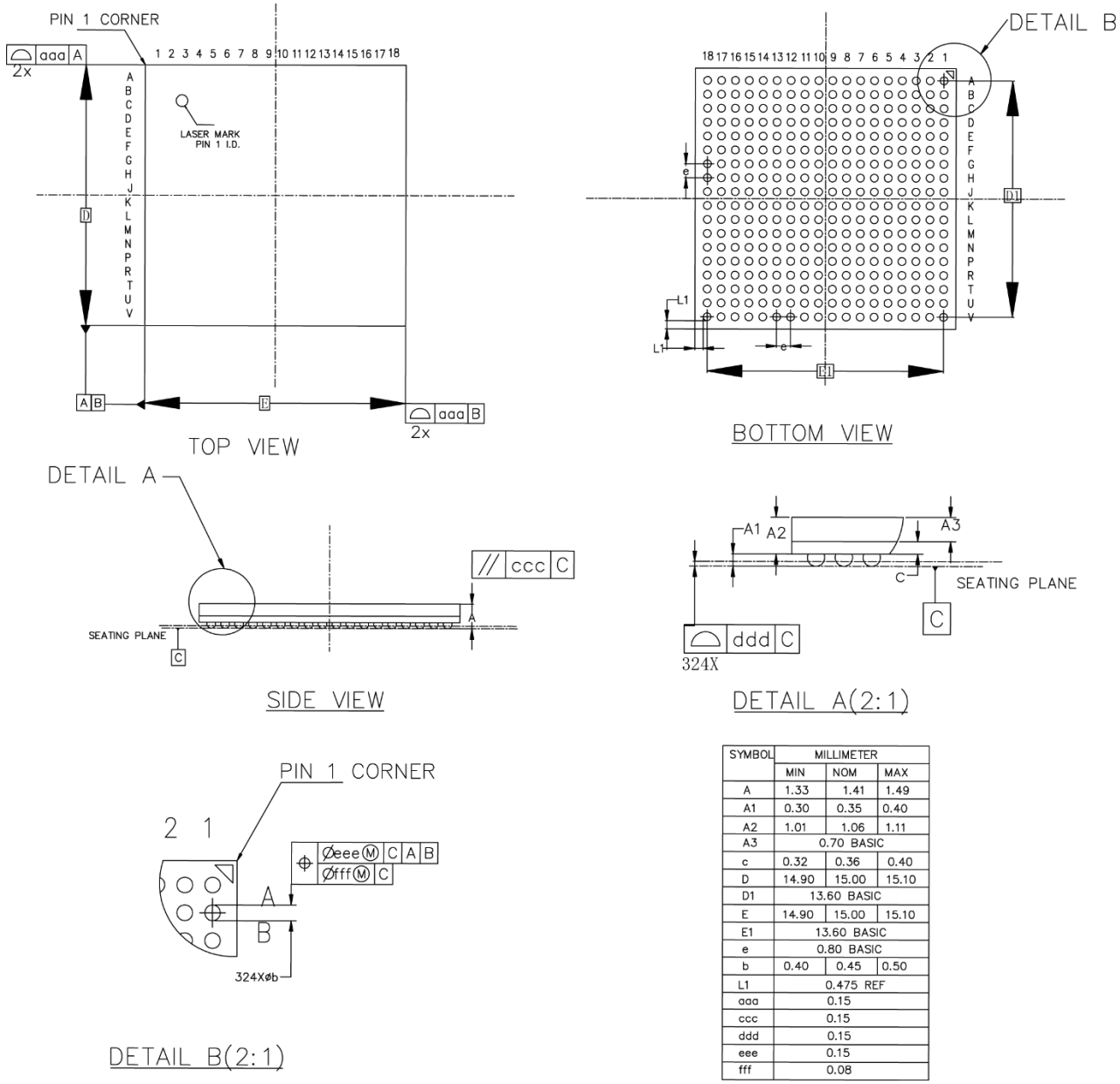


Unit:mm

D	15.00
E	15.00
e	0.80
b	0.40

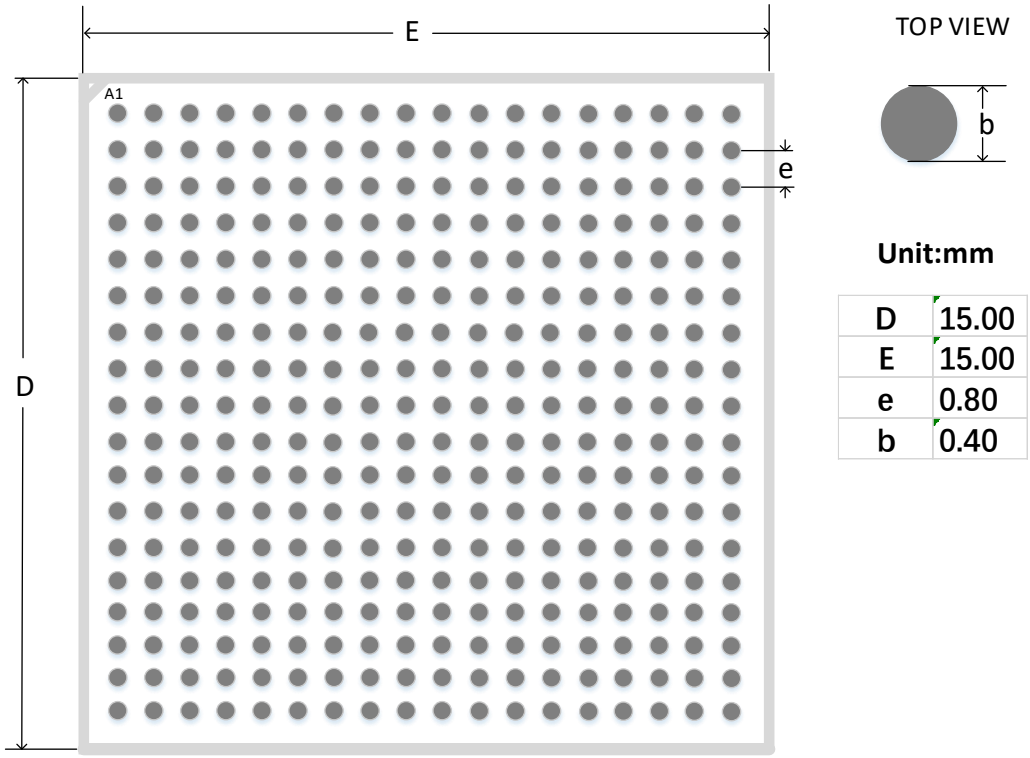
4.13 UG324A Package Outline (15mm x 15mm, GW5AT-60)

Figure 4-25 Package Outline UG324A (GW5AT-60)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.33	1.41	1.49
A1	0.30	0.35	0.40
A2	1.01	1.06	1.11
A3	0.70 BASIC		
c	0.32	0.36	0.40
D	14.90	15.00	15.10
D1	13.60 BASIC		
E	14.90	15.00	15.10
E1	13.60 BASIC		
e	0.80 BASIC		
b	0.40	0.45	0.50
L1	0.475 REF		
aaa	0.15		
ccc	0.15		
ddd	0.15		
eee	0.15		
fff	0.08		

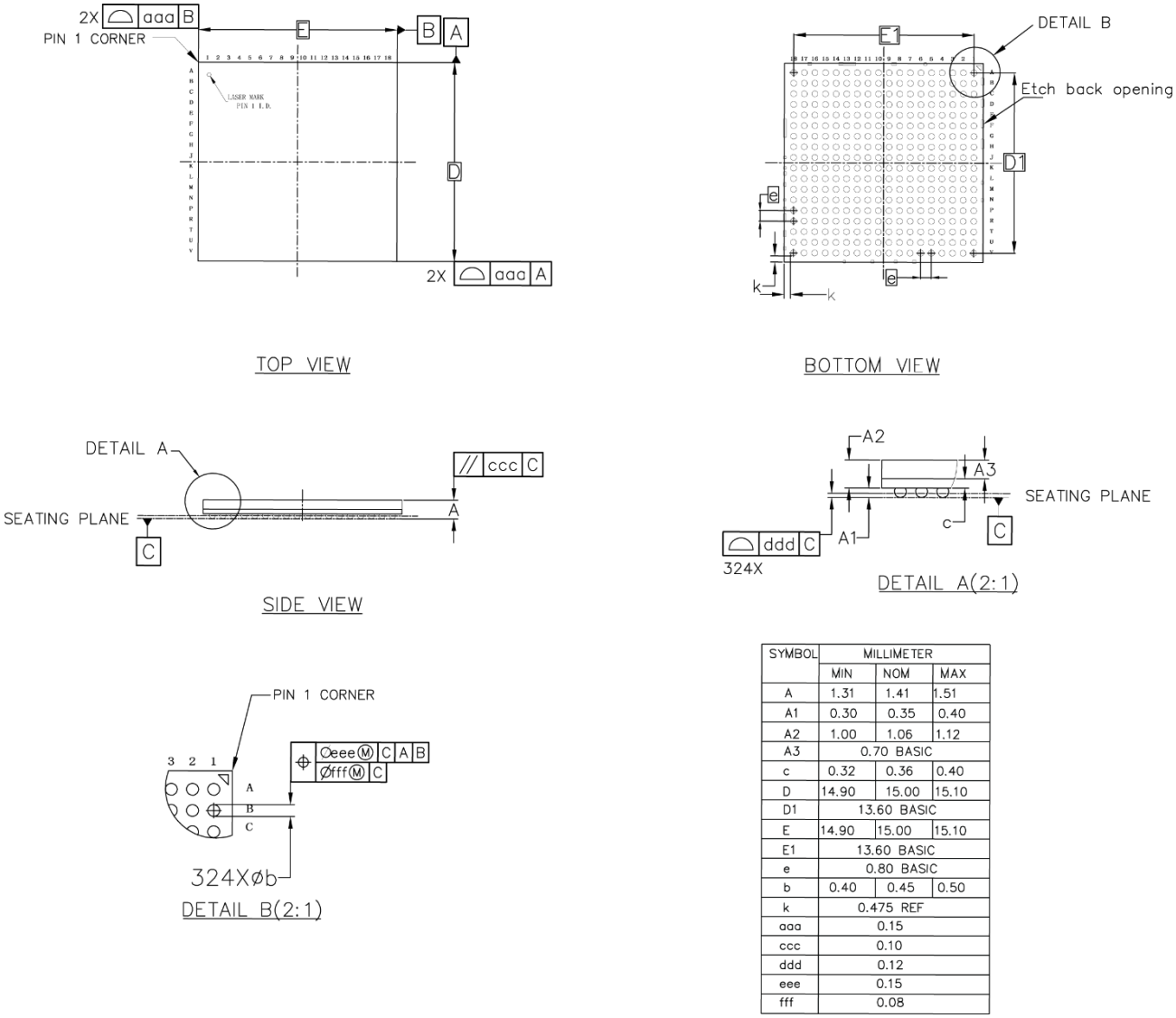
Figure 4-26 Recommended PCB Layout UG324A (GW5AT-60)



D	15.00
E	15.00
e	0.80
b	0.40

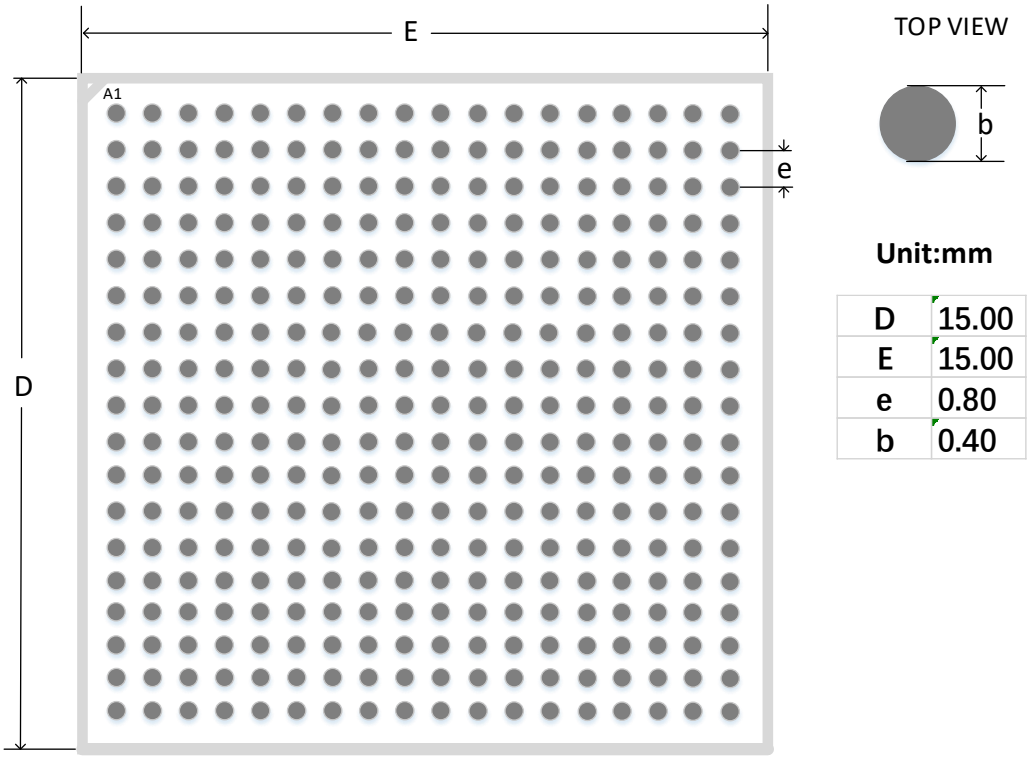
4.14 UG324A Package Outline (15mm x 15mm, GW5AT-138)

Figure 4-27 Package Outline UG324A (GW5AT-138)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.31	1.41	1.51
A1	0.30	0.35	0.40
A2	1.00	1.06	1.12
A3		0.70 BASIC	
c	0.32	0.36	0.40
D	14.90	15.00	15.10
D1		13.60 BASIC	
E	14.90	15.00	15.10
E1		13.60 BASIC	
e		0.80 BASIC	
b	0.40	0.45	0.50
k		0.475 REF	
aaa		0.15	
ccc		0.10	
ddd		0.12	
eee		0.15	
fff		0.08	

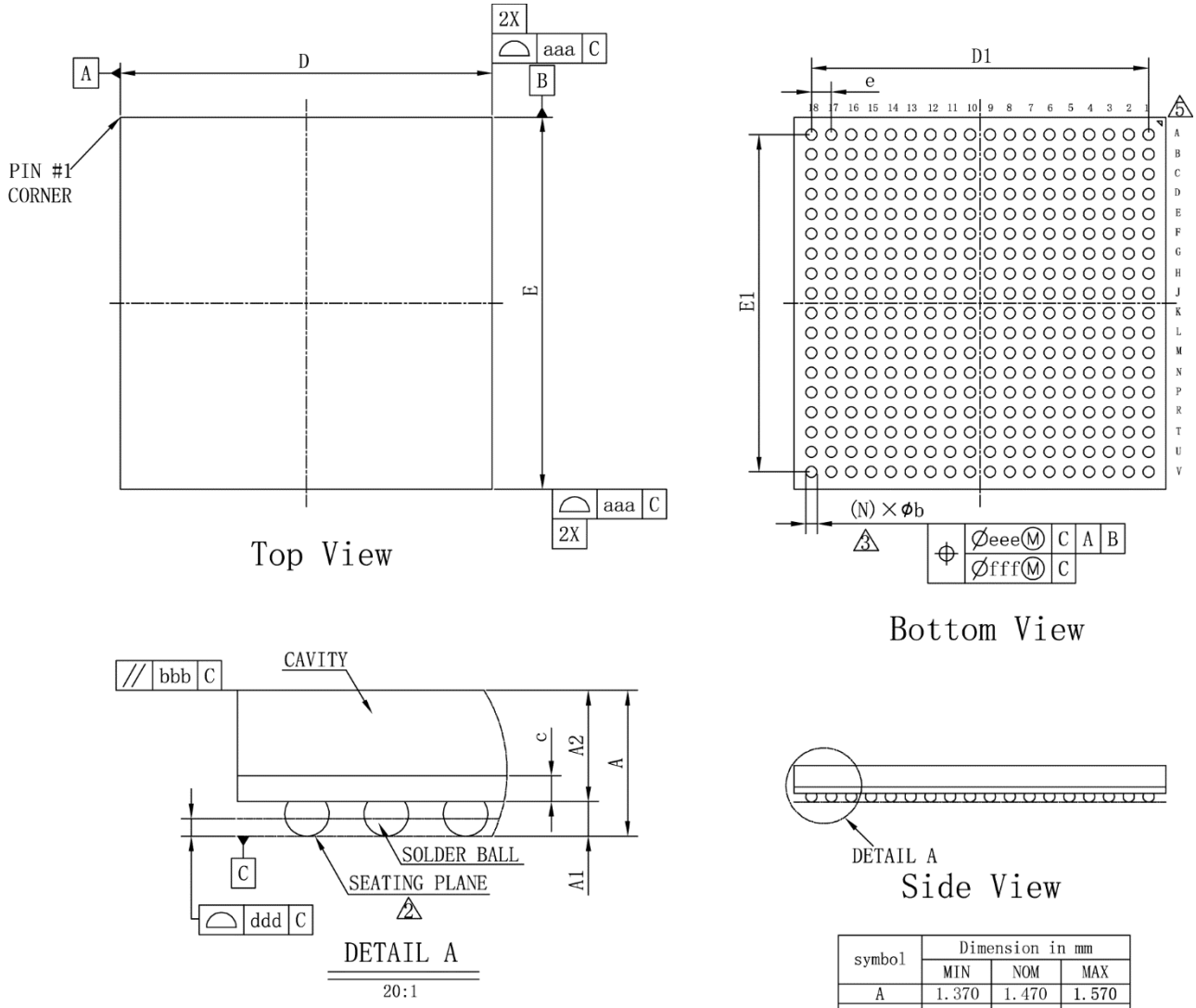
Figure 4-28 Recommended PCB Layout UG324A (GW5AT-138)



D	15.00
E	15.00
e	0.80
b	0.40

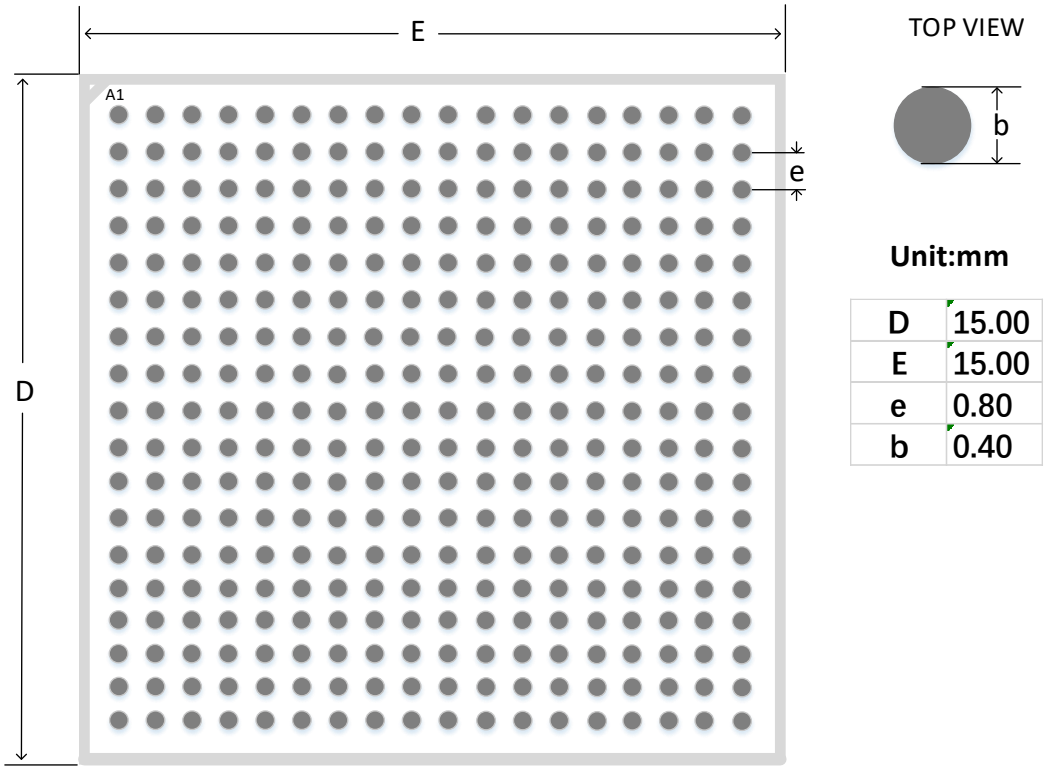
4.15 UG324S Package Outline (15mm x 15mm, GW5AT-60)

Figure 4-29 Package Outline UG324S (GW5AT-60)



symbol	Dimension in mm		
	MIN	NOM	MAX
A	1.370	1.470	1.570
A1	0.300	0.350	0.400
A2	1.070	1.120	1.170
c	0.230	0.260	0.290
D	14.900	15.000	15.100
E	14.900	15.000	15.100
D1	---	13.600	---
E1	---	13.600	---
e	---	0.800	---
b	0.400	0.450	0.500
aaa	0.150		
bbb	0.200		
ddd	0.200		
eee	0.150		
fff	0.080		
Ball Diam	0.450		
N	324		
MD/ME	18/18		

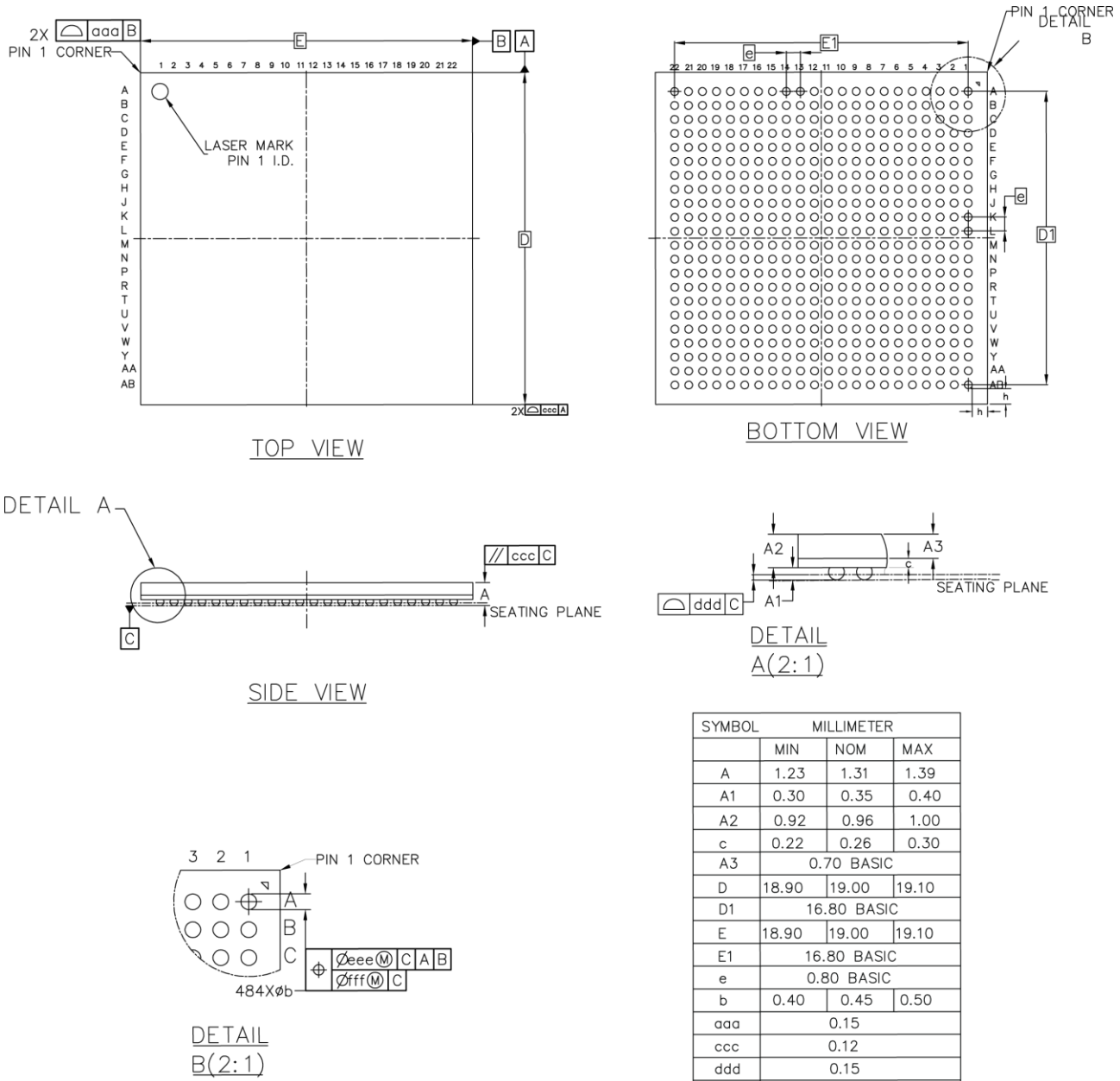
Figure 4-30 Recommended PCB Layout UG324S (GW5AT-60)



D	15.00
E	15.00
e	0.80
b	0.40

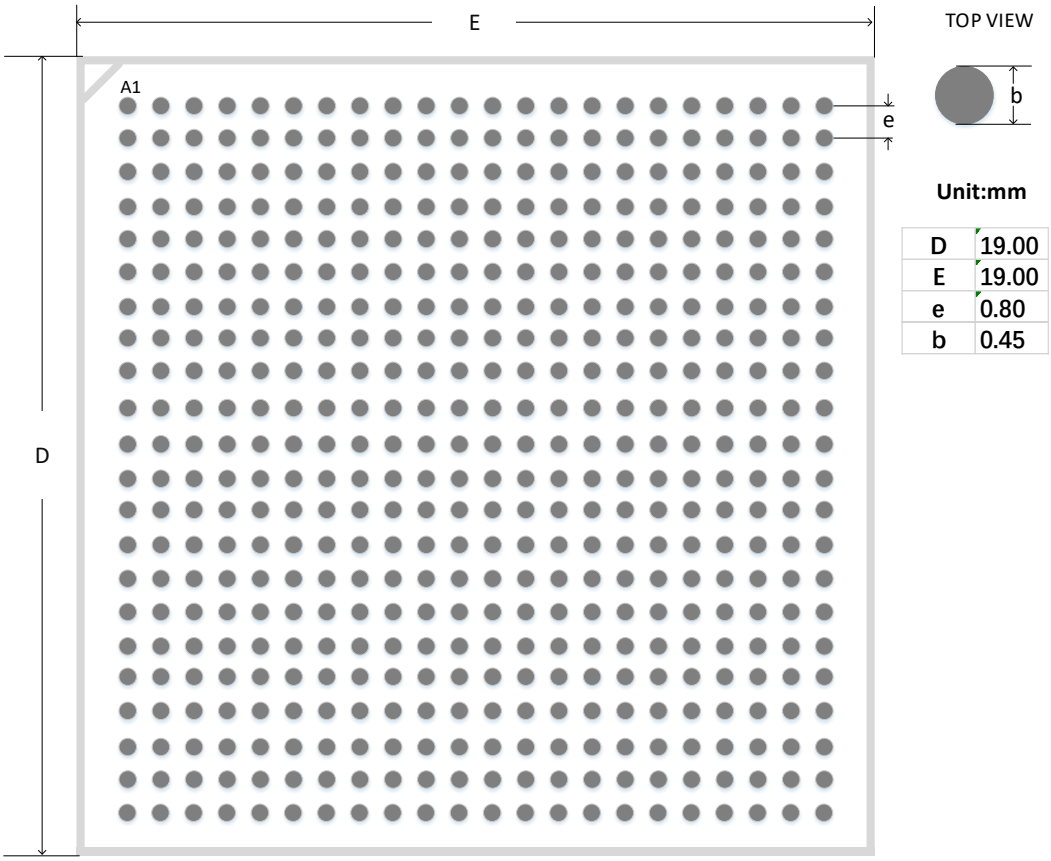
4.16 UG484 Package Outline (19mm x 19mm, GW5AT-75)

Figure 4-31 Package Outline UG484 (GW5AT-75)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.23	1.31	1.39
A1	0.30	0.35	0.40
A2	0.92	0.96	1.00
c	0.22	0.26	0.30
A3		0.70 BASIC	
D	18.90	19.00	19.10
D1		16.80 BASIC	
E	18.90	19.00	19.10
E1		16.80 BASIC	
e		0.80 BASIC	
b	0.40	0.45	0.50
aaa		0.15	
ccc		0.12	
ddd		0.15	
eee		0.15	
fff		0.08	
h		0.875 REF	

Figure 4-32 Recommended PCB Layout UG484 (GW5AT-75)

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