GOWIN
PROGRAMMING FOR THE FUTURE

GW5AT & GW5AST series of FPGA Products

Schematic Manual

UG984-1.2.2E,08/24/2026

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Revision History

Date	Version	Description
04/20/2023	1.0E	Initial version published.
05/25/2023	1.0.1E	● “Figure 2-1 Isolate Wave Filtering” in “2.4 Schematic Design Considerations” updated. ● “Figure 3-1 RECONFIG_N, READY, DONE Schematic Reference Circuit” in “3.1.2 Schematic Design Considerations” updated. ● “4-8 Configuration Modes Supported by Each Device” updated.
06/30/2023	1.0.2E	● “2.2 Power Index” updated. ● PG676A package added to “Table 4-10 GW5AT-138 Configuration Modes” and “Table 4-11 GW5AST-138 Configuration Modes” in “4.8 Configuration Modes Supported by Each Device”. ● The overview in “4.1 MODE” updated.
08/10/2023	1.0.3E	The overview in “4.1 MODE” optimized.
09/12/2023	1.0.4E	● The note of “Table 3-1 RECONFIG_N, READY, DONE Description” in “READY, RECONFIG_N, DONE” added. ● UG324 package added to “Table 4 10 GW5AT-138 Configuration Modes” and “Table 4 11 GW5AST-138 Configuration Modes” in “4.8 Configuration Modes Supported by Each Device”.
11/30/2023	1.0.5E	● UG324A package added to “Table 4 10 GW5AT-138 Configuration Modes” in “4.8 Configuration Modes Supported by Each Device”.
02/02/2024	1.0.6E	● “Table 2-3 Recommendations for Power Combination” in “2.4 Schematic Design Considerations” updated. ● “Table 4 9 GW5AT-75 Configuration Modes” in “4.8 Configuration Modes Supported by Each Device” added.
03/01/2024	1.0.7E	The description of “3.2 CFGBVS” optimized.
07/05/2024	1.1E	● The names of voltage pins updated. ● The content and structure of “4 Configuration Mode” optimized.
07/12/2024	1.1.1E	The note of “Table 2-2 Power Supply Ramp Rate” in “2.3 Power-on Time and Sequence” updated.
10/12/2024	1.1.2E	The note in “6 Pin Distribution” removed.
01/17/2025	1.1.3E	The note and Min. value of V_{CC} ramp rate in “Table 2-2 Power Supply Ramp Rate” in “2.3 Power-on Time and Sequence” updated.
04/30/2025	1.1.4E	The names of voltage pins updated.
06/20/2025	1.1.5E	● The chapter of “Total Power” removed. ● The description of “2.4 Schematic Design Considerations” optimized. ● “Table 4-1 Signal Definition of JTAG Configuration Mode” and its note updated.
08/08/2025	1.2E	“4.6 Configuration Modes Supported by Each Device” added.
03/09/2026	1.2.1E	The description of RECONFIG_N in “Table 3-1 RECONFIG_N, READY, DONE Description” optimized.
08/24/2026	1.2.2E	Updated “6 Pin Distribution” description to include DDR and MIPI I/O information.

Contents

List of Figures

List of Tables

1 About This Guide

1.1 Purpose

This manual describes the characteristics and special features of GW5AT & GW5AST series of FPGA products and provides a comprehensive checklist to guide design processes, aiming to help users better use the Gowin GW5AT & GW5AST series of FPGA products.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- DS981, GW5AT series of FPGA Products Datasheet
- DS1104, GW5AST series of FPGA Products Data Sheet
- UG1224, GW5AT-15 Pinout
- UG1222, GW5AT-60 Pinout
- UG1221, GW5AT-75 Pinout
- UG982, GW5AT-138 Pinout
- UG986, GW5AST-138 Pinout
- UG983, GW5AT series of FPGA Products Package and Pinout Manual
- UG1102, GW5AST series of FPGA Products Package and Pinout Manual
- UG704, Arora V 138K FPGA Products Programming and Configuration User Guide
- UG714, Arora V 25K FPGA Products Programming and Configuration User Guide
- UG718, Arora V 60K FPGA Products Programming and Configuration User Guide
- UG720, Arora V 15K FPGA Products Programming and Configuration User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
CPU	Central Processing Unit
DDR	Double Data Rate
DQS	Bidirectional Data Strobe Circuit for DDR Memory
FPGA	Field Programmable Gate Array
GCLK	Global Clock
GPIO	Gowin Programmable Input/Output
HCLK	High-speed Clock
JTAG	Joint Test Action Group
LDO	Low Dropout Regulator
LVDS	Low-Voltage Differential Signaling
MIPI	Mobile Industry Processor Interface
MSPI	Master Serial Peripheral Interface
PLL	Phase-locked Loop
SPI	Serial Peripheral Interface
SSPI	Slave Serial Peripheral Interface

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Power Supply

2.1 Overview

GW5AT & GW5AST series of FPGA products consist of three groups of voltage, as shown in Table 2-1.

Table 2-1 GW5AT & GW5AST series of FPGA Products Voltage

Group	Name	Description
FPGA	V_{CC}	Core voltage
	V_{CCX}	Auxiliary voltage
	V_{CCIO}	I/O Bank voltage
	V_{CCLDO}	Power supply pin of the internal LDO module voltage that provides voltage for the SRAM
SerDes	V_{DDAQ*}	Power supply of the internal analog circuit voltage of QUAD* for SerDes module
	V_{DDDQ*}	Power supply of the internal digital circuit voltage of QUAD* for SerDes module
	V_{DDHAQ*}	Power supply of the internal high voltage of QUAD* for SerDes module
	V_{DDTQ*}	Power supply of the QUAD* TX transmitter voltage for SerDes module
MIPI	V_{DDAM}	Power supply of the internal analog circuit voltage for MIPI module
	V_{DDDM}	Power supply of the internal digital circuit voltage for MIPI module
	V_{DDXM}	Power supply of the auxiliary voltage for MIPI module

2.2 Power Index

For the power supply requirements of the GW5AT & GW5AST series devices, please refer to the Power section of the following document.

- UG1224, GW5AT-15 Pinout
- UG1222, GW5AT-60 Pinout
- UG1221, GW5AT-75 Pinout

- UG982, GW5AT-138 Pinout
- UG986, GW5AST-138 Pinout

Note!

You should ensure GOWINSEMI products are always used within recommended operating conditions and range. Data beyond the operating conditions and ranges are for reference only. GOWINSEMI does not guarantee that all devices will operate as expected beyond the standard operating conditions and ranges.

2.3 Power-on Time and Sequence

Table 2-2 Power Supply Ramp Rate

Description	Min.	Typ.	Max.
V_{CC} Ramp Rate	0.1 mV/us	-	15 mV/us
V_{CCLDO} Ramp Rate	0.09 mV/us	-	15 mV/us
V_{CCX} Ramp Rate	0.005 mV/us	-	15 mV/us
V_{CCIO} Ramp Rate	0.06 mV/us	-	15 mV/us

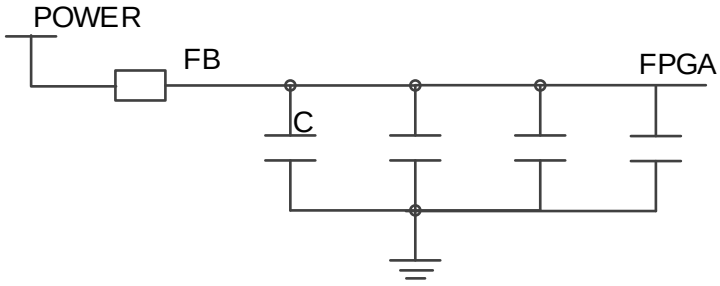
Note!

It is recommended that V_{CCX} is power on before V_{CC}.

2.4 Schematic Design Considerations

1. GW5AT & GW5AST series of FPGA products need to isolate the wave filtering for each voltage, as shown in Figure 2-1.

Figure 2-1 Isolate Wave Filtering



FB is a ferrite bead, C is a ceramic capacitor with accuracy not less than ±10%. For the capacitance value of C, see the minimum FPGA system schematic for each package.

2. Combine power network and isolate ferrite bead.

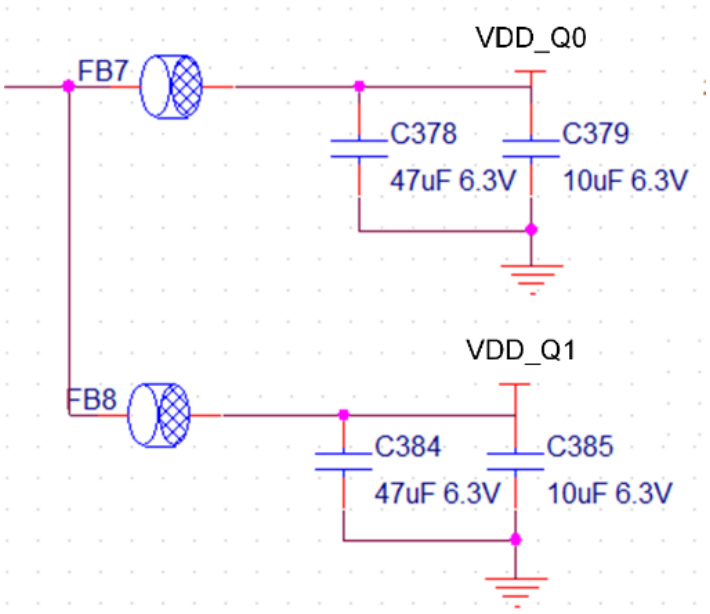
Table 2-3 Recommendations for Power Combination

Group	Name	Recommendations for Power Combination	Supply Voltage
FPGA	V_{CC}	If current is large, it is recommended to supply power independently.	-
	V_{CCX}	With current requirements met, you can consider combining power supplies that are consistent with the supply voltage.	-

Group	Name	Recommendations for Power Combination	Supply Voltage
	V_{CCLDO}	With current requirements met, you can consider combining power supplies that are consistent with the supply voltage.	-
SerDes	V_{DDAQ0} V_{DDAQ1} V_{DDDQ0} V_{DDDQ1}	With current requirements met, you can consider combining power supplies that are consistent with the supply voltage.	It is recommended to use a low noise power supply (e.g. LDO power supply) to ensure SerDes performance.
	V_{DDHAQ0} V_{DDHAQ1}	With current requirements met, you can consider combining power supplies that are consistent with the supply voltage.	
	V_{DDTQ0} V_{DDTQ1}	With current requirements met, you can consider combining power supplies that are consistent with the supply voltage. This group of power supplies is of high noise so that it is recommended that it not be combined with other power supplies.	
MIPI	V_{DDAM} V_{DDDM}	With current requirements met, you can consider combining power supplies that are consistent with the supply voltage.	-
	V_{DDXM}	With current requirements met, you can consider combining power supplies that are consistent with the supply voltage.	-

If you want to combine power supplies, it is recommended that you use ferrite beads for isolation as follows.

Figure 2-2 Isolate with Ferrite Beads



3 Key Configuration Pins

3.1 READY, RECONFIG_N, DONE

3.1.1 Overview

Table 3-1 RECONFIG_N, READY, DONE Description

Name	Description
RECONFIG_N	Active low is used as the reset function for the FPGA programming configuration. FPGA can't be configured if RECONFIG_N is set to low. Keep high-level during FPGA powering up until the powering up is stable for 1ms. As a configuration pin, a low level signal with pulse width no less than 25ns is required for GowinCONFIG to reload bitstream data according to the MODE setting value. You can control the pin by writing logic to trigger the device to reconfigure as required.
READY[1]	Active-high. FPGA can be configured only when the READY signal is pulled up. When the READY signal is pulled down, recover the status by powering up or triggering RECONFIG_N. As a configuration pin, it indicates that the FPGA can be configured or not. If the FPGA meets the configuration condition, the READY signal is high. If the configuration fails, READY signal is low.
DONE[1]	A signal which indicates whether FPGA is configured successfully or not. DONE is pulled up after successfully configuring. As an output configuration pin, it indicates the current configuration of FPGA: if configured successfully, the DONE signal is high and the device enters into working state. if the configuration fails, the DONE signal keeps low. As an input configuration pin, the user can delay the entering of user mode via its own internal logic or by reducing the DONE signal. When RECONFIG_N or READY signals are low, DONE signal also keeps low. When configuring SRAM using JTAG circuit, it does not need to take DONE signal into account. As a GPIO, it can be used as an input or output pin. If DONE is used as an input GPIO, the initial value of DONE should be 1 before configuring. Otherwise, the FPGA will fail to enter the user mode after being configured.

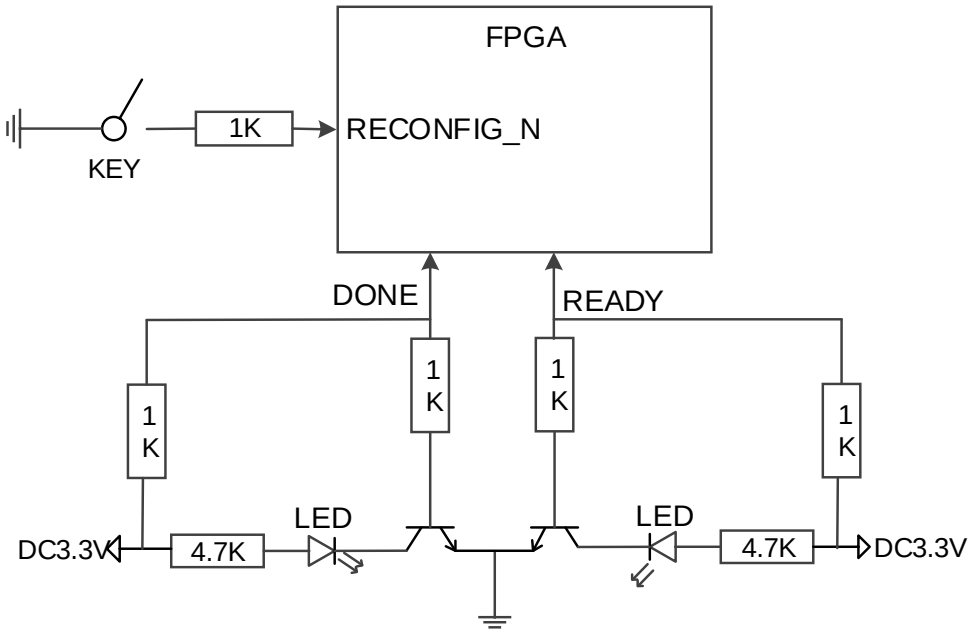
Note!

[1] The default state of READY/DONE is open-drain output, internal weak pull-up. DONE outputs 0 during configuration.

3.1.2 Schematic Design Considerations

READY/DONE is open-drain output, external pull-up resistance is required.

Figure 3-1 RECONFIG_N, READY, DONE Schematic Reference Circuit



Note!

- The values of READY and DONE signals have no meaningful reference in JTAG configuration.
- The unbonded RECONFIG_N, READY, and DONE pins have been internally handled, with no influence on the configuration function.

3.2 CFGBVS

3.2.1 Overview

Table 3-2 CFGBVS Description

Name	Description
CFGBVS	CFGBVS (Configuration Banks Voltage Select) is an input pin. The bank where the configuration IO (JTAG, MSPI, etc.) is located refers to bank3, bank4, and bank10. ● When the V_{CCIO} of the bank where the configuration IO is located is 2.5V and 3.3V, CFGBVS is connected to 1. ● If the V_{CCIO} of the bank where the configuration IO is located is less than 1.8V, CFGBVS is connected to 0.

3.2.2 Schematic Design Considerations

This pin must be set to either High or Low.

3.3 PUDC_B

3.3.1 Overview

Table 3-3 PUDC_B Description

Name	Description
PUDC_B	As a configuration pin, PUDC_B (Pull-up During Configuration (bar)) is an input pin. The FPGA will determine the pin level during the configuration process after power on. ● When it is low, all GPIOs other than this pin will be weakly pull-up [1]. ● When it is high, all GPIOs other than this pin will be high resistance. **Note!** [1] The weak pull-up strength of the 138K/75K devices is Weak. The weak pull-up strength of the 60K devices is Medium.

3.3.2 Schematic Design Considerations

PUDC_B is not allowed to be floating during configuration and can be connected to the V_{CCIO} or GND where it is located through a 1kΩ (or greater) resistor.

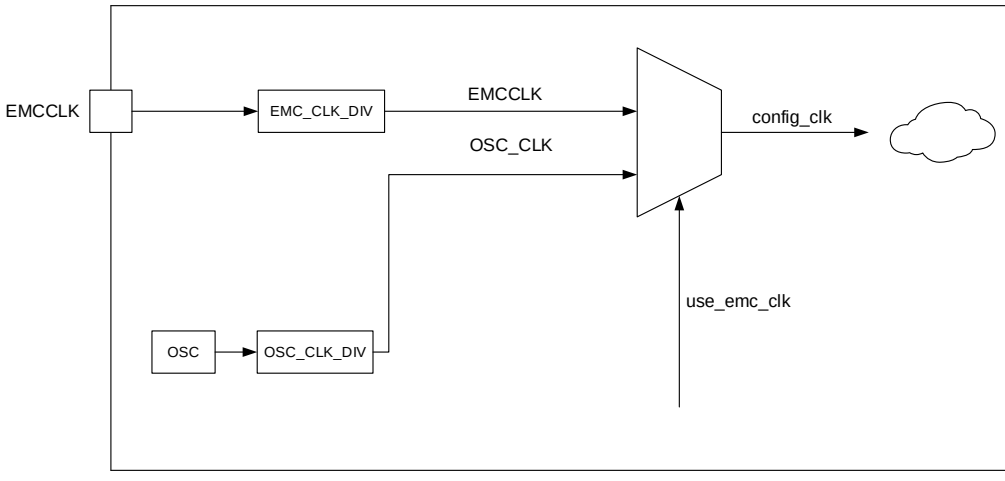
3.4 EMCCLK

3.4.1 Overview

Table 3-4 EMCCLK Description

Name	Description
EMCCLK	Used to configure the optional external clock input source in a master mode (versus the internal configuration oscillator). ● For master mode: FPGA can optionally switch to use EMCCLK as the clock source rather than internal oscillator. ● For slave mode: EMCCLK is not associated with slave mode.

Figure 3-2 EMCCLK and CCLK Diagram



3.5 Configuration Mode Selection Signal (MODE)

3.5.1 Overview

MODE (MODE0, MODE1, MODE2) is GowinCONFIG configuration mode selection signal. When the FPGA powers on or a low pulse triggers the RECONFIG_N, the device enters the corresponding GowinCONFIG state according to the MODE value. MODE [2:0] is used to select the GowinCONFIG programming configuration mode. The configuration mode can be fixed by using pull-up or pull-down resistors. It is recommended to use a 4.7K resistor for pull-up or a 1K resistor for pull-down. As the number of pins for each package is different, some MODE pins are not all bonded out for some devices, and the unbound MODE pins are internally grounded or internal-circuited to V_{CCIO} by default. Please refer to the corresponding PINOUT manual for further details.

Please refer to the following programming configuration manual for the supported configuration modes corresponding to different MODE values:

- *UG704, Arora V 138K FPGA Product Programming and Configuration Guide* > 3.1 Configuration Modes
- *UG714, Arora V 25K FPGA Products Programming and Configuration User Guide* > 3.1 Configuration Modes
- *UG718, Arora V 60K FPGA Products Programming and Configuration User Guide* > 3.1 Configuration Modes
- *UG720, Arora V 15K FPGA Products Programming and Configuration User Guide* > 3.1 Configuration Modes

Please refer to the following Programming Configuration Manual for the pins to be used in each of these configuration modes:

- *UG704, Arora V 138K FPGA Product Programming and Configuration Guide* > 3.2 Configuration Pins
- *UG714, Arora V 25K FPGA Products Programming and Configuration User Guide* > 3.2 Configuration Pins
- *UG718, Arora V 60K FPGA Products Programming and Configuration User Guide* > 3.2 Configuration Pins
- *UG720, Arora V 15K FPGA Products Programming and Configuration User Guide* > 3.2 Configuration Pins

As GPIOs, MODE pins can be used as an input or output. Note that when the MODE value changes, FPGA needs to be powered on again or provided with one low pulse for triggering RECONFIG_N to take effect.

GW5AT & GW5AST series of FPGA products will automatically turn to SSPI mode after the program is loaded successfully. If SSPI mode is not used, make sure that SSPI_HOLDN has a pull-down resistor or SSPI_CSN has a pull-up resistor.

3.5.2 Signal Description

Table 3-5 MODE Signal Definition

Name	I/O	Description
MODE2	I, internal weak pull-down	GowinCONFIG mode selection pin port
MODE1	I, internal weak pull-down	GowinCONFIG mode selection pin port
MODE0	I, internal weak pull-down	GowinCONFIG mode selection pin port

4 Configuration Mode

4.1 JTAG

4.1.1 Overview

In JTAG configuration mode, bitstream data is written to the SRAM of Gowin FPGA products. All configuration data is lost after the device is powered down. All Gowin FPGA products support the JTAG configuration mode.

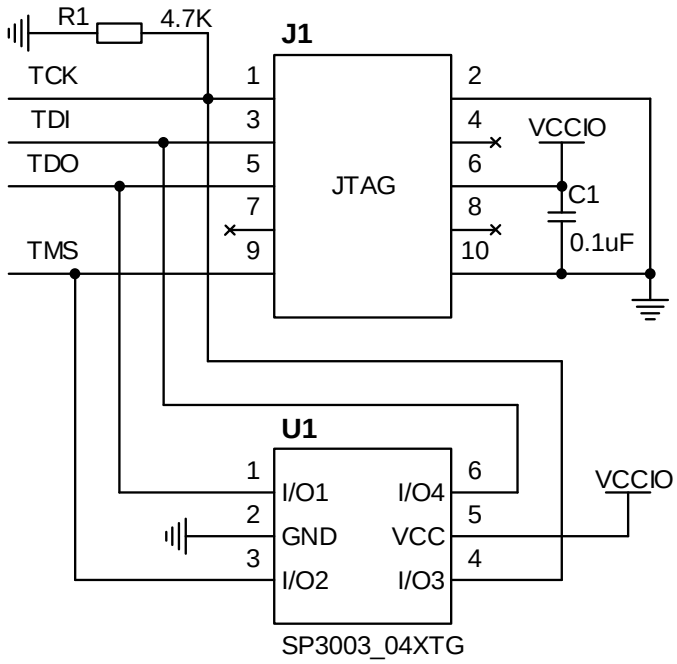
4.1.2 Signal Description

Table 4-1 Signal Definition of JTAG Configuration Mode

Name	Description
TCK	JTAG serial clock input
TMS	JTAG serial mode input
TDI	JTAG serial data input
TDO	JTAG serial data output

4.1.3 JTAG Circuit Reference

Figure 4-1 Connection Diagram for JTAG Configuration Mode



Note!

- The clock frequency for JTAG configuration mode cannot be higher than 100MHz.
- The VCCIO voltage should remain consistent with the voltage of the bank where the JTAG signals are located.

4.2 MSPI

4.2.1 Overview

In MSPI (Master SPI) mode, FPGA is used as a Master and reads bitstream data from the external Flash via SPI interface to complete configuration.

4.2.2 Signal Definition

Table 4-2 Signal Definition of MSPI Configuration Mode

Name	Description
CCLK	Clock Configuration ● Slave mode: CCLK is an input and requires connection to an external clock source ● Master mode: CCLK is an output
MCS_N	Enable signal in MSPI mode, active-low
DIN	Data input in MSPI mode
MOSI	MSPI Mode: Serial instruction and address output. In X2 and X4 modes, the input pin of parallel data bit 0 connects to pin DQ0/D/SI/IO0 of external Flash device.

4.2.3 Circuit Reference

The connection diagram for configuring Gowin FPGA products through MSPI is shown in Figure 4-2 ~ Figure 4-4.

Figure 4-2 Connection Diagram for MSPIx1 Configuration Mode

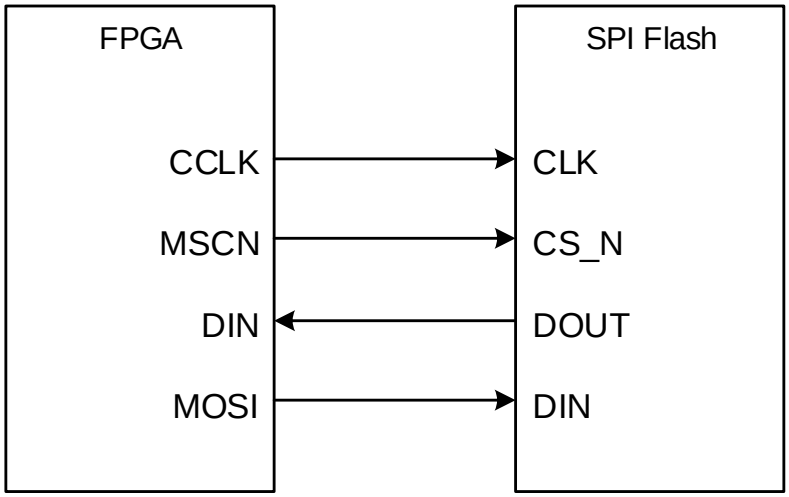


Figure 4-3 Connection Diagram for MSPIx2 Configuration Mode

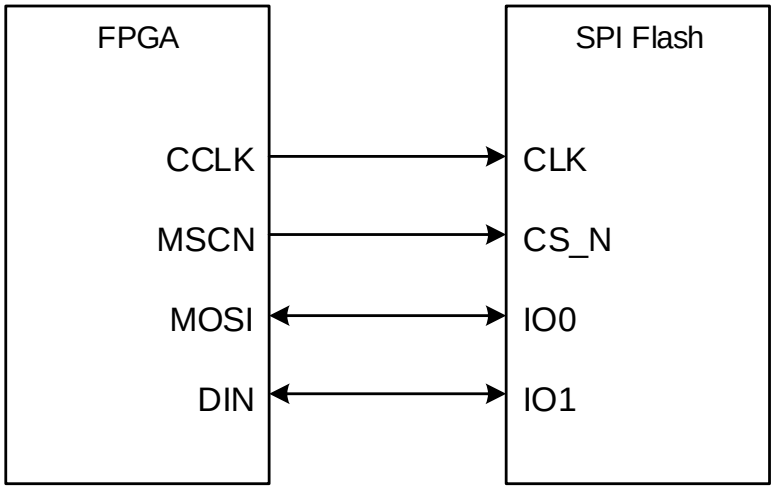
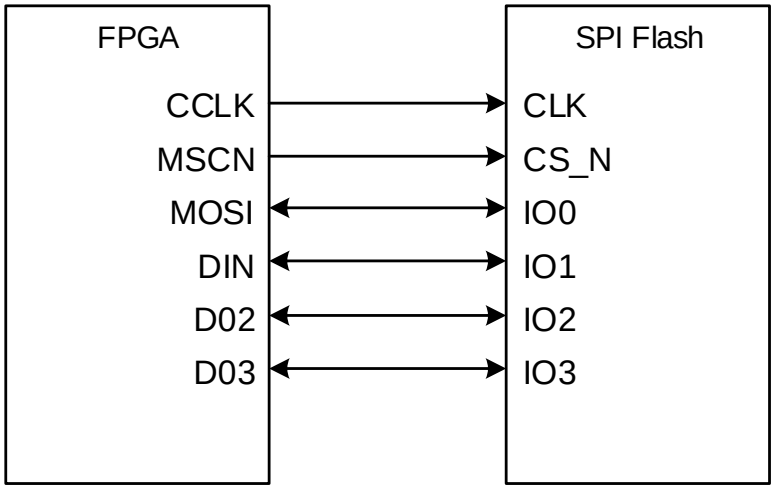


Figure 4-4 Connection Diagram for MSPIx4 Configuration Mode



4.3 SSPI

4.3.1 Overview

In SSPI (Slave SSPI) mode, FPGA is used as a slave device and is configured via SPI interface by an external Host.

4.3.2 Signal Definition

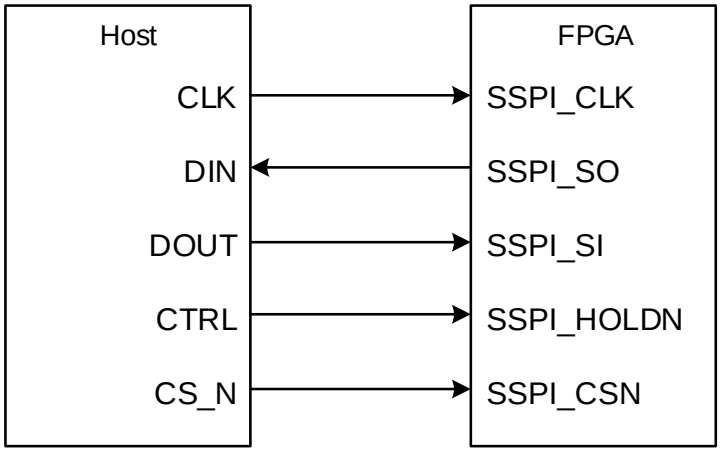
Table 4-3 Signal Definition of SSPI Configuration Mode

Name	Description
SSPI_HOLDN	As a configuration pin, it is an input pin with internal weak pull-up. SSPI clock lock pin: ● When the input is high level, the operation corresponding to SCLK is valid; ● When the input is low level, the operation corresponding to SCLK is invalid. As a GPIO, it can be used as an input or output pin.
SSPI_CSN	As a configuration pin, it is an input pin with internal weak pull-up. It is a chip select signal in the SSPI configuration mode, active low. As a GPIO, it can be used as an input or output pin.
SSPI_CLK	As a configuration pin, it is an input pin. It is a clock input pin of SSPI configuration mode. As a GPIO, it can be used as an input or output pin.
SI	As a configuration pin, it is an input pin. It is a serial data input pin in the SSPI configuration mode. As a GPIO, it can be used as an input or output pin.
SO	As a configuration pin, it is an output pin. It is a serial data output pin in the SSPI configuration mode. As a GPIO, it can be used as an input or output pin.
SSPI_WPN	As a configuration pin, it is an input pin. A write protection pin in SSPI mode: SSPI operation is valid when the input is high, SSPI operation is invalid when the input is low. As a GPIO, it can be used as an input or output pin.

4.3.3 Circuit Reference

The connection diagram for configuring Gowin FPGA products via SSPI is shown in Figure 4-5.

Figure 4-5 Connection Diagram for SSPI Configuration Mode

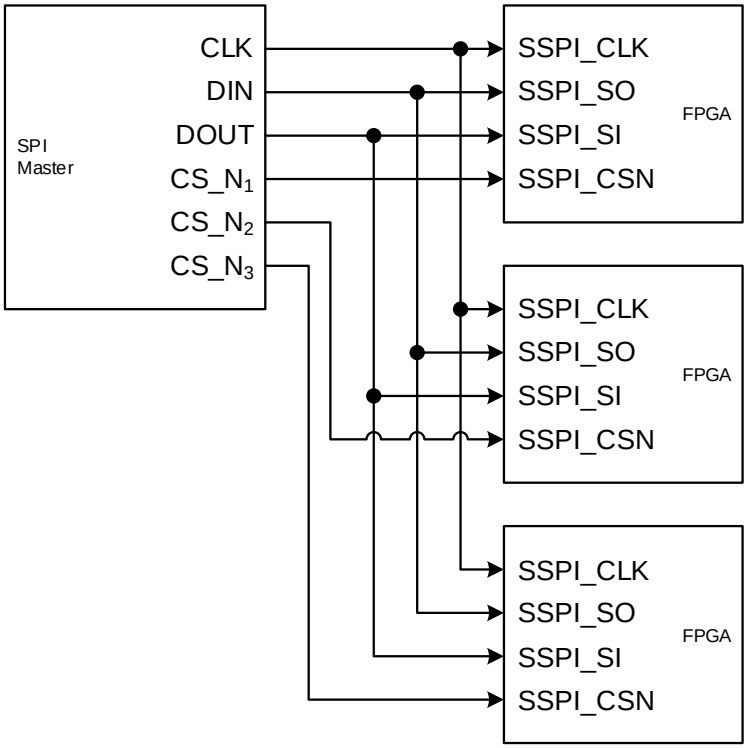


Note!

This figure is the connection diagram for SSPI configuration mode.

The connection diagram for configuring multiple FPGA products via SSPI is shown in Figure 4-6.

Figure 4-6 Multiple FPGA Connection Diagram



4.4 CPU

4.4.1 Overview

CPU mode consists of Master CPU and Slave CPU.

In Master CPU mode (i.e. FPGA is the master device), the configuration data is read from the external via the DBUS interface for configuration.

In Slave CPU mode, GW5AT & GW5AST series of FPGA products are configured by external Host via DBUS interface.

4.4.2 Signal Definition

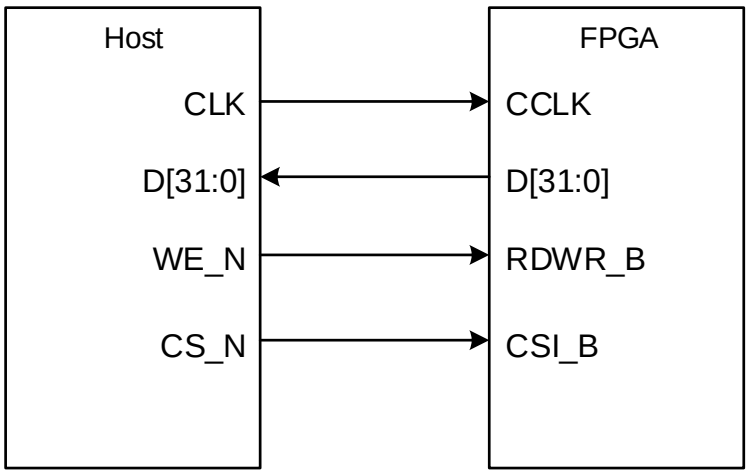
Table 4-4 Signal Definition of CPU Configuration Mode

Name	Description
D00~D31	Input/Output pins In CPU mode, D00~D31 are data input/output pins. The FPGA device will automatically detect the bus width of x8, x16, or x32. As a GPIO, it can be used as an input or output pin.
DIN	In CPU mode, DIN is a multi-function pin as D01 data pin. As a GPIO, it can be used as an input or output pin.
CSI_B	As a configuration pin, it is an input pin. It is a chip select input signal in the CPU mode, active low. ● In master CPU mode, connect to GND directly or via a 1 kΩ (or greater) resistor. ● In slave CPU mode: An external configuration controller can control CSI_B for selecting the devices to be configured on the bus, or in a daisy-chain configuration, connect to the CSO_B pin of the upstream devices.
RDWR_B	As a configuration pin, it is an input pin. Read/write enable signal selection pin in CPU configuration mode ● High, it indicates read operation ● Low, it indicates write operation As a GPIO, it can be used as an input or output pin.
CCLK	As a configuration clock pin, CCLK runs the synchronous FPGA configuration sequence in all modes except JTAG mode. In slave mode: CCLK is an input and requires connection to an external clock source. In master mode: CCLK is an output as configuration source clock. **Note!** CCLK is the key clock signal, so good signal integrity must be ensured.
CSO_B	As a configuration pin, it is an output pin. It is a chip select output signal in the CPU mode. It connects to the CSI_B pin of the downstream FPGA in a daisy-chain configuration.

4.4.3 Circuit Reference

The connection diagram for the CPU mode is shown in Figure 4-7.

Figure 4-7 Connection Diagram for CPU Mode



Note!

CCLK is an output in master mode and an input in slave mode.

Other than the power requirements, the following conditions need to be met to use the CPU configuration mode:

- CPU interface enable
  RECONFIG_N is not set as a GPIO during the first configuration after power up or the previous programming.
- Initiate new configuration
  Power-on again or trigger RECONFIG_N at one low pulse.

4.5 SERIAL

4.5.1 Overview

In SERIAL configuration mode, Host configures Gowin FPGA products through the serial interface. SERIAL is one of the configuration modes that use the least number of pins. It supports both master mode and slave mode. The only difference between the two modes is the different direction of the interface clock. The SERIAL mode can only write bitstream data to FPGA and cannot readback data from FPGA devices; as such, the SERIAL mode cannot read information on the ID CODE and USER CODE and status register.

4.5.2 Signal Definition

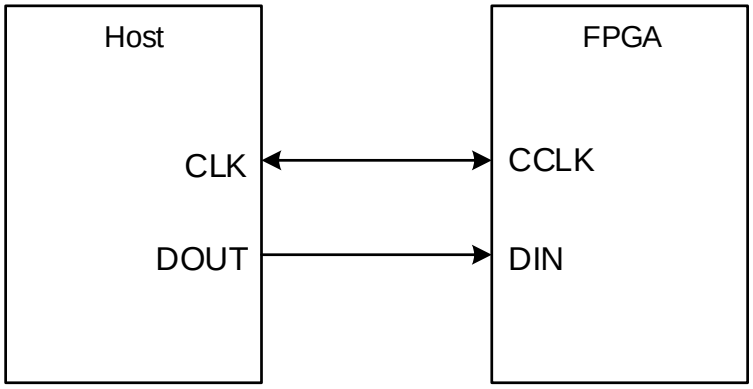
Table 4-5 Signal Definition of SERIAL Configuration Mode

Name	Description
DIN	As a configuration pin, it is an input pin. It is a serial data input pin. ● In SERIAL and MSPI modes: DIN receives serial data from the data source and samples data at the CCLK rising edge in the default configuration. ● In CPU mode, DIN is a multi-function pin as D01 data pin. As a GPIO, it can be used as an input or output pin.
CCLK	As a configuration clock pin, CCLK runs the synchronous FPGA configuration sequence in all modes except JTAG mode. ● In slave mode: CCLK is an input and requires connection to an external clock source. ● In master mode: CCLK is an output as configuration source clock. **Note!** CCLK is a key clock signal, so good signal integrity must be ensured.

4.5.3 Circuit Reference

The connection diagram for the SERIAL mode is shown in Figure 4-8.

Figure 4-8 Connection Diagram for SERIAL Configuration Mode



Note!

CCLK is an output in master mode and an input in slave mode.

4.6 Configuration Modes Supported by Each Device

4.6.1 GW5AT-15

Table 4-6 GW5AT-15 Configuration Mode

Package	JTAG	MSPI	SSPI	Slave Serial	Slave CPU
CS130	Yes	Yes	Yes	Yes	Yes
CS130F	Yes	Yes	Yes	Yes	Yes
MG132	Yes	Yes	Yes	Yes	Yes

4.6.2 GW5AT-60

Table 4-7 GW5AT-60 Configuration Mode

Package	JTAG	MSPI	SSPI	Master Serial	Slave Serial	Master CPU	Slave CPU
CS234	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PG484A	Yes	Yes	Yes	Yes	Yes	Yes	Yes
UG225	Yes	Yes	Yes	Yes	Yes	Yes	Yes
UG225H	Yes	Yes	Yes	Yes	Yes	Yes	Yes
UG324	Yes	Yes	Yes	Yes	Yes	Yes	Yes
UG324A	Yes	Yes	No	Yes	Yes	Yes	Yes
UG324S	Yes	Yes	Yes	Yes	Yes	Yes	Yes

4.6.3 GW5AT-75

Table 4-8 GW5AT-75 Configuration Mode

Package	JTAG	MSPI	SSPI	Master Serial	Slave Serial	Master CPU	Slave CPU
UG484	Yes	Yes	Yes	Yes	Yes	Yes	Yes

4.6.4 GW5AT-138

Table 4-9 GW5AT-138 Configuration Mode

Package	JTAG	MSPI	SSPI	Master Serial	Slave Serial	Master CPU	Slave CPU
FPG676A (FC)	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PG484	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PG484A	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PG484F	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PG676A	Yes	Yes	Yes	Yes	Yes	Yes	Yes
UG324A	Yes	Yes	Yes	Yes	Yes	Yes	Yes

4.6.5 GW5AST-138

Table 4-10 GW5AST-138 Configuration Mode

Package	JTAG	MSPI	SSPI	Master Serial	Slave Serial	Master CPU	Slave CPU
FPG676A (FC)	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PG484A	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PG676A	Yes	Yes	Yes	Yes	Yes	Yes	Yes

5 Clock Pin

5.1 Overview

GW5AT & GW5AST series of FPGA products provide the global clock network (GCLK) which connects to all the device resources directly. In addition to the GCLK, PLL, HCLK, DDR memory interface DQS, etc. are also provided.

For more detailed information of GCLK, HCLK, PLL, and DDR memory interface DQS, see the following manuals.

- UG306, Arora V Clock User Guide
- DS981, GW5AT series of FPGA Products Datasheet
- DS1104, GW5AST series of FPGA Products Data Sheet

GCLK: The GCLK is distributed as 8 clock regions in GW5AT & GW5AST series of FPGA products. Each clock region provides 16 GCLKs. The clock sources of GCLK can be from dedicated clock pins, the output of the PLL, SerDes clocks, the output of HCLK, and common wiring resources. Using a dedicated clock input pin provides better clock performance.

HCLK: HCLK is the high-speed clock in GW5AT & GW5AST series of FPGA products. It can support high-speed data transfer and is mainly suitable for source synchronous data transfer protocols.

PLL: PLL blocks in GW5AT & GW5AST series of FPGA products can configure the parameters to adjust the frequency (multiplication and division), phase, and duty cycle.

DDR Memory Interface Clock DQS

CCLK: As a configuration signal clock, CCLK runs the synchronous FPGA configuration sequence in all modes except JTAG mode.

EMCCLK: EMCCLK as an external clock input, FPGA can optionally switch to use EMCCLK as the clock source rather than internal oscillator.

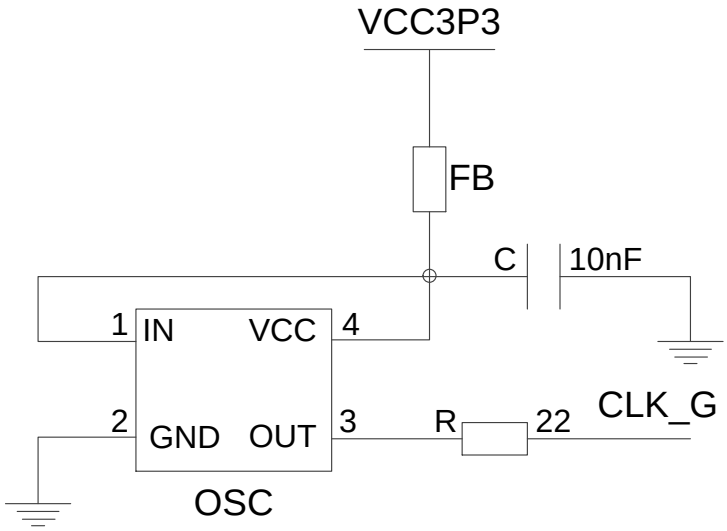
Table 5-1 Clock Overview

Name	Overview
SGCLKT_[x]	Dedicated clock input pin driving the same clock region, T (True), [x]: clock No.
SGCLKC_[x]	Differential input pin of SGCLKT_[x], C (Comp), [x]: clock No.
MGCLKT_[x]	Dedicated clock input pin driving multiple clock region, T (True), [x]: clock No.
MGCLKC_[x]	Differential input pin of MGCLKT_ x], C (Comp), [x]: clock No.
LPLL_C_fb/RPLL_C_fb	Left/Right PLL feedback input pin, C(Comp)
LPLL_T_fb/RPLL_T_fb	Left/Right PLL feedback input pin, T(True)
LPLL_C_in/RPLL_C_in	Left/Right PLL clock input pin, C(Comp)
LPLL_C_in/RPLL_C_in	Left/Right PLL clock input pin, T(True)
EMCCLK	Used to configure the optional external clock input in a master mode (versus the internal configuration oscillator). ● In master mode: FPGA can optionally switch to use EMCCLK as the clock source rather than internal oscillator. ● In slave mode: EMCCLK is not associated with slave mode.
CCLK	As a configuration clock pin, CCLK runs the synchronous FPGA configuration sequence in all modes except JTAG mode. ● In master mode: CCLK is an output as configuration source clock. ● In slave mode: CCLK is an input and requires connection to an external clock source. **Note!** CCLK is the key clock signal, so good signal integrity must be ensured.
TCK	JTAG mode: Serial clock input

5.2 Schematic Design Considerations

1. SerDes high-speed clock: 0.1uf capacitor needs to be connected in series near the FPGA pins.
2. System clock pins selection: GCLK is directly connected to all resources in the device. The GCLK_T end is advised if the GCLK inputs from the single-end. If the external clock as a PLL clock input, it is advised to input from the PLL dedicated pin. And the PLL_T end is selected if the external clock inputs from the single-end.
3. External crystal oscillator circuit is shown in Figure 5-1.

Figure 5-1 FPGA External Crystal Oscillator Circuit



FB is a ferrite bead, with MH2029-221Y reference model, more than ±5% resistance accuracy, and more than ±10% capacitance accuracy.

6 Pin Distribution

6.1 Overview

Before designing circuits, users should take the overall FPGA pin distribution into consideration and make informed decisions related to the application of the device architecture features, including I/O LOGIC, global clock resources, PLL resources, etc.

6.2 LVDS

LVDS is a low-voltage differential signal that offers low power consumption, low bit error rate, low crosstalk, and low radiation. It facilitates the transmission of data using a low-voltage swing high-speed differential. Different packages employ different signals. Please refer to the GW5AT & GW5AST series of FPGA Product Pinout to ensure that the corresponding pins support true LVDS output.

6.3 MIPI IO

GW5AT-15 and GW5AT-60 devices support soft-core MIPI D-PHY RX/TX via MIPI-IO. The MIPI IO integrates an internal resistor network and supports automatic switching between HS and LP modes.

GW5AT-75&GW5AT-138& GW5AST-138 devices support soft-core MIPI D-PHY RX via MIPI-IO (TX not supported). The MIPI IO integrates an internal resistor network and supports automatic switching between HS and LP modes.

GW5AT-15

Package	MIPI TX Soft Core	MIPI TX Soft Core I/O Standard	MIPI TX Soft Core Power Supply Requirements	MIPI RX Soft Core	MIPI RX Soft Core I/O Standard	MIPI RX Soft Core Power Supply Requirements
Dedicated LP TX power supply pins are provided for the following packages: GW5AT-LV15MG132 GW5AT-LV15MG132A0	Supported	MIPI	HS: VCCIO 1.5~3.3V VCCX 1.8~3.3V LP: VCCLDO 1.2V	Supported	MIPI	**HS: VCCIO 1.2~3.3V** VCCX 1.8~3.3V LP: VCCIO 1.2~1.8V
		MIPI_3MA	HS: VCCIO 1.8V VCCX 1.8~3.3V LP: VCCLDO 1.2V			
		MIPI_4MA	HS: VCCIO 1.8V VCCX 1.8~3.3V LP: VCCLDO 1.2V			
The LP TX power supply is shorted to VDD12M for the following packages: GW5AT-LV15CS130F	Supported	MIPI	HS: VCCIO 1.5~3.3V VCCX 1.8~3.3V LP: VDD12M 1.2V	Supported	MIPI	**HS: VCCIO 1.2~3.3V** VCCX 1.8~3.3V LP: VCCIO 1.2~1.8V
		MIPI_3MA	HS: VCCIO 1.8V VCCX 1.8~3.3V LP: VDD12M 1.2V			
		MIPI_4MA	HS: VCCIO 1.8V VCCX 1.8~3.3V LP: VDD12M 1.2V			
GW5AT-LV15CS130	Not Supported			Not Supported		

Note!

- MIPI TX: A V_{CCX} voltage that is too low limits the MIPI data rate. When V_{CCX} is 1.8 V, the MIPI I/O data rate is limited to 1.2 Gbps or lower. For designs requiring a data rate higher than 1.2 Gbps, a V_{CCX} voltage of 2.5 V or higher is required.
- MIPI_3mA/MIPI_4mA: These settings are intended for applications with relatively high channel attenuation. They increase the output VOD, which may exceed the upper limit specified by the MIPI compliance test. However, this does not affect functional operation.
- The V_{CCIO} supply voltage ranges for TX and RX are different.
- LP readback is not supported when V_{CCIO} = 2.5 V or 3.3 V.

The HS RX supply is V_{CCX} and is independent of V_{CCIO}. The V_{CCX} supply range is 1.2 V to 3.3 V.

The LP RX supply is V_{CCIO}, which must be lower than 1.8 V.

GW5AT-60

Package	MIPI TX Soft Core	MIPI TX Soft Core I/O Standard	MIPI TX Soft Core Power Supply Requirements	MIPI RX Soft Core	MIPI RX Soft Core I/O Standard	MIPI RX Soft Core Power Supply Requirements
Dedicated LP TX power supply pins are provided for the following packages: GW5AT-EV60UG324S	Supported	MIPI	HS: VCCIO 1.8~3.3V VCCX 1.8~3.3V LP: VCC 1.2V	Supported	MIPI	HS: VCCIO 1.2~3.3V VCCX 1.8~3.3V LP: VCCIO 1.2~1.8V
		MIPI_3MA	**HS: VCCIO 1.8V** VCCX 1.8~3.3V LP: VCC 1.2V			
		MIPI_4MA	HS: VCCIO 1.8V VCCX 1.8~3.3V LP: VCC 1.2V			
Dedicated LP TX power supply pins are provided for the following packages: GW5AT-LV60PG484A GW5AT-LV60UG324S GW5AT-LV60UG324A **The LP TX power supply is shorted to VDD12M for the following packages:** GW5AT-LV60CS234 GW5AT-LV60UG225 GW5AT-LV60UG324A0	Supported	MIPI	HS: VCCIO 1.8~3.3V VCCX 1.8~3.3V LP: VDD12M 1.2V	Supported	MIPI	HS: VCCIO 1.2~3.3V VCCX 1.8~3.3V LP: VCCIO 1.2~1.8V
		MIPI_3MA	**HS: VCCIO 1.8V** VCCX 1.8~3.3V LP: VDD12M 1.2V			
		MIPI_4MA	HS: VCCIO 1.8V VCCX 1.8~3.3V LP: VDD12M 1.2V			

Note!

- MIPI TX: A V_{CCX} voltage that is too low limits the MIPI data rate. When V_{CCX} is 1.8 V, the MIPI I/O data rate is limited to 1.2 Gbps or lower. For designs requiring a data rate higher than 1.2 Gbps, a V_{CCX} voltage of 2.5 V or higher is required.
- MIPI_3mA/MIPI_4mA: These settings are intended for applications with relatively high channel attenuation. They increase the output VOD, which may exceed the upper limit specified by the MIPI compliance test. However, this does not affect functional operation.
- The V_{CCIO} supply voltage ranges for TX and RX are different.
- LP readback is not supported when V_{CCIO} = 2.5 V or 3.3 V.

The HS RX supply is V_{CCX} and is independent of V_{CCIO}. The V_{CCX} supply range is 1.2 V to 3.3 V.

The LP RX supply is V_{CCIO}, which must be lower than 1.8 V.

GW5AT-75&GW5AT-138&GW5AST-138

Package	MIPI TX Soft Core	MIPI RX Soft Core	MIPI RX Soft Core I/O Standard	MIPI RX Soft Core Power Supply Requirements
GW5AT-LV138PG484 GW5AT-LV138PG484A GW5AT-LV138PG484F GW5AT-LV138PG676A GW5AT-LV138UG324A GW5AT-LV138FPG676A GW5AST-LV138PG484A GW5AST-LV138PG676A	Not Supported	Supported	MIPI	VCCIO 1.2V VCCX 1.8V

Note!

Bidirectional LP is not supported; LP signals are receive-only.

6.4 DDR

To support SSTL, HSTL, etc., each bank also provides one independent voltage source (V_{REF}) as the reference voltage. Users can choose V_{REF} from the internal reference voltage of the bank (0.5 * V_{CCIO}) or external reference voltage V_{REF} using any I/O from the bank.

For DDR related pin distribution, please see *TN662, Gowin FPGA-based DDR2 & DDR3 Hardware Design Reference Manual*.

6.5 Schematic Design Considerations

- It is recommended that all lanes of each MIPI channel be placed in the same Bank and on adjacent differential pairs. When using MIPI-IO RX, the clock lane must be placed on global clock differential pins.
- All Banks of Arora V 15K and 60K devices support on-chip programmable 100 Ω input differential termination.
- The Top and Bottom Banks of Arora V 138K, 75K, and 25K devices support on-chip programmable 100 Ω input differential termination.
- For devices with VREFP/VREFN pins, when the internal reference voltage is selected, a 100 nF capacitor must be connected between VREFP and VREFN. When an external reference voltage is used, VREFP and VREFN should be treated as regular power supply pins.

- GW5AT-15 Device: When the internal differential termination resistor is used, V_{CCX} must be greater than or equal to 3 V.
- GW5AT-15 Device: When V_{CCX} = 1.8 V, the Fmax of the I/O input and output is limited. For I/O applications with data rates greater than 600 Mbps, V_{CCX} must be greater than or equal to 2.5 V.

6.6 Others

For more information on various IO usage, see UG304, *Arora V Programmable IO (GPIO) User Guide*.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